MX·COM, INC.

MX•COM, INC.

MiXed Signal ICs & Modules

1997 PRODUCT DATABOOK

©1997 MX-COM, Inc.

4800 Bethania Station Road, Winston-Salem, NC 27105-1201
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
www.mxcom.com e-mail: mxsales@mxcom.com

Acknowledgments

The following people have made a significant contribution to the authoring and production of this data book:

Gail Bass	Keith Lambeth
William Farlow	Ravi Narala
Ann Hayes	Pamela Roberts
Jim Kemerling	Charles Volk
Fred Kostedt	Brian Scott Wells

Introduction

This data book presents technical specifications and application notes for MX-COM's integrated circuits. Its purpose is to help a customer to successfully select and apply our products. Also included is information concerning MX-COM's abilities to reliably partner with customers and provide high quality service and products in a timely manner.

Contact Us

You can gather the latest information and contact us using our Internet web site, http://www.mxcom.com, or any of the following methods:

Internet website	www.mxcom.com
Internet email	mxsales@mxcom.com
FAX	910-744-5054
Telephone	910-744-5050
Telephone, U.S. only	800-638-5577
Postal address	MX-COM, Inc. 4800 Bethania Station Rd. Winston-Salem, NC 27105 U.S.

Table of Contents

Section	Page
Introduction to MX-COM, Inc.	5
Company Profile	6
Product Profile	7
Worldwide Service	8
Facilities	9
Technology	9
Quality and Reliability	10
Affiliates, Distributors, and Representatives	11
Product Selection Guide	16
Order Information	19
Special Order Devices	20
Technical Specifications	21
Technical Specifications Product List	22
Wireless Modem IC's	1-1
Telephony IC's	2-1
Sub-Audio Tone signaling & Detection IC's	3-1
Sequential Tone Encoder/Decoder	4-1
CVSD CODEC IC's	5-1
Voice Processor IC's	6-1
Voice Security IC's	7-1
Cellular IC's	8-1
General Purpose IC's	9-1
Signal Processing IC's	9-3
Digital Control Amplifier IC's	9-29
Digitally Controlled Analog I/O Processor IC	9-55
Application Notes	10-1
Development Kits	11-1
Appendix	A-1
Glossary of Technical Terms	A-3
Device Handling Procedures	A-7
Package Description	A-9
Tape and Reel Specifications	A-11
Notes	A-17

Introduction to MX-COM Inc.

Description	Page
Company Profile	6
Product Profile	7
Worldwide Service	8
Facilities	9
Technology	9
Quality and Reliability	10
Affiliates	11
Distributors	13
Representatives	15

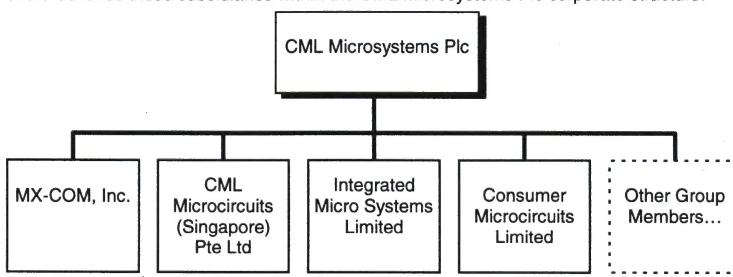
Company Profile

MX-COM, Inc. designs and manufactures integrated circuits, modules, and systems for the communication industries. With core competencies in IC design, manufacturing, and customer service, we serve a variety of commercial, consumer, and industrial markets in both domestic and international territories.

MX-COM is a semiconductor manufacturer with complete sales, marketing, engineering, planning, and manufacturing functions operating according to certified ISO9002 quality procedures.

Conducting business since 1980, MX-COM is a subsidiary of CML Microsystems Plc, a group of technology source companies publicly traded on the London Stock Exchange. Our standard and specialized products are tailored with strong customer participation to meet market needs.

MX-COM shares design technology and expertise on a cooperative basis with other semiconductor oriented subsidiaries within the CML Microsystems Plc Group. This greatly enhances the technical depth and capability supporting new product developments and optimizes the distribution and support of product. The following partial organization chart identifies these subsidiaries within the CML Microsystems Plc corporate structure:



Coordinating closely with Consumer Microcircuits Limited ("CML" for short), a similarly fully functioning affiliate located in England, MX-COM products can be confidently and reliably second sourced by virtue of their independent manufacturing capability.

MX-COM's focused designs provide an attractive balance of power, performance, size, and cost benefits to consistently satisfy customers ranging from small start-up companies to some of the worlds largest, high volume consumer electronics manufacturers.

Product Profile

MX-COM's devices perform critical functions for many familiar end products. Although their most common purpose is to perform or facilitate electronic communications, this can take many forms. The following product examples illustrate some of MX-COM's product range:

- MX102 autocorrelator filters out random noise and preserves coherent tone information to increase S/N and the operating range of pagers.
- MX109 CVSD voice codec digitizes voice for robust, low cost battery powered transmission over wireless links.
- MX589 GMSK filter/modem supports Cellular Digital Packet Data (CDPD) engine to provide digital data messaging in cellular telephones.
- MX602 Caller ID on Call Waiting telecom processor with ring detector, 1200bps FSK demodulator, 2nd call alert dual tone detector, and asynchronous/synchronous serial output port provides a very low cost, low power engine for competitive high volume designs.
- MX818 baseband signal processor streamlines FM land mobile trunked radio addressing/selective squelch applications with Rx and Tx audio processing (limiter, splatter filter, etc.), 15 parallel programmable sub-audio tone detectors, 2 sub-audio tone encoders, digitally controlled amplifiers for two point r.f. modulation support, and 23/24 tone address CODEC.
- MX839 digitally controlled analog I/O processor trims parts count and cost with four input intelligent 8/10 bit A/D monitoring subsystem, three 8/10 bit DACs, two digitally controlled attenuators, programmable A/D clock frequency, and IRQ generator.
- MX919A wireless modem data pump provides a low software overhead engine to achieve robust high performance data networks through the use of root raised cosine filtered four level FSK Tx and Rx demodulation, CRC error detection, interleaving, forward error correction, and embedded packet protocol primitives.
- MX980 digital radio 36kbps $\pi/4$ DQPSK baseband processor for portable radios and base stations uses an optimized DSP engine to provide flexible root raised cosine filters and eight A/D and D/A converters for system support functions.

Worldwide Service

MX-COM products are distributed, sold, and supported worldwide with some exceptions to provide the best customer service possible. Products may be purchased factory direct or via distributors according to customer preference.

Certain regions of the world are jointly served by both MX-COM and CML, the affiliate, via a common local organization. One example organization is CML Microcircuits (Singapore) Pte Ltd, an affiliate dedicated to sales, technical support and distribution functions for the greater Far East territory, excepting Japan, Korea, India, and the Philippines.

The following table identifies the areas served by MX-COM.

Territory	Served by MX-COM	Jointly Served via CML Microcircuits (Singapore) Pte Ltd	Jointly Served via Common Distributor	Served via Separate Distributors	Served by CML, the affiliate
North America South America Philippines	X				
Far East, excluding: Korea, Japan, India, and the Philippines		X			
Japan			X		
Korea				X	
Europe, Israel, Turkey, South Africa, Australia, New Zealand, India					X

Please refer to the Affiliates, Distributors and Representatives section of this chapter to identify those resources which are best suited to your needs.

Facilities

MX-COM occupies a 28,000 square foot purpose-built facility in Winston-Salem, NC, USA, where all functions, except wafer fabrication, are performed. Qualified foundries, operating under strict quality oversight, are used for wafer fabrication.

Technology

Using predominantly 1.2µm CMOS technology, our products use combinations of mixed signal, embedded DSP, and analog design architectures to deliver optimized solutions. Power consumption, size, and cost advantages are achieved using world class IC design and simulation tools which are applied on levels ranging from the system view down to transistor sizing. This design flexibility and latitude is exercised to create best in class solutions which are preferred by both mainstream and smaller market segments.

MX-COM also maintains a strong tradition of working closely with prospects and customers to define new products to better meet the needs of particular industries. This has led to the successful development and introduction of well received products for smaller market segments.

Quality and Reliability

Our quality objective is Total Customer Satisfaction which requires that we satisfy customers in all aspects of their relationship with us. Since January, 1995, MX-COM has been registered to ISO-9002 through Underwriters Laboratories.

Product quality and reliability are an integral part of our product definition objectives and manufacturing practices. For instance, MX-COM products are implemented according to conservative design rules and fabricated using well-established, reliable processes at qualified foundries. Foundry processes are independently tested for reliability performance by MX-COM, in addition to reliability testing which is performed by the foundry. The product is then assembled at the MX-COM facility in North Carolina or by qualified third party assembly operations. Conformance to quality and reliability requirements is strictly monitored through inspection, audit procedures, and periodic reliability monitors. Electrical test, at wafer level and finished assembly, is performed at the Winston-Salem facility using proprietary hardware and software using calibration standards that are NIST traceable. Product traceability is provided throughout the production cycle.

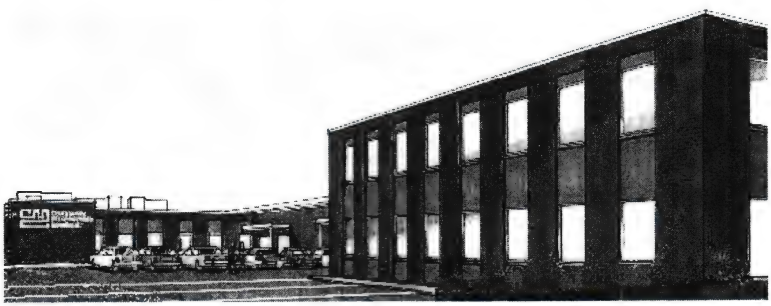
We continue to build on this quality standard and extend it to all aspects of our business.

Affiliates, Distributors and Representatives

Affiliates

As described earlier, MX-COM is one of several subsidiaries of CML Microsystems Plc which work together to provide the best service possible to the global market.

Consumer Microcircuits Limited



CML acts as a qualified second source for MX-COM's integrated circuit products and provides service to Europe, Israel, Turkey, South Africa, Australia, New Zealand and India. Other territories are also served. They may be reached by the following means:

Internet website	www.cmlmicro.co.uk
Internet email	sales@cmlmicro.co.uk
FAX	+44 (0) 1376 518247
Telephone	+44 (0) 1376 513833
Postal address	1 Wheaton Road Witham Essex CM8 3TD England

CML Microcircuits (Singapore) Pte Ltd

CML Microcircuits (Singapore) Pte Ltd provides sales, technical support and distribution functions for products from both MX-COM and CML, the affiliate. Based in Singapore, they are well positioned to support the greater Far East territory excepting Japan, Korea, India, and the Philippines locations. They may be reached by the following means:

FAX	+65 7452917
Telephone	+65 7450426
Postal address	2 Kallang Pudding Road #09-06 Mactech Industrial Building Singapore 349307 Republic Of Singapore

Additional contact information may be found on the CML Microsystems Plc website, http://www.cmlmicro.com.

Integrated Micro Systems Limited

Integrated Micro Systems Limited (IMS) is a custom IC contract design company with strong expertise in a broad range of semiconductor processes and design techniques. With IC design experience spanning baseband to radio frequency, IMS provides a strong technical complement to the other Group affiliates. They may be reached by the following means:

Internet email	ims@ims.co.uk
FAX	+44 1634 715298
Telephone	+44 1634 714285
Postal address	49 Riverside Medway City Estate Rochester Kent ME2 4DP England

Additional contact information may be found on the CML Microsystems Plc website, http://www.cmlmicro.com.

Distributors

Domestic

Component Distributors Inc. CDI

Huntsville, AL
800 888 0331
205 536 8850
205 533 3919 Fax

San Diego, CA
800 372 1580
619 272 1580
619 272 2362 Fax

Littleton, CO
800 551 7357
303 770 6214
303 770 6057 Fax

Palm Bay, FL
800 555 2351
407 724 9910
407 729 6579 Fax

Norcross, GA
800 874 7209
770 441 3320
770 449 1712 Fax

Fort Wayne, IN
219 490 3414
220 489 6934 Fax

Plano, TX
800 848 4234
972 578 2644
972 578 2208 Fax

Annadale, VA
800 293 2080
703 764 9700
703 764 9704 Fax

Seattle, WA
888 734 9600
360 734 9538
360 734 8476 Fax

In Canada
Ottowa, Ontario
613 828 0598
613 828 0563 Fax

Toronto, Ontario
905 890 7799
905 890 2290 Fax

Distributors

International

In Korea

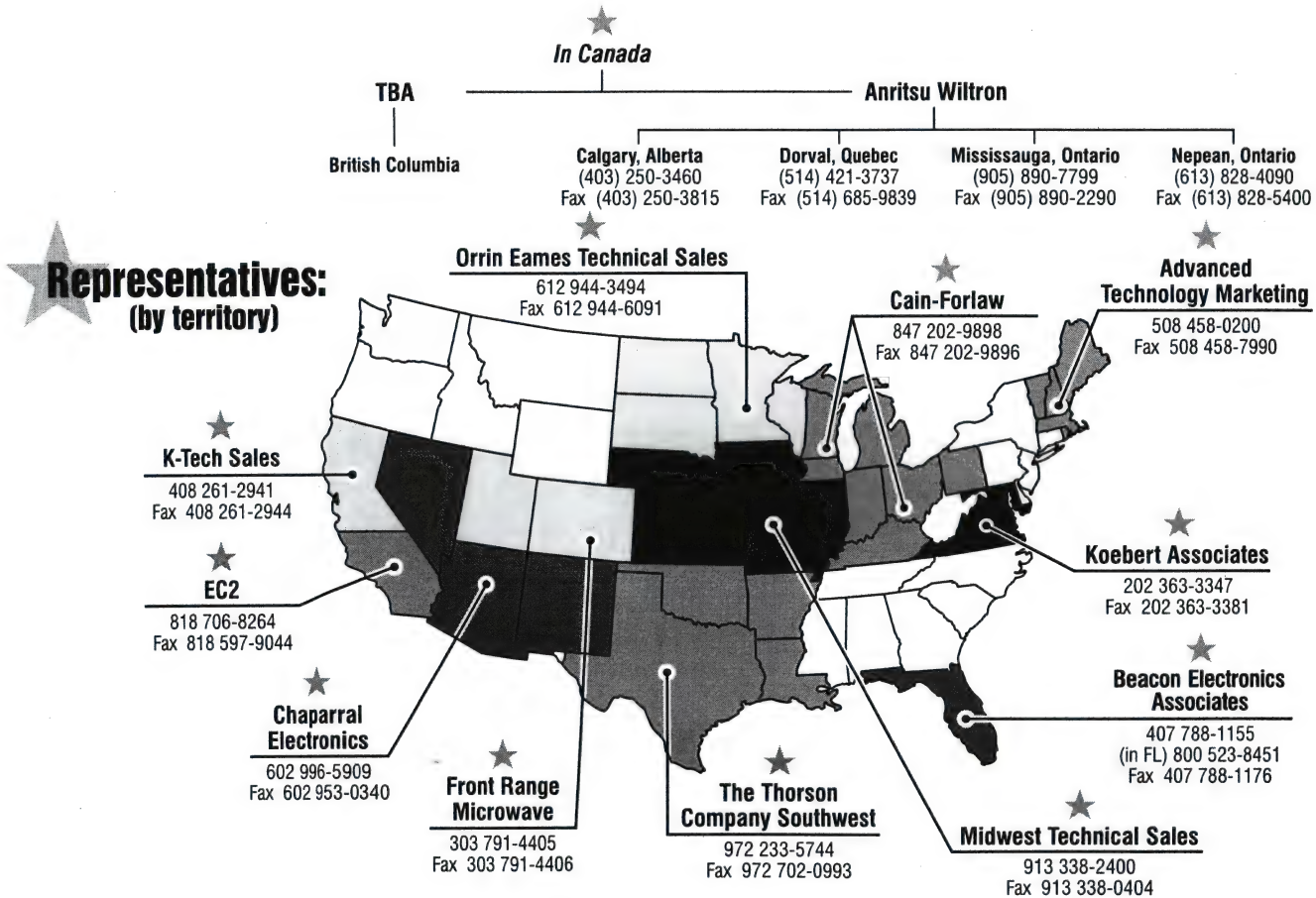
ELECTRO-COMM KOREA
Seoul Office
7th FL., KeumJung Bldg.
11-2, YangJae-Dong
Seo Cho-Ku, Seoul, Korea
02 578 4077
02 578 4079 Fax

In Philippines

PANGAEA CORPORATION PHILIPPINES
Suite 2A Value Point Executive Building
No. 227 Salcedo Street Legaspi Village
1229 Makati City, Philippines
632 810 58 09/10
632 894 54 22
632 810 06 03 Fax

In Japan

CORNES & COMPANY LIMITED
Tokyo Office
Ryukakusan Building
5-12 Higashikanda 2-chome, Chiyoda-ku, Tokyo 101
81 03 5821 1621
81 03 5821 1632 Fax


In Canada
TBA
British Columbia
Anritsu Wiltron
Calgary, Alberta
(403) 250-3460
Fax (403) 250-3815
Dorval, Quebec
(514) 421-3737
Fax (514) 685-9839
Mississauga, Ontario
(905) 890-7799
Fax (905) 890-2290
Nepean, Ontario
(613) 828-4090
Fax (613) 828-5400
Representatives:
(by territory)
Orrin Eames Technical Sales
612 944-3494
Fax 612 944-6091
Cain-Forlaw
847 202-9898
Fax 847 202-9896
Advanced Technology Marketing
508 458-0200
Fax 508 458-7990
K-Tech Sales
408 261-2941
Fax 408 261-2944
EC2
818 706-8264
Fax 818 597-9044
Koebert Associates
202 363-3347
Fax 202 363-3381
Beacon Electronics Associates
407 788-1155
(in FL) 800 523-8451
Fax 407 788-1176
Chaparral Electronics
602 996-5909
Fax 602 953-0340
Front Range Microwave
303 791-4405
Fax 303 791-4406
The Thorson Company Southwest
972 233-5744
Fax 972 702-0993
Midwest Technical Sales
913 338-2400
Fax 913 338-0404

Product Selection Guide

Device	Description	Applications								
		2-WAY MOBILE RADIO	DIGITAL RADIO	CELLULAR PHONES	CORDLESS PHONES	TELEPHONY	WIRELESS DATA	PAGING	VOICE SECURITY	GENERAL PURPOSE
Wireless Modems / Data										
MX429A	1200/2400bps MSK Modem with Parallel Control	✓					✓			✓
MX469	1200/2400bps MSK Modem with Serial Control	✓					✓			✓
MX589	4kbps to 64kbps GMSK Modem	✓	✓	✓	✓		✓		✓	✓
MX604	v.23 1200bps Modem				✓	✓	✓			✓
MX614	Bell 202 1200bps Modem				✓	✓	✓			✓
MX809	1200bps MSK Modem with serial C-BUS Control						✓			✓
MX829	Baseband Signal Processor with MSK Modem, DTMF Encoder and Level Controls, for Trunked Radio Control	✓					✓			✓
MX839	Digitally Controlled Analog I/O Processor		✓	✓			✓			✓
MX909A	GMSK Modem Data Pump (Mobitex™)		✓				✓		✓	✓
MX919A	4-Level FSK Modem Data Pump (Multi-Purpose)		✓				✓		✓	✓
MX929A	4-Level FSK Modem Data Pump (RD-LAP™)						✓		✓	✓
MX949A	CDPD Formatted Wireless Modem GMSK Data Pump			✓			✓			
MX980	Digital Radio Baseband Processor for π/4 DQPSK TETRA	✓	✓				✓			
Telephony										
MX602	Caller ID / Caller ID On Call Waiting				✓	✓				✓
MX604	v.23 1200bps Modem				✓	✓	✓			✓
MX613	Global Call Progress Tone Detector					✓				✓
MX614	Bell 202 1200bps Modem				✓	✓	✓			✓
MX623	Line-Powered Call Progress Tone Detector					✓				✓
MX631	Low Voltage Subscriber Pulse Metering (SPM) Detector					✓				✓
MX633	Call Progress Tone Detector					✓				✓
MX641	Dual Subscriber Pulse Metering (SPM) Detector					✓				✓
MX643	Call Progress Tone Detector with Special Information Tones (SIT)					✓				✓
MX651	Telephone Subscriber Pulse Metering (SPM) Detector and Anti-Fraud Processor					✓				✓

Product Selection Guide

Device	Description	Applications								
		2-WAY MOBILE RADIO	DIGITAL RADIO	CELLULAR PHONES	CORDLESS PHONES	TELEPHONY	WIRELESS DATA	PAGING	VOICE SECURITY	GENERAL PURPOSE
Sub-Audio Tone Signaling & Detection										
MX165C	Low Voltage CTCSS Encoder/Decoder with Tx/Rx Filters	✓								✓
MX315A	CTCSS Encoder	✓								✓
MX375	*Pvt*SQUELCH™ CTCSS Encoder/Decoder with Scrambling	✓							✓	✓
MX465	Low Voltage CTCSS Encoder/Decoder with Tx/Rx Filters	✓								✓
MX805A	Sub-Audio Signaling Processor	✓								✓
MX818	CTCSS Signaling Processor	✓								✓
MX828	CTCSS / DCS / SelCall Signaling Processor	✓								✓
Sequential Tone Encoder/Decoder										
MX803A	Audio Signaling Processor	✓						✓		✓
CVSD CODEC										
MX109	Low Voltage Full Duplex CVSD CODEC with Serial Control				✓				✓	
MX609	PCN/PCS Delta Modulation CODEC				✓				✓	
MX619/629	Military Delta Modulation CODEC								✓	
MX802	Digital Voice Storage & Retrieval CODEC									
MX812	Digital Voice Storage & Retrieval CODEC with DRAM Control									
Voice Processing										
MX506	Mobile Radio Audio Processor	✓								
MX806A	Audio Processor	✓								✓
MX829	Baseband Signal Processor with MSK Modem, DTMF Encoder and Level Controls, for Trunked Radio Control	✓								✓
Voice Security										
MX014	Half-Duplex Voice Band Frequency Inversion Scrambler	✓							✓	✓
MX128	Full-Duplex Cordless Phone Voice Band Frequency Inversion Scrambler	✓			✓				✓	✓
MX224	Variable Split Band Scrambler	✓		✓					✓	

Product Selection Guide

Device	Description	Applications								
		2-WAY MOBILE RADIO	DIGITAL RADIO	CELLULAR PHONES	CORDLESS PHONES	TELEPHONY	WIRELESS DATA	PAGING	VOICE SECURITY	GENERAL PURPOSE
Cellular										
MX316	MNT Audio Filter Array			✓						✓
MX826	AMPS/NAMPS System Audio Processor			✓						
MX839	Digitally Controlled Analog I/O Processor		✓	✓						✓
General Purpose										
MX102	Autocorrelator Random Noise Blanker							✓		✓
MX105A	Tunable Tone Detector							✓		✓
MX019	Quad Digitally Controlled Amplifier									✓
MX029	Dual Digitally Controlled Amplifier			✓						✓
MX839	Digitally Controlled Analog I/O Processor		✓	✓						✓
Development Boards										
DB469	1200bps MSK modem: MX469	✓					✓			✓
DB600	µController companion board for DB602 and DB604				✓	✓				
DB602	Caller ID and Caller ID on Call Waiting: MX602				✓	✓				
DB604	v.23 & Bell 202 1200bps modem with telephone line interface: MX604 & MX614				✓	✓	✓			
DB800	Mobile Radio Baseband Toolset with CTCSS / DCS / SelCall signaling processor, MSK Modem, DTMF Encoder, level controls, trunked radio control processor: MX818, MX828, MX829	✓					✓			✓
DB900	Wireless data: MX909A, MX919A, and MX929A		✓				✓			✓
DB1065	CTCSS subaudio tone decoder & filters: MX465	✓								✓
DBS800	Mobile radio digitally integrated baseband subsystem: MX802, MX803A, MX805A, MX806A, MX809	✓								

ORDERING INFORMATION

TO PLACE AN ORDER:

Contact the MX-COM Customer Service Department.

MX-COM, Inc.
4800 Bethania Station Rd.
Winston-Salem, NC 27105-1201
USA

Phone: (910) 744-5050 OR (800) 638-5577 (Toll-Free in the Continental U.S., Alaska and Canada)

Fax (910) 744-5054.

e-mail: mxsales@mxcom.com

The phones are staffed from 8AM to 5PM E.S.T., Monday through Friday.

Please specify the device package type when placing an order. Package type suffix codes are defined below. See the last section of the data book for package dimensions.

Package Description

Example: MX909AP

MX909 A P

Device	Major Revision Level
MX909	(A, B, C,...)

Package Style

J	CDIP	Ceramic Dual In-Line
P	PDIP	Plastic Dual In-Line
LG LH LH8	PLCC	Plastic Leaded Chip Carrier
DW	SOIC	Small Outline Integrated Circuit
DS	SSOP	Small Shrink Outline Package
TG	TQFP	Thin Quad Flat Pack
TN	TSSOP	Thin Shrink Small Outline Package

SECOND SOURCE:

A qualified second source for MX-COM integrated circuits is CML, the affiliate. Top marks on CML and MX-COM products are the same with the following exceptions:

1. Where MX-COM products bear the MX-COM logo, CML products bear the CML logo.
2. Where MX-COM products bear an "MX" prefix, CML's products bear an "FX" prefix. For example, an MX-COM MX909A device may be second sourced by a CML FX909A.
3. MX-COM and CML products may not have identical pin-outs or package styles. Call the factory for more information
4. Some MX-COM and CML's package styles have different package designator suffixes. For a complete reference list refer to Appendix: Package Description.
5. In some rare instances, the device designator may differ between MX-COM and CML equivalent products. Please contact MX-COM to confirm the device designator for a second source part number.

Special Order Devices

The integrated circuits listed in the Special Order Column are available by special order only. Recommended replacement devices for new designs are shown.

Special Order Device	Recommended Replacement Device for New Design
MX003	MX803A - Audio Signaling Processor
MX004	MX014 - Voice Band Inverter
MX013	MX803A - Audio Signaling Processor
MX009	MX019 - Quad Digitally Controlled Amplifier
MX105	MX105A - Tone Detector
MX118	MX128 - Cordless Telephone Scrambler
MX203	MX803A - Audio Signaling Processor MX829 - Baseband Signal Processor
MX214	MX224 - Variable Split Band Inverter
MX165B	MX165C - CTCSS Encoder/Decoder MX465 - CTCSS Encoder/Decoder MX805A - Sub-Audio Signaling Processor MX818 - CTCSS Signaling Processor MX828 - CTCSS/DCS/SelCall Processor
MX335	same as MX165B, see above
MX355	same as MX165B, see above
MX365	same as MX165B, see above
MX365A	same as MX165B, see above
MX205	MX805A - Sub-Audio Signaling Processor
MX275	MX375 - *Pvt*SQUELCH™ CTCSS Encoder/Decoder
MX336	N/A
MX346	N/A
MX366	MX826 - AMPS/NAMPS System Audio Processor
MX386	MX826 - AMPS/NAMPS System Audio Processor
MX816	MX826 - AMPS/NAMPS System Audio Processor
MX836	
MX409	MX469 - 1200/2400bps MSK Modem with Serial Control
MX419	MX469 - 1200/2400bps MSK Modem with Serial Control
MX429	MX429A - 1200/2400bps MSK Modem with Parallel Control
MX439	MX469 - 1200/2400bps MSK Modem with Serial Control
MX489	MX589 - 4kbps to 64kbps GMSK Modem
MX503	MX803A - Audio Signaling Processor
MX611	MX631 - Low Voltage Subscriber Pulse Metering (SPM) Detector
MX621	MX631 - Low Voltage Subscriber Pulse Metering (SPM) Detector
MX709	MX802 - DVSR Codec MX812 - VSR Codec with DRAM control
MX909	MX909A - GMSK Modem Data Pump (Mobitex™)
MX919	MX919A - 4-Level FSK Modem Data Pump (Multi-Purpose)
MX929	MX929A - 4-Level FSK Modem Data Pump (RD-LAP™)
MX939	MX949A - CDPD Wireless Modem Data Pump

Technical Specifications

MiXed Signal Integrated Circuits

Section	*Description*	*Page*
1	Wireless Modem ICs	1-1
2	Telephony ICs	2-1
3	Sub-Audio Tone Signaling & Detection ICs	3-1
4	Sequential Tone Encoder/Decoder ICs	4-1
5	CVSD CODEC ICs	5-1
6	Voice Processor ICs	6-1
7	Voice Security	7-1
8	Cellular ICs	8-1
9	General Purpose ICs	9-1
10	Application Notes	10-1
11	Development Kits	11-1

Technical Specifications Product List

Wireless Modem ICs		***SECTION 1***
MX429A	**1200/2400bps MSK Modem with Parallel Control**	1-3
MX469	**1200/2400bps MSK Modem with Serial Control**	1-21
MX589	**4kbps to 64kbps GMSK Modem**	1-37
MX809	**1200bps MSK Modem with C-BUS Control**	1-57
MX909A	**GMSK Modem Data Pump (Mobitex™)**	1-71
MX919A	**4-Level FSK Modem Data Pump (Multi Purpose)**	1-111
MX929A	**4-Level FSK Modem Data Pump (RD-LAP™)**	1-149
MX949A	**CDPD Wireless Modem Data Pump**	1-187
Telephony ICs		***SECTION 2***
MX602	**Calling Line Identifier/Calling Line Identifier on Call Waiting**	2-3
MX604	**v.23 Compatible Modem**	2-29
MX613	**Global Call Progress Tone Detector**	2-47
MX614	**Bell 202 Compatible Modem**	2-57
MX623	**Line-Powered Call Progress Tone Detector**	2-75
MX631	**Low Voltage Subscriber Pulse Metering (SPM) Detector**	2-81
MX633	**Call Progress Tone Detector**	2-89
MX641	**Dual Subscriber Pulse Metering (SPM) Detector**	2-101
MX643	**Call Progress Tone Detector with Special Information Tones**	2-117
MX651	**Telephone Subscriber Pulse Metering (SPM) Detector and Anti-Fraud Processor**	2-129
MX663	**Call Progress Decoder**	2-143
Sub-Audio Tone Signaling & Detection ICs		***SECTION 3***
MX165C	**Low Voltage CTCSS Encoder/Decoder with Tx/Rx Filters**	3-3
MX315A	**CTCSS Encoder**	3-19
MX375	***Pvt*SQUELCH™ CTCSS Encoder/Decoder**	3-29
MX465	**Low Voltage CTCSS Encoder/Decoder with Tx/Rx Filters**	3-45
MX805A	**Sub-Audio Signaling Processor**	3-61
MX818	**CTCSS Signaling Processor**	3-79
MX828	**CTCSS/DCS/SelCall Processor**	3-107
Sequential Tone Encoder/Decoder IC		***SECTION 4***
MX803A	**Audio Signaling Processor**	4-3
CVSD CODEC IC		***SECTION 5***
MX109	**Low Voltage Full Duplex CVSD CODEC with Serial Control**	5-3
MX609	**PCN/PCS Delta Modulation CODEC**	5-17
MX619/629	**Delta Modulation CODEC**	5-25
MX802	**DVSR CODEC**	5-39
MX812	**VSR CODEC with DRAM Control**	5-55
Voice Processor ICs		***SECTION 6***
MX506	**Mobile Radio Audio Processor**	6-3
MX806A	**Audio Processor**	6-21
MX829	**Baseband Signal Processor**	6-35
MX980	**Digital Radio Baseband Processor for π/4 DQPSK TETRA**	6-61

Voice Security ICs — *SECTION 7*

MX014	**Voice Band Inverter**	7-3
MX128	**Cordless Telephone Scrambler**	7-15
MX224	**Variable Split Band Inverter**	7-25

Cellular ICs — *SECTION 8*

MX316	**NMT Audio Filter Array**	8-3
MX826	**AMPS/NAMPS System Audio Processor**	8-9

General Purpose ICs — *SECTION 9*

Signal Processing ICs		9-3
MX102	**Autocorrelator**	9-5
MX105A	**Tone Detector**	9-15
Digitally Controlled Amplifier		9-29
MX019	**Quad Digitally Controlled Amplifier**	9-31
MX029	**Dual Digitally Controlled Amplifier**	9-43
Digitally Controlled Analog I/O Processor		9-55
MX839	**Digitally Controlled Analog I/O Processor**	9-57

Application Notes — *SECTION 10*

Practical GMSK Data Transmission	10-3
MX589 GMSK Modem Application	10-15
MX909A Signal Acquisition Principles	10-33
MX909A Fade Management, Data Detection, and Carrier Drift Management	10-37
MSK and its Application to Wireless Data Transmission	10-41
Using an MX469 MSK Synchronous Modem with an Asynchronous Data I/O	10-73
Continuously Variable Sloped Delta Modulation: A Tutorial	10-77
Audio Delay Circuit based on the MX609 CVSD Codec	10-93
Crystal Oscillator Circuit Design	10-95
Tone Generation: An Application of the MX105A	10-99
MX029: Dual Digitally Controlled Amplifier Application	10-107
MX009 and MX019 Amplifier Array Application	10-113
Noise Immunity Circuit for the MX633/643 Call Progress Detectors	10-115
SPM (Subscriber Pulse Metering) for PCMCIA, Data, and Fax Modems	10-119
Error Detection & Correction of MPT1327 formatted messages	10-121
Generation of Non-Standard CTCSS Tones	10-129
Switched Capacitor Interfacing	10-137
Variable Split Band Scrambling	10-147
DBS800 C-BUS System Development Overview	10-153

Development Kits — *SECTION 11*

DB900	**Development Kit for the MX909A, MX919A, and MX929A**	11-3
DB600	**μController Board for use with DB602 and DB604**	11-5
DB602	**Development Kit for the MX602**	11-7
DB604	**Development Kit for the MX604**	11-9
DB469	**Development Kit for the MX469**	11-11
DB800	**Development Kit for the MX818, MX828, and MX829**	11-13
DB1065	**Development Kit for the MX465**	11-15
DBS800	**Development Kit for the DBS800**	11-17

Technical Specifications

Section 1: Wireless Modem IC's

Device	Description	Page
MX429A	1200/2400bps MSK Modem with Parallel Control	3
MX469	1200/2400bps MSK Modem with Serial Control	21
MX589	4kbps to 64kbps GMSK Modem	37
MX809	1200bps MSK Modem with C-BUS Control	57
MX909A	GMSK Modem Data Pump (Mobitex™)	71
MX919A	4-Level FSK Modem Data Pump (Multi Purpose)	111
MX929A	4-Level FSK Modem Data Pump (RD-LAP™)	149
MX949A	CDPD Wireless Modem Data Pump	187

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

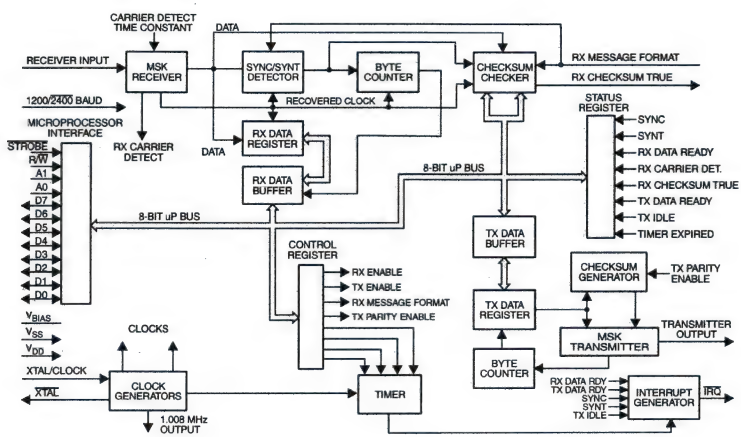
MX429A 1200/2400 Baud MSK Modem

for Trunked Radio Systems

PRELIMINARY INFORMATION

Features

- **Band III & General Purpose Trunked Radio Apps**
- **Full-Duplex 1200 and 2400 Baud Operation**
- **Error Check Word Generation and Checking**
- **Preamble Generation**
- **µProcessor Compatible Interface**
- **Frame SYNC and SYNT Detection**
- **Low Power Consumption**
- **General Purpose Timer**



The MX429A is a single-chip CMOS 1200 and 2400 baud MSK modem, designed primarily for use in trunked radio systems but may also be employed in other general purpose radio or line data communication applications. The device has been designed to conform to the UK Band III trunked radio protocols MPT 1317/1327.

The MX429A is full duplex at 1200 and 2400 baud and includes an 8-bit parallel microprocessor interface and a programmable timer which may be set for interrupt periods of 8 to 120 bits. Preamble may be generated by the device in transmit. The 16-bit SYNC or SYNT words are detected in receive. An error check word is automatically generated in transmit and error checking is performed in the receive mode. An on-chip Xtal/clock generator requiring an external 4.032MHz Xtal or clock input provides both 4.032MHz and 1.008MHz outputs and performs all modem timings.

The MX429A requires a single 5-volt power supply and has a powersave facility and is available in the following package styles: 24-pin CDIP (MX429AJ), 24-pin PDIP (MX429AP), and 24-pin PLCC (MX429ALH).

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480128.003
All trademarks and service marks are held by their respective companies.

CONTENTS

Section **Page**

1. Block Diagram 1-5

2. Signal List 1-5

3. External Components 1-7

4. General Description 1-8

4.1 Modems in Mobile Data Signaling 1-8

4.1.1 Digital Code Format 1-8

4.1.2 Operation 1-8

4.1.3 Non MPT Application – Full-Duplex 1-9

4.1.4 Control Register 1-9

4.1.5 Status Register 1-10

4.1.6 Rx Data Buffer 1-11

4.1.7 Tx Data Buffer 1-11

4.2 Syndrome Word 1-12

4.2.1 Syndrome Low Byte 1-12

4.2.2 Syndrome High Byte 1-12

4.3 Carrier Detect Time Constant 1-12

5. Application 1-13

5.1 Checksum Generation and Checking 1-13

5.2 Receive Operation 1-13

5.3 Transmit Operation 1-14

5.4 Basic Power Up Software 1-15

5.5 Basic Software Interrupt Flow 1-16

6. Performance Specification 1-17

6.1 Electrical Performance 1-17

6.1.1 Timing 1-19

6.2 Packaging 1-19

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1. Block Diagram

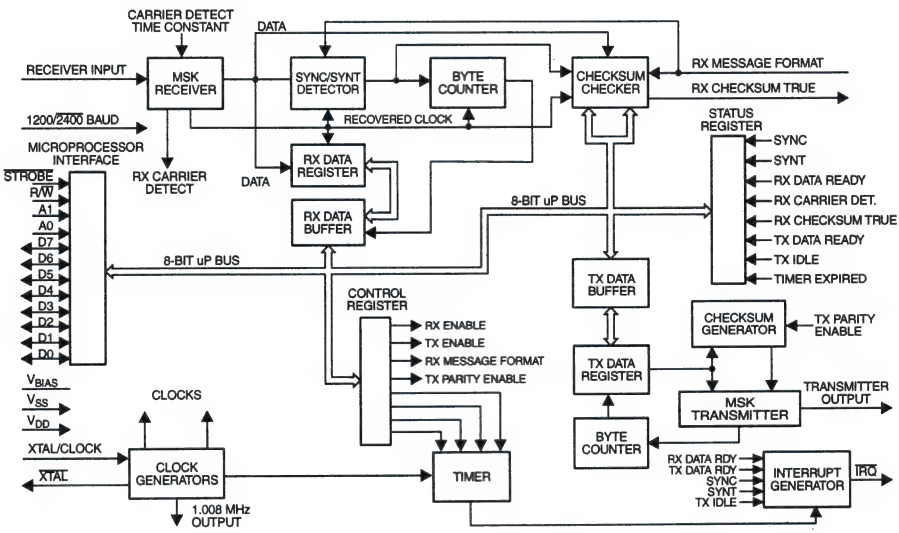


Figure 1: Block Diagram

2. Signal List

Pin No.		Signal		Description
J/P	LH	Name	Type	
1	1	V_{BIAS}		The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS} by a capacitor, see Figure 2.
2	2	Transmit Output	Output	The 1200 baud, 1200Hz/1800Hz and 2400 baud, 1200Hz/2400Hz MSK Tx output. When not enabled by the Control Register (D0) its output impedance is set high.
3	4	Receiver Input	Input	The 1200/2400 baud received MSK signal input. The 1200Hz/1800Hz, 1200Hz/2400Hz audio to this pin must be ac coupled via a capacitor, see Figure 2.
5	5	V_{DD}	Power	Positive Supply. A single +5V regulated supply is required. It is recommended that this power rail be decoupled to V_{SS} by a capacitor, see Figure 2.
6	6	Carrier Detect Time Constant:		The on-chip Carrier Detect function requires external component(s) on this pin. See Figure 2for recommended component(s).
7	7	Xtal/Clock		The input to the clock oscillator inverter. A 4.032 MHz Xtal or externally derived clock pulse input should be connected here, see Figure 2.
8	8	$\overline{XTAL}$		The output of the 4.032 MHz clock oscillator.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Pin No.		Signal		Description
J/P	LH	Name	Type	
9	9	D0		Microprocessor Data Interface These 8 lines are used by the device to communicate with a micro-processor with the R/$\overline{W}$, A0 and A1 inputs determining register selection.
10	10	D1		
11	11	D2		
12	12	D3		
13	13	D4		
14	14	D5		
15	15	D6		
16	16	D7		
17	17	A0		Register Selection: These inputs, with the R/$\overline{W}$ input, select the required register to the data bus as shown in Table 2
18	18	A1		
19	19	$\overline{STROBE}$		Performs the dual functions of selecting the device for Read or Write and strobing data in or out. It should be generated by gating the high order address bits with a Read/Write clock. The MX429A is selected when this pin is a logic '0'.
20	20	R/$\overline{W}$		Used in conjunction with A1 and A0 to determine which internal registers are connected to the data interface pins (D0 to D7) during Strobe.
21	21	$\overline{IRQ}$		Interrupt Request. This line will go to a logic '0' when an interrupt occurs. This output can be "wire OR'd" with other active low components (100kW pullup to V_{DD}). The conditions that cause the interrupts are indicated at the Status Register and are as follows: Timer Expired, Rx Data Ready, Tx Data Ready, Tx Idle, Rx SYNC Detect, Rx SYNT Detect
22	24	1200/2400 Baud Select		A logic '1' on this pin selects the 1200 baud option. Tone frequencies are: one cycle of 1200Hz represents a logic '1', one and a half cycles of 1800Hz represents a logic '0'. A logic '0' on this pin selects the 2400 baud option. Tone frequencies are: one half cycle of 1200Hz represents a logic '1', one cycle of 2400Hz represents a logic '0'. This pin has an internal 1MΩ pullup resistor.
23	22	V_{SS}	Power	Negative Supply (GND)
24	23	Clock/4		A 1.008 MHz (X1 ÷ 4) clock is available at this output for external circuit use, note the source impedance and source current limits.
4	3			Leave this pin open-circuit

Table 1: Signal List

Register	R/$\overline{W}$	A0	A1
Control	0	1	1
Status	1	1	1
Rx Data	1	0	1
Tx Data	0	0	1
Syndrome Low	1	0	0
Syndrome High	1	1	0

Table 2: Register Selection

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components

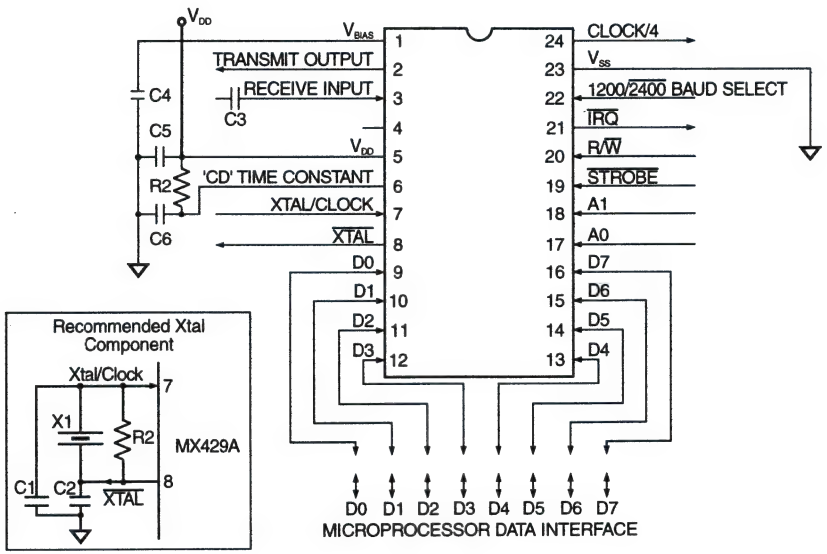


Figure 2: Recommended External Components

R1		1MΩ	±10%
R2		1MΩ	±10%
C1		33pF	±20%
C2		33pF	±20%
C3		0.1µF	±20%

C4		1.0µF	±20%
C5		1.0µF	±20%
C6		1.0µF	±20%
X1	Note 1	4.032MHz	

Table 3: Recommended External Components

Notes:

1. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of VDD, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4. General Description

4.1 Modems in Mobile Data Signaling

4.1.1 Digital Code Format

The MPT 1327 Signaling Standard for Trunked LMR Systems protocol is used by the MX429 for communication between a Trunking System Controller (TSC) and users' radio units. These data stream formats are summarized in Figure 3.

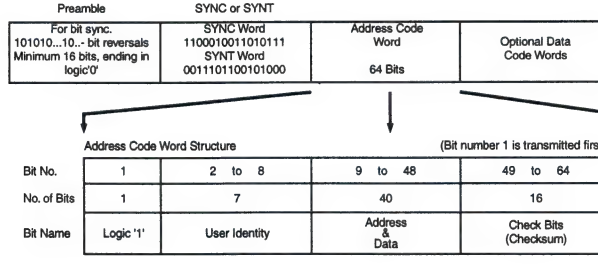


Figure 3: Tx and Rx Data Stream

4.1.2 Operation

The MX429A can be used for Full-Duplex operation with the host microprocessor only having to operate on the data whilst the modem (MX429A) handles all other signaling routines and requirements.

In the Tx mode the MX429A will :

1. Internally generate and transmit a preamble – bit reversals, for system bit synchronization.
2. Accept from the host, and transmit, a 16-bit 'SYNC' or 'SYNT' word.
3. Accept from the host, and transmit, 6 bytes of data (Address Code Word):
   A. Upon a software command, internally calculate and transmit a 2-byte checksum based on the previous 6 data bytes.
   B. Upon a software command, disable internal checksum generation and allow continuous data transmission.
4. Transmit 1 'hang bit' and go idle when all loaded data traffic has been sent (followed by a "Tx Idle" interrupt).

In the Rx mode the MX429A will:

1. Detect and achieve bit synchronization within 16 bits.
2. Search for and detect the 16-bit 'SYNC'/'SYNT' word.
3. Output all received data after 'SYNC/SYNT,' in byte form.
4. Upon a software command (Rx Message Format), use the received checksum to calculate the presence (if any) of errors, and advise the host with an interrupt and a 16-bit Syndrome word.

Note: In Rx, a software command is used to determine whether a 'SYNC'/'SYNT' word is required after every 8 (6 data + 2 checksum) received bytes, or "data" is received continually.
Normally the 'SYNC' word is used on the Control data channel and the 'SYNT' word is used on the Traffic data channel.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.1.3 Non MPT Application – Full-Duplex

The functions described in this section, to allow the MX429A modem to operate as a general purpose device, are obtained using the commands and indications detailed in the "Register Instructions" pages.

Tx: When enabled the device transmits a "101010.....10" preamble until data for transmission is loaded by the host microprocessor. Transmits 6 bytes of the loaded data followed by a 2-byte checksum based on that data. As long as Tx data is loaded the transmitter will transmit, the 2-byte checksum being produced after every 6 bytes (8 byte packages). Automatic checksum generation can be inhibited by a software command to allow transmission of continuous data streams.

Rx: When enabled requires the 16-bit SYNC or SYNT word (see notes) before outputting data bytes. The modem receiver will then output continuous bytes of data, after every 6 bytes received a 2-byte checksum word will be output and can be ignored or used for error checking.

4.1.4 Control Register (A1 = 1, A0 = 1, R/$\overline{W}$ = 0, Write Only)

The Control Register, when selected, directs the modem's operation as described in Table 4

Bit	Description	Function
Bit 0 D0	TX Enable	**Set**: D0 enables the transmitter for operation. A '0 – 1' transition causes bit synchronization and the start of 1010.....10 preamble pattern transmission. At least one byte of preamble will be transmitted. If data is loaded into the Tx Data Buffer before one byte has been sent then that data will follow, otherwise whole bytes of preamble will continue until data is loaded. **Clear**: The Transmitter Output pin is set to a high impedance and no transmitter interrupts are produced.
Bit 1 D1	Tx Parity Enable	**Set**: D1 indicates to the transmitter that 2–byte checksums are to be generated by the modem. A '0 – 1' transition starts checksum generation on the next six bytes loaded from the Tx Data Buffer into the Tx Data Register. Checksum generation continues for every 6 bytes loaded until this bit is cleared. The transmitter will send the generated checksum (2 bytes) after the last of each 6 bytes have been sent. If an underrun (no more data loaded) condition occurs before 6 bytes have been loaded checksum generation will abort, the transmission will cease after one 'hang' bit has been sent and Bit 4 in the Status Register (Tx Idle) will be set. No checksum will be transmitted. **Clear**: No checksum generation is carried out and the host may supply the checksum bytes. The output is then "as written".
Bit 2 D2	Rx Enable	**Set**: D2 enables the receiver for operation. No data is produced (i.e. No Rx Data Ready interrupts) until a 'SYNC' or 'SYNT' word is found in the received bit stream. **Clear**: The receiver is disabled and all interrupts caused by the receiver are inhibited.
Bit 3 D3	Rx Message Format	**Set**: D3 is sampled after a checksum has been received and allows the host to control the way the receiver handles the following data bits. If 'set' the receiver will assume that the next 6 bytes are data and will start error checking accordingly. **Clear**: The receiver will stop data transfer to the host after the 2 checksum bytes until another 'SYNC' or 'SYNT' frame word is received.
Bit 4 D4	Timer LSB	Reference Table 5
Bit 5 D5	Timer	
Bit 6 D6	Timer	
Bit 7 D7	Timer MSB	If a new timer value is written to these inputs within 1 byte period of the last timer interrupt then the next timer period will be correct without first having to reset the timer, otherwise the timer must be reset to zero and then set to the new time.
Tx Enable		If using the internal Tx preamble generation facility, e.g. with the internal timer setting the preamble length, the device may occasionally produce a Tx Ready interrupt immediately after a Tx Enable command. User software should handle this occurrence by either: a. Detecting that the timer interrupt status bit is not set and that it is not appropriate to load Tx data at this time. b. Not using the timer. i.e. immediately after Tx Enable, reading the Status Register and loading a byte of preamble. This resets any interrupt. The length of preamble transmitted is now controlled by the number of bytes loaded.

Table 4: Control Register

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

D7	D6	D5	D4	Reset counter and disable timer interrupts				
0	0	0	0	Count and interrupt every				
0	0	0	1	"	"	"	8	bits
0	0	1	0	"	"	"	16	bits
0	0	1	1	"	"	"	24	bits
0	1	0	0	"	"	"	32	bits
0	1	0	1	"	"	"	40	bits
0	1	1	0	"	"	"	48	bits
0	1	1	1	"	"	"	56	bits
1	0	0	0	"	"	"	64	bits
1	0	0	1	"	"	"	72	bits
1	0	1	0	"	"	"	80	bits
1	0	1	1	"	"	"	88	bits
1	1	0	0	"	"	"	96	bits
1	1	0	1	"	"	"	104	bits
1	1	1	0	"	"	"	112	bits
1	1	1	1	"	"	"	120	bits

Table 5: Timer Control Bits

4.1.5 Status Register (A1 = 1, A0 = 1, R/$\overline{W}$ = 1, Read Only)

When an interrupt is generated, the $\overline{IRQ}$ Output goes low with the Status Register bits indicating the sources of the interrupt.

Bit	Description	Function
Bit 0 D0	Rx Data Ready	**D0**: when set, causes an interrupt indicating that received data is ready to be read from the Rx Data Buffer. This data must be read within 8 bit periods. **Set** when a byte of data is loaded into the Rx Data Buffer, if a frame (SYNC/SYNT) word has been received. **Bit and Interrupt Cleared**: (i). by a read of the Status Register followed by a read of the Rx Data Buffer (ii). by Rx Enable going Low.
Bit 1 D1	Rx Checksum True	**D1**: when set, indicates that the error checking on the previous 6 bytes agreed with the received checksum. This function, which is valid when the Rx Data Ready bit (D0) is set for the second byte of the received checksum, does not cause an interrupt. **Set**: by a correct comparison between the received and generated checksums. **Cleared**: (i). by a read of the Status Register followed by a read of the Rx Data Buffer (ii). by Rx Enable going Low.
Bit 2 D2	Rx Carrier Detect	**D2**: is a "Real Time" indication from the modem receiver's carrier detect circuit and does not cause an interrupt. When FFSK tones are present at the receiver input this bit goes High, for no FFSK input this bit goes Low. When the Rx Enable bit (D2– Control Register) is Low Rx Carrier Detect will go Low.
Bit 3 D3	Tx Data Ready	D3: when set, causes an interrupt to indicate that a byte of data should be written to the Tx Data Buffer within 8 bit periods. **Set**: (i). when the contents of the Tx Data Buffer are transferred to the Tx Data Register (ii). when the Tx Enable is set (No interrupt is generated in this case. **Bit Cleared**: (i). by a read of the Status Register followed by a write to the Tx Data Buffer (ii). by Tx Enable going Low. **Interrupt Cleared**: (i). by a read of the Status Register (ii). by Tx Enable going Low.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Bit 4 D4	Tx Idle	**D4**: causes an interrupt when set, to indicate that all loaded data and one 'hang' bit have been transmitted. **Set**: one bit period after the last byte is transmitted. This last byte could be either "checksum" or " loaded data" depending upon the Tx Parity Enable state (Control Register D1). **Bit Cleared**: (i). by a write to the Tx Data Buffer (ii). by Tx Enable going Low. **Interrupt Cleared**: (i). by a read of the Status Register (ii). by Tx Enable going Low.
Bit 5 D5	Timer Interrupt	**D4**: causes an interrupt when set, to indicate that all loaded data and one 'hang' bit have been transmitted. **Set**: one bit period after the last byte is transmitted. This last byte could be either "checksum" or " loaded data" depending upon the Tx Parity Enable state (Control Register D1). **Bit Cleared**: (i). by a write to the Tx Data Buffer (ii). by Tx Enable going Low **Interrupt Cleared**: (i). by a read of the Status Registe (ii). by Tx Enable going Low.
Bit 6 D6	Rx SYNC Detect *	**D6**: when set, causes an interrupt to indicate that a 16-bit 'SYNC' word (1100010011010111) has been detected in the received bit stream. **Set**: on receipt of the 16th bit of a 'SYNC' word. **Bit and Interrupt Cleared**: (i). by a read of the Status Register (ii). by Rx Enable going Low.
Bit 7 D7	Rx SYNT Detect *	**D7**: when set, causes an interrupt to indicate that a 16-bit 'SYNT' word (0011101100101000) has been detected in the received bit stream. **Set**: on receipt of the 16th bit of a 'SYNT' word. **Bit and Interrupt Cleared**: (i). by a read of the Status Register (ii). by Rx Enable going Low.

* SYNC and SYNT Detection is disabled while the checksum checker is running.

Table 6: Status Register

4.1.6 Rx Data Buffer (A1 = 1, A0 = 0, R/$\overline{W}$ = 1, Read Only)

These 8 bits are the last byte of data received with bit 7 being received first. Note the relative positions of the MSB and LSB presented in this bit stream, the position may be different to the convention used in other µProcessor peripherals.

D0 LSB	D1	D2	D3	D4	D5	D6	D7 MSB

4.1.7 Tx Data Buffer (A1 = 1, A0 = 0, R/$\overline{W}$ = 0, Write Only)

These 8 bits loaded to the Tx Data Buffer are the next byte of data that will be transmitted, with bit 7 being transmitted first. Note the relative positions of the MSB and LSB presented in this bit stream, the position may be different to the convention used in other µProcessor peripherals. If the Tx Parity Enable bit(Control Register D1) is set, a 2–byte checksum will be inserted and transmitted by the modem after every 6 transmitted "message" bytes.

D0 LSB	D1	D2	D3	D4	D5	D6	D7 MSB

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.2 Syndrome Word

This 16-bit word (both Low and High bytes) may be used to correct errors. Bits S1 to S15 are the 15 bits remaining in the polynomial divider of the checksum checker at the end of 6 bytes of " received message." For a correct message all 15 bits (S1 to S15) will be zero. The 2 Syndrome bytes are valid when the Rx Data Ready bit (Status Register D0) is set for the second byte of the received checksum and should be read, if required, before 8 byte periods.

4.2.1 Syndrome Low Byte (A1 = 0, A0 = 0, R/$\overline{W}$ = 1, Read Only)

D0	D1	D2	D3	D4	D5	D6	D7
S1	S2	S3	S4	S5	S6	S7	S8

4.2.2 Syndrome High Byte (A1 = 0, A0 = 1, R/$\overline{W}$ = 1, Read Only)

D0	D1	D2	D3	D4	D5	D6	D7
S9	S10	S11	S12	S13	S14	S15	Parity Error

D7: This is a "Parity Error Bit". Indicating an error between the received parity bit and the parity bit internally generated from the incoming message. Therefore a correctly received message all 16 bits of the Syndrome Word (S1 to S15 and Parity Error) will be zero.

4.3 Carrier Detect Time Constant

The value of the Carrier Detect capacitor, C5, determines the carrier detect time constant. A long time constant (larger value C5), results in improved noise immunity but increased response time. C5 may be varied to optimize noise immunity/response time.

1. With R2 = 1MΩ and C5 = 1µF as external components for the carrier detect function at 1200 baud only.
2. By using C5 = 0.1µF and removing R2 completely the MX429A will operate at both 1200 and 2400 baud rates.

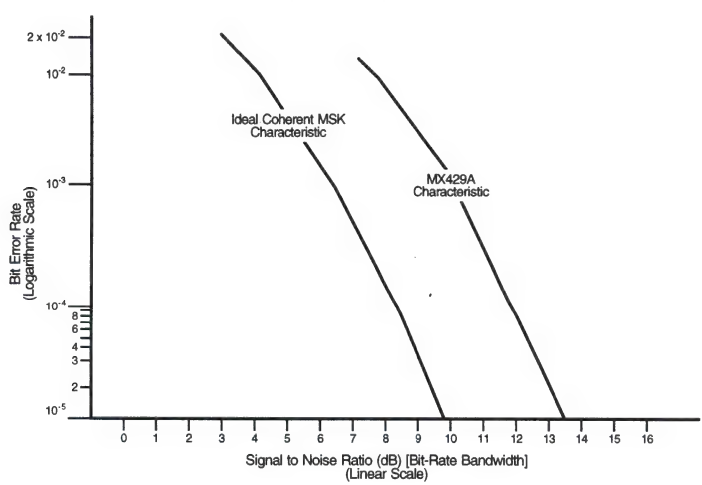


Figure 4: Bit Error Rate vs. Signal to Noise Ratio

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. Application

5.1 Checksum Generation and Checking

Generation – The checksum generator takes the 48 bits from the 6 bytes loaded into the Tx Data Buffer and divides them modulo–2, by the generating polynomial;-

$$X15 + X14 + X13 + X11 + X4 + X2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted). This 16–bit word is used as the "Checksum."

Checking – The checksum checker does two things:

It takes the first 63 bits of a received message, inverts bit 63, and divides them modulo–2, by the generating polynomial;-

$$X15 + X14 + X13 + X11 + X4 + X2 + 1$$

The 15 bits remaining in the polynomial divider are checked for all zero. Secondly, it generates an EVEN parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64). If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the Rx Checksum True bit (SR D1) bit is set.

5.2 Receive Operation

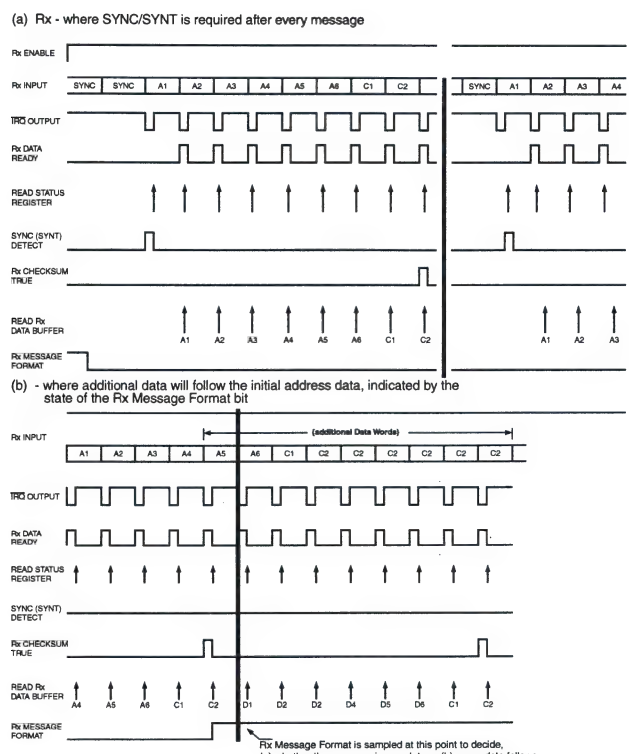


Figure 5: Receive Operation

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.3 Transmit Operation

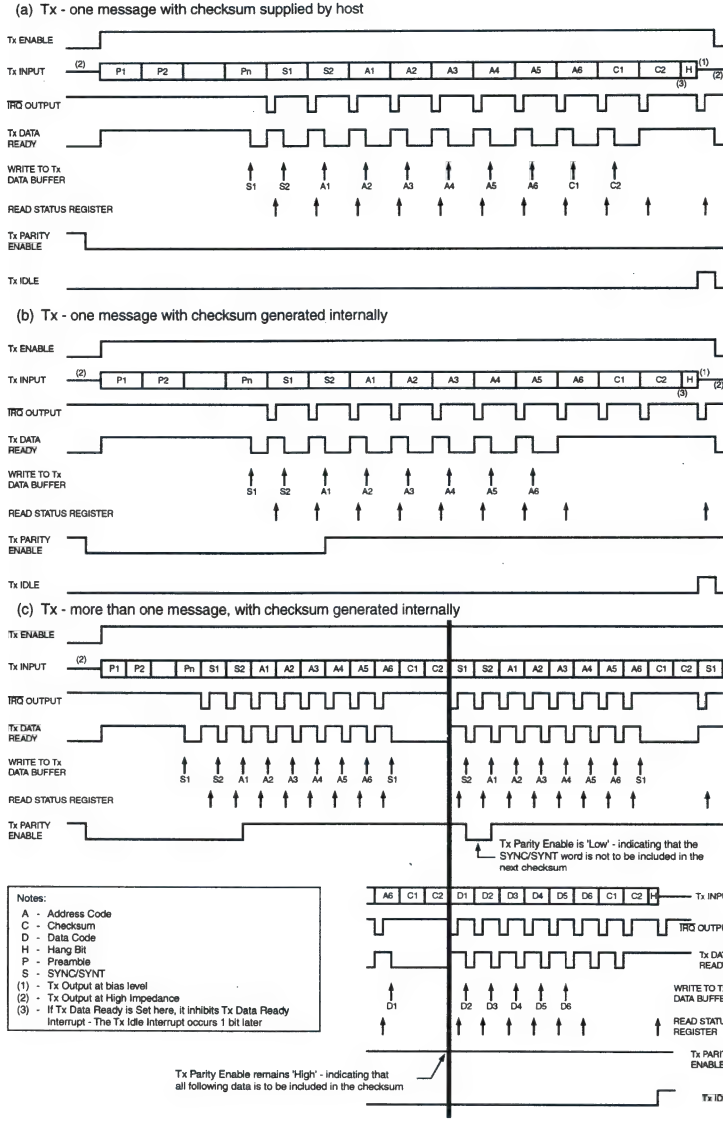

(a) Tx - one message with checksum supplied by host
Tx ENABLE
Tx INPUT
P1 P2 Pn S1 S2 A1 A2 A3 A4 A5 A6 C1 C2 H
IRQ OUTPUT
Tx DATA READY
WRITE TO Tx DATA BUFFER
READ STATUS REGISTER
Tx PARITY ENABLE
Tx IDLE
(b) Tx - one message with checksum generated internally
(c) Tx - more than one message, with checksum generated internally
Tx Parity Enable is 'Low' - indicating that the SYNC/SYNT word is not to be included in the next checksum
Tx Parity Enable remains 'High' - indicating that all following data is to be included in the checksum
Notes:
A - Address Code
C - Checksum
D - Data Code
H - Hang Bit
P - Preamble
S - SYNC/SYNT
(1) - Tx Output at bias level
(2) - Tx Output at High Impedance
(3) - If Tx Data Ready is Set here, it inhibits Tx Data Ready Interrupt - The Tx Idle Interrupt occurs 1 bit later

Figure 6: Transmit Operation

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.4 Basic Power Up Software

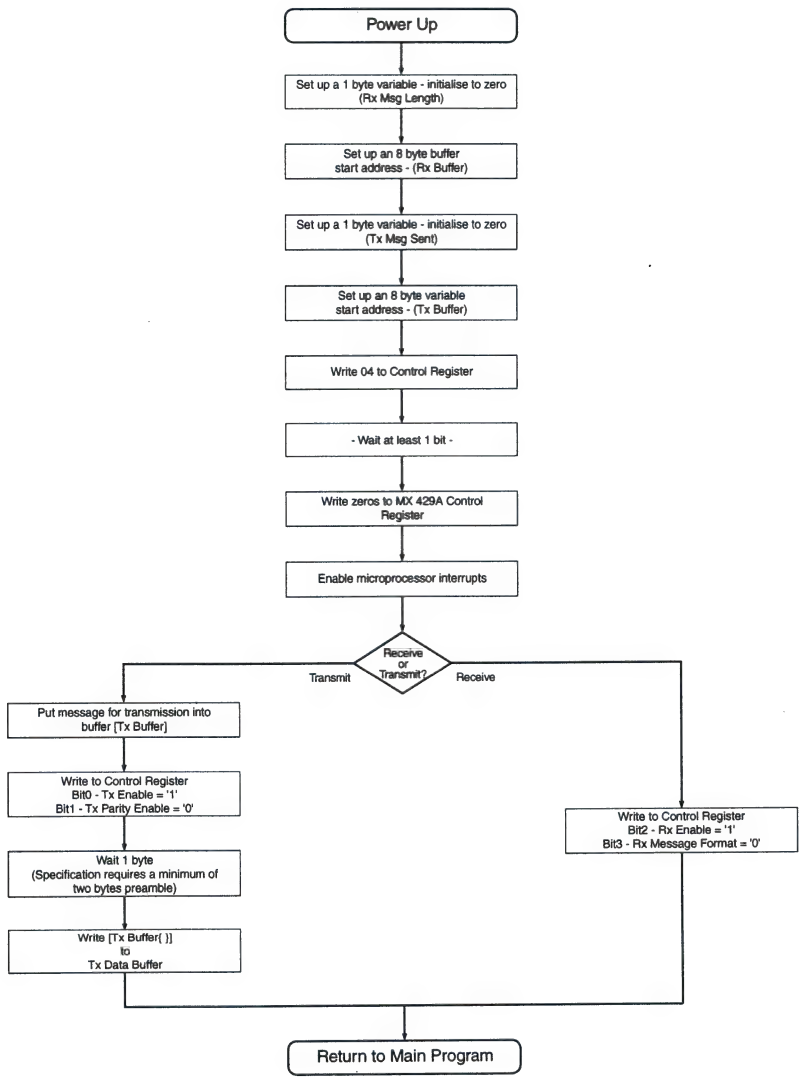

Power Up
Set up a 1 byte variable - initialise to zero (Rx Msg Length)
Set up an 8 byte buffer start address - (Rx Buffer)
Set up a 1 byte variable - initialise to zero (Tx Msg Sent)
Set up an 8 byte variable start address - (Tx Buffer)
Write 04 to Control Register
- Wait at least 1 bit -
Write zeros to MX 429A Control Register
Enable microprocessor interrupts
Receive or Transmit?
Transmit
Receive
Put message for transmission into buffer (Tx Buffer)
Write to Control Register Bit0 - Tx Enable = '1' Bit1 - Tx Parity Enable = '0'
Wait 1 byte (Specification requires a minimum of two bytes preamble)
Write [Tx Buffer( )] to Tx Data Buffer
Write to Control Register Bit2 - Rx Enable = '1' Bit3 - Rx Message Format = '0'
Return to Main Program

Figure 7: Basic Power-Up Software

© 1997 MX-COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.5 Basic Software Interrupt Flow

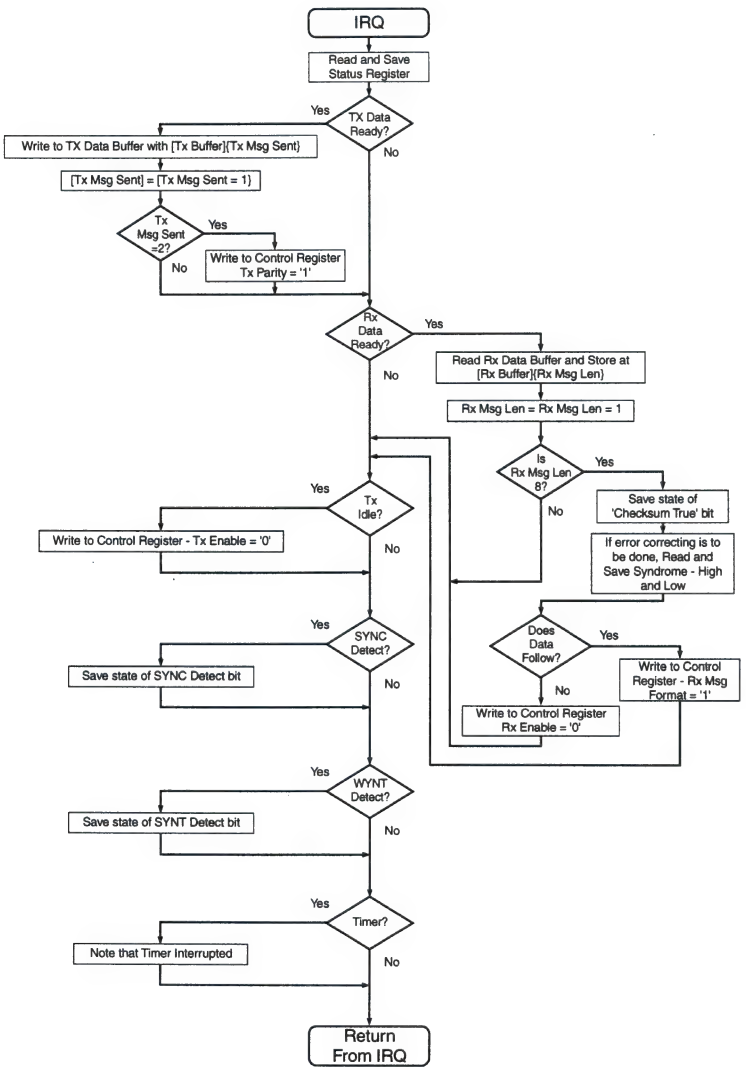


Figure 8: Basic Software Interrupt Flow

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
J / P / LH Package					
Total allowable Power Dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			10		mW/°C above °C
Operating Temperature		-30		85	°C
Storage Temperature		-55		125	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-30		85	°C
Xtal Frequency			4.032		MHz

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C, Xtal/Clock f_0 = 4.032MHz
Bit Rate Bandwidth = 1200Hz, Audio Level 0dB ref: = 300mV_{RMS}

Static Values	Notes	Min.	Typ.	Max.	Units
Supply Current Ranges					
Rx and Tx Enabled				7.0	mA
Rx Enabled, Tx Disabled			4.0	6.0	mA
Rx Disabled, Tx Enabled				7.0	mA
Rx and Tx Disabled			1.5	2.5	mA
Dynamic Values					
Modem Internal Delay			1.5		ms
Interface Levels					
Output Logic '1' Source Current	2			120	µA
Output Logic '0' Sink Current	3			360	µA
Three State Output Leakage Current				4.0	µA

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

D0 – D7 Data In/Out		1				
Logic '1' Level			3.5			V
Logic '0' Level					1.5	V
A1, A0, R/W, STROBE, IRQ 4						
Logic '1' Level			4.0			V
Logic '0' Level					1.0	V
Analogue Impedances						
Rx Input			100			kΩ
Tx Output (Enabled)				10		kΩ
Tx Output (Disabled)				5.0		MΩ
On-Chip Xtal Oscillator						
RIN			10.0			MΩ
ROUT		5		30.0		kΩ
Oscillator Gain				25.0		dB
Xtal frequency				4.032		MHz
Receiver						
Signal Input Levels		6	–9.0	–2.0	10.5	dB
Bit Error Rate		7				
@ 12dB Signal/Noise Ratio				7.0		10^{-4}
@ 20dB Signal/Noise Ratio				1.0		10^{-8}
Synchronization @ 12dB Signal/Noise Ratio		8				
Probability of Bit 16 being correct				99.5		%
Carrier Detect Response Time		8		13.0		ms
Transmitter						
Output Level				8.25		dB
Output Level Variation			-1.0		1.0	dB
Output Distortion				3.0	5.0	%
3rd Harmonic Distortion				2.0	3.0	%
Logic '1' Frequency	1200 baud	9		1200		Hz
	2400 baud	9		1200		Hz
Logic '0' Frequency	1200 baud	9		1800		Hz
	2400 baud	9		2400		Hz
Isochronous Distortion						
1200Hz – 1800Hz/1200Hz - 2400Hz			25	40	µs	
1800Hz – 1200Hz/2400Hz - 1200Hz			20	40	µs	

Operating Characteristics Notes:

1. With each data line loaded as, C = 50pf and R = 10kΩ.
2. V_{OUT} = 4.6V.
3. V_{OUT} = 0.4V
4. Sink/Source currents - 0.1mA.
5. Both Xtal and Xtal " 4 Outputs.
6. With 50dB Signal/Noise Ratio.
7. See Figure 4, Bit Error Rate.
8. This Response Time is measured using a 10101010101....01 pattern input signal at a level of 230mV_{RMS} (-2.3dB) with no noise.
9. Dependent upon Xtal tolerance.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.1.1 Timing

Timing see Figure 9		Min.	Typ.	Max.	Units
(t_{ACS})	Access Time			135	ns
(t_{AH})	Address Hold Time	0			ns
(t_{AS})	Address Set-up Time	0			ns
(t_{DHW})	Data Hold Time (Write)	85			ns
(t_{DS})	Data Set-up Time (Write)	0			ns
(t_{OHR})	Output Hold Time (Read)	15		105	ns
(t_{ST})	Strobe Time			140	ns

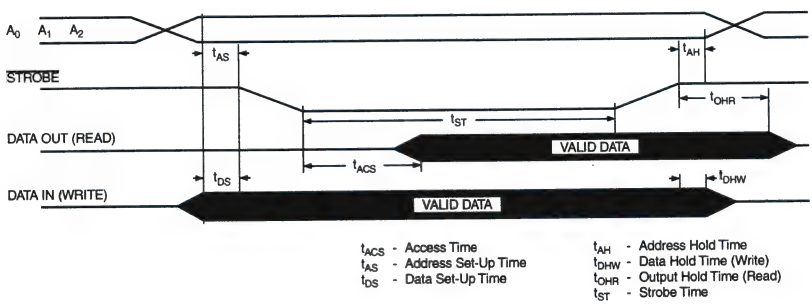
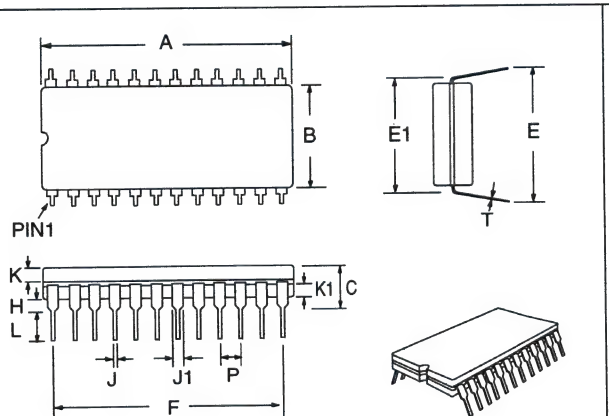


Figure 9: Timing Diagram

6.2 Packaging



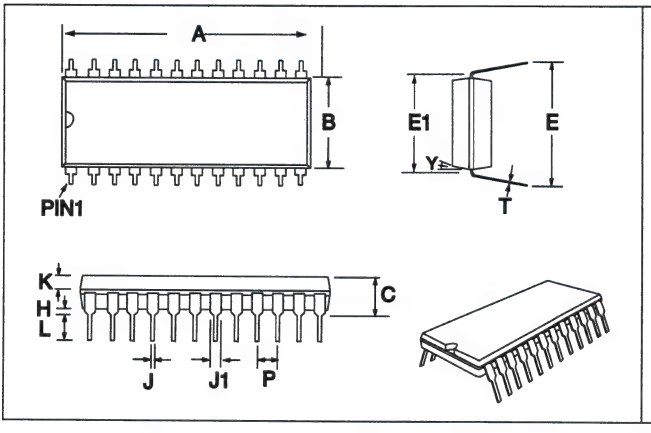
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Figure 10: 24-pin CDIP Mechanical Outline: *order as part no. MX429AJ*

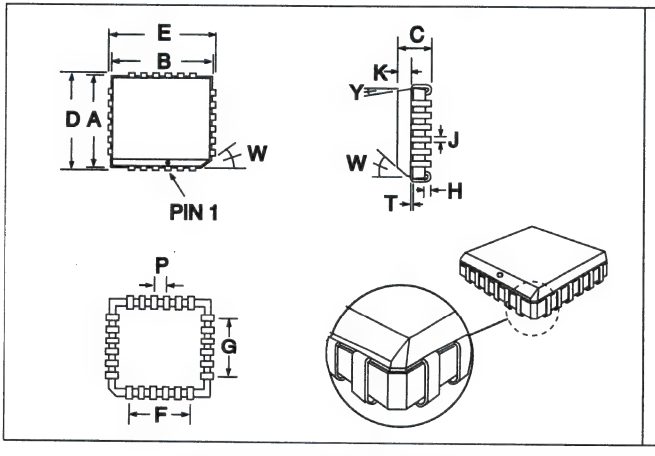


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 24-pin PDIP Mechanical Outline: *order as part no. MX429AP*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 12: 24-pin PLCC Mechanical Outline: *order as part no. MX429ALH*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480128.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

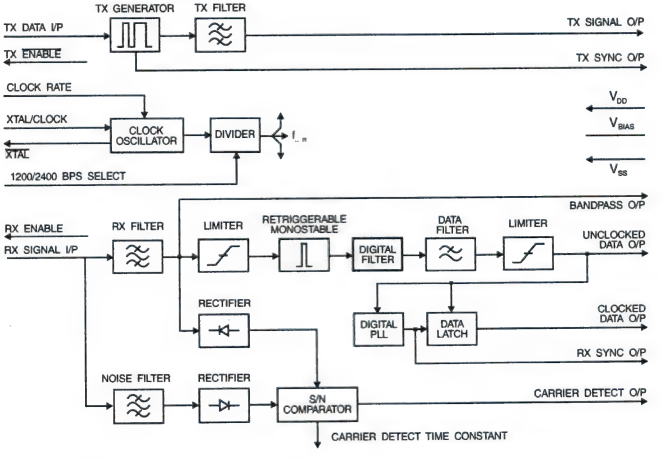
MX469 1200/2400bps MSK Modem

Features

- **Selectable Data Rates**
  1200 and 2400 bps
- **Full-Duplex MSK**
- **RX and TX Bandpass Filters**
- **Clock Recovery and Carrier Detect Capabilities**
- **Pin Selected Xtal/Clock Inputs**
  1.008MHz or 4.032MHz

Applications

- **Radio and General Applications**
- **Data-Over-Radio**
- **PMR/Cellular Signaling**
- **Portable Data Terminals**
- **Personal/Cordless Telephone**



The MX469 is a full-duplex pin-selectable 1200 or 2400 bps Minimum Shift Key (MSK) Modem for FM radio links. The mark and space frequencies are 1200/1800 and 1200/2400Hz respectively. Tone frequencies are phase continuous; transitions occur at the zero crossing point. The use of a common Xtal oscillator with a choice of two clock frequencies (1.008MHz or 4.032MHz) provides data-rate, transmit frequencies, and RX/TX synchronization. The transmitter and receiver operate entirely independently including individual section powersave functions.

The MX469 includes on-chip circuitry for Carrier Detect and RX Clock Recovery, both of which are made available at output pins. RX, TX and Carrier Detect paths each contain a bandpass filter to make sure you get the best quality signal in the Modem and TX modulation circuitry. The carrier detect time constant is set by an external capacitor, whose value should be arranged as required to further enhance this product's performance in high-noise environments.

The MX469 demonstrates a high sensitivity and good bit-error-rate even under adverse signal conditions.

This low-power device requires few external components and is available in the following packages: 24-pin SOIC (MX469DW), 22-pin CDIP (MX469J), 22-pin PDIP (MX469P) and 24-pin PLCC (MX469LH).

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480081.007
All trademarks and service marks are held by their respective companies.

Contents

Section **Page**

1. Block Diagram 1-23

2. Signal List 1-24

3. External Components 1-26

4. General Description 1-27

4.1 Timing 1-27

4.1.1 1200bps 1-27

4.1.2 2400bps 1-28

5. Application 1-29

5.1 Synchronous Modem Design Considerations 1-29

5.2 Bit Error Rate 1-30

6. Performance Specifications 1-32

6.1 Electrical Specifications 1-32

6.1.1 Absolute Maximum Limits 1-32

6.1.2 Operating Limits 1-32

6.1.3 Operating Characteristics 1-33

6.1.4 Packages 1-35

MXCOM, Inc. reserves the right to change specifications at any time without notice.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1. Block Diagram

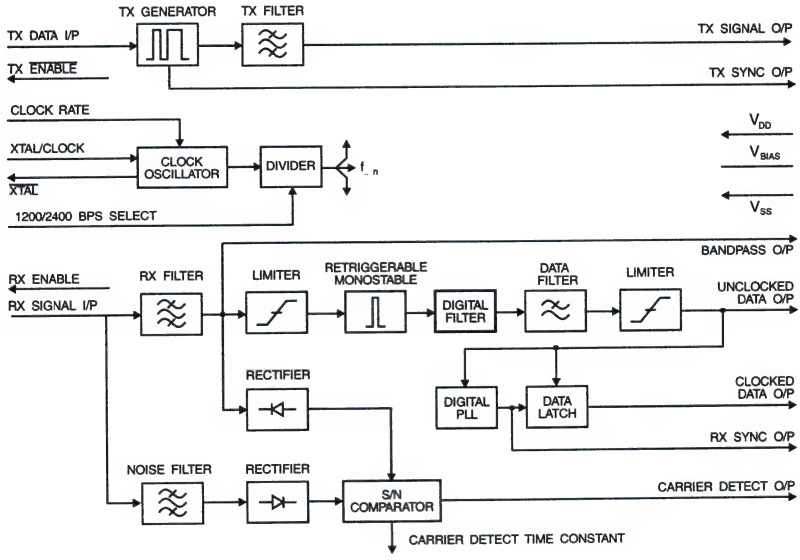


Figure 1: Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. Signal List

Pin No.			Signal	Type	Description
DW	J/P	LH			
1	1	1	Xtal/Clock	output	The input to the on-chip inverter, for use with either a 1.008MHz or a 4.032MHz Xtal or external clock. Clock frequency selection is by the "Clock Rate" input pin. The selection of this frequency will affect the operational Data Rate of this device. Refer to 1200/2400 BPS Selection information on the next page. Operation of any MX•COM IC without a Xtal or clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, it is recommended that a current limiting device (resistor or fast-reaction fuse) be installed on the power supply (V_{DD}).
2	2	2	Xtal		Output of the on-chip inverter.
3	3	3	TX Sync	output	A squarewave, produced on-chip, to synchronize the input of logic data and transmission of the MSK signal (See Figure 3).
5	5	5	TX Signal	output	When the transmitter is enabled, this pin outputs the (140-step pseudo sinewave) MSK signal (See Figure 3). With the transmitter disabled, this output is set to a high-impedance state.
7	6	7	TX Data	input	Serial logic data to be transmitted is input to this pin.
8	7	8	TX Enable		A logic '0' will enable the transmitter (See Figure 3). A logic '1' at this input will put the transmitter into powersave while forcing "TX Sync Out" to a logic '1' and "TX Signal Out" to a high-impedance state. This pin is internally pulled to V_{DD}.
9	8	9	Bandpass	output	The output of the RX Bandpass Filter. This output impedance is typically 10kΩ and may require buffering prior to use.
10	9	10	RX Enable		The control of the RX function. The control of other outputs is provided in Table 2
11	10	11	V_{BIAS}	power	The output of the on-chip analog bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} by a capacitor (C2). See Figure 2 and RX Enable notes. This bias voltage is maintained under all powersave conditions.
12	11	12	V_{SS}	power	Negative supply (GND).
13	12	13	Unclocked Data	output	The recovered asynchronous serial data output from the receiver.
14	13	14	Clocked Data	output	The recovered synchronous serial data output from the receiver. Data is latched out by the recovered clock, available at the "RX Sync O/P", (See Figure 4 and Figure 6).
15	14	15	Carrier Detect	output	When an MSK signal is being received this output is a logic '1'.
16	15	16	RX Signal	input	The MSK signal input for the receiver. This input should be coupled via a capacitor, C3.
18	17	18	RX Sync	output	A flywheel squarewave output. This clock will synchronize to incoming RX MSK data. (See Figure 4 and Figure 6).
19	16	19	1200/2400 BPS Select		A logic '1' on this pin selects the 1200 bps option. Tone frequencies are: one cycle of 1200Hz represents a logic '1', one-and-a-half cycles of 1800Hz represents a logic '0'. A logic '0' on this pin selects the 2400 bps option. Tone frequencies are: one-half cycle of 1200Hz represents a logic '1', one cycle of 2400Hz represents a logic '0'. This pin has an internal 1MΩ pullup resistor. Operational Data Rate Configurations are illustrated in table.
20	18	20			Internally connected, leave open circuit.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

21	19	21	Clock Rate		A logic input to select and allow the use of either a 1.008MHz or 4.032MHz Xtal/clock. Logic '1' = 4.032MHz, logic '0' = 1.008MHz. This input has an internal pulldown resistor (1.008MHz).
23	20	23	Carrier Detect Time Constant		Part of the carrier detect integration function. The value of C4 connected to this pin will affect the carrier detect response time and therefore the noise performance (See Figure 2, Note 3).
24	22	24	V_{DD}	power	Positive supply. A single 5-volt supply is required.
4, 6, 17, 22	4, 21	4, 6, 17, 22	N/C		No internal connection.

Table 1: Signal List

RX Enable	=	RX Function	Clock Data Output	Carrier Detect	Rx Sync Out
1	=	Enabled	Enable	Enabled	Enabled
0	=	Powersave	0	0	1 or 0

Table 2: RX Enable Control Functions

XTAL/CLOCK Frequency	1.008MHz		4.032MHz	
Clock Rate pin	0	0	1	1
1200/2400 Select Pin	1	0	1	0
Data Rate (bps)	1200	2400	1200	2400

Table 3: Operational Data Rate Configuration

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components

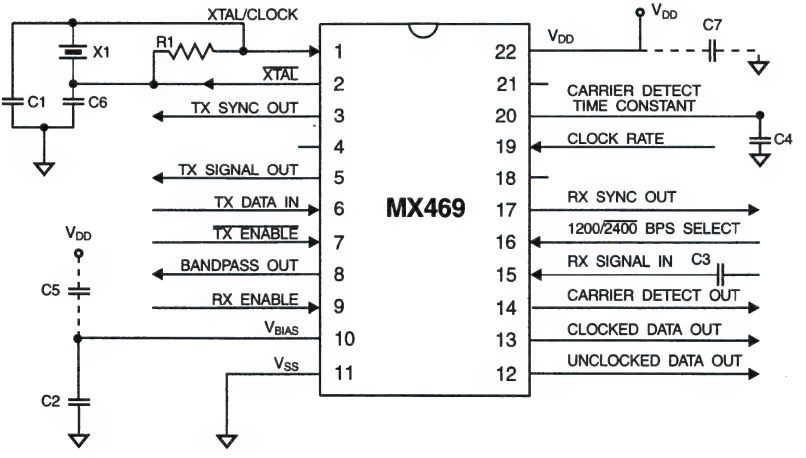


Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1		1.0MΩ	±10%
C1		33pF	±5%
C2		1.0µF	±20%
C3		0.1µF	±20%
C4	Note 1	0.1µF	±10%
C5	Note 2	1.0µF	±25%
C6	Note 3	33pF	±5%
C7	Note 2	1.0µF	±20%
X1	Note 4	1.008MHz or 4.032MHz	See 'Clock-Rate' Pin

Table 4: Recommended External Components

Notes:

1. The value of C4 determines the Carrier Detect time constant. A long time constant results in improved noise immunity but increased response time. C4 may be varied to trade-off response time for noise immunity.
2. Decoupling circuits depend upon whether the input signal is referenced to V_{BIAS} or V_{SS}. Use C5 when the input signal is referenced to V_{BIAS}. Use C7 when the input signal is referenced to V_{SS}. It is not necessary to use both C5 and C7.
3. C6 reduces Xtal voltage overshoot. Reference the MX•COM Xtal Application Note.
4. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4. General Description

4.1 Timing

4.1.1 1200bps

Characteristics		Note	Min.	Typ.	Max.	Unit
TX Enable to TX Sync Rise Time	t_{SYNC}			416		µs
TX Delay, Signal to Disable Time	t_{ESET}		2.0		800	µs
Data Set-Up Time	t_{DSET}	1	2.0			µs
Data Hold Time	t_{DH}		2.0			µs
TX Delay to O/P Time	t_{TxD}			1.2		µs
TX Data Rate Period	t_{TDR}			833		µs
RX Data Rate Period	t_{RDR}		800		865	µs
Undetermined State					2.0	µs
Internal RX Delay	t_{ID}			1.5		ms

Notes:

1. Consider the Xtal/clock tolerance.
2. All TX timings are related to the TX Sync Output.

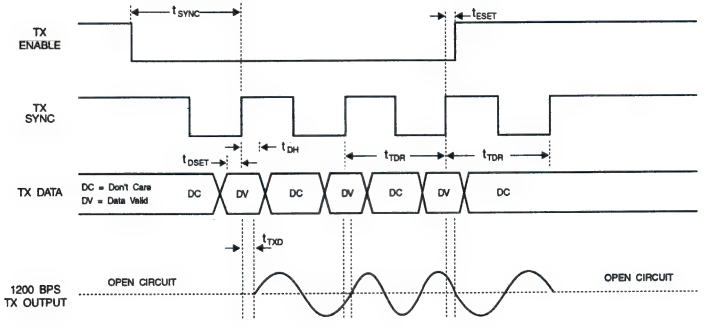


Figure 3: Transmitter Timing: 1200bps

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

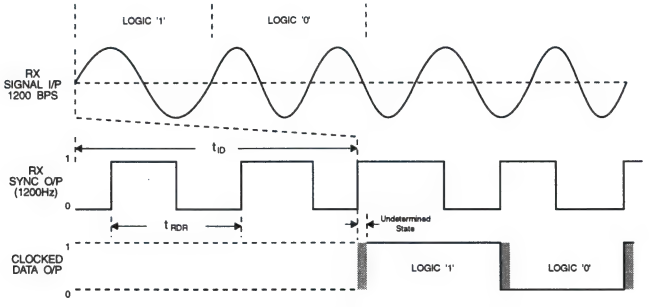


Figure 4: Receiver Timing Diagram: 1200bps

4.1.2 2400bps

Characteristics		Note	Min.	Typ.	Max.	Unit
TX Enable to TX Sync Rise Time	t_{SYNC}			208		µs
TX Delay, Signal to Disable Time	t_{ESET}		2.0		400	µs
Data Set-Up Time	t_{DSET}	1	2.0			µs
Data Hold Time	t_{DH}		2.0			µs
TX Delay to O/P Time	t_{TxD}			1.2		µs
TX Data Rate Period	t_{TDR}			416		µs
RX Data Rate Period	t_{RDR}		400		433	µs
Undetermined State					2.0	µs
Internal RX Delay	t_{ID}			1.5		ms

Notes:

1. Consider the Xtal/Clock tolerance.
2. All TX timings are related to the TX Sync Output.

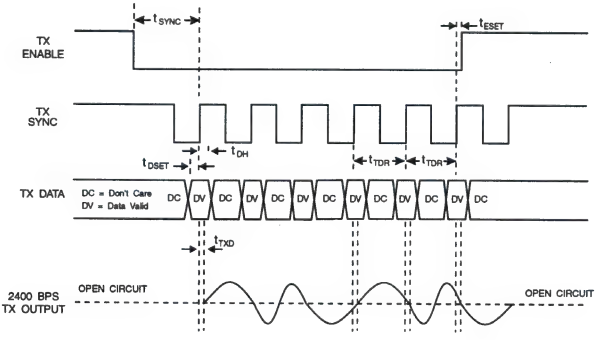


Figure 5: Transmitter Timing: 2400bps

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

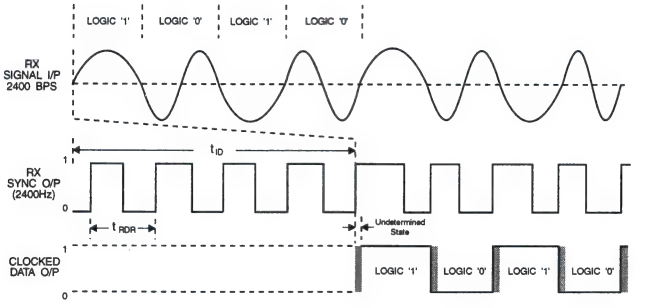


Figure 6: Receiver Timing: 2400bps

5. Application

5.1 Synchronous Modem Design Considerations

The MX469 is an easily applied data pump which can be used with many protocols. Because it is an MSK, or minimum shift keying, modem, it achieves a more noise resistant, higher data rate in a narrower bandwidth than other FSK (frequency shift keying) modems. This characteristic is especially important for wireless applications because it fundamentally determines the bandwidth of r.f. transmissions which are strictly limited and controlled by regulatory agencies. Using MSK signaling, the MX469 data modem can achieve a 2400 bps data rate within the typical 300-3000 Hz voice band of many common radios.

In order to achieve this advantage, an MSK modem must precisely control the bit rate and timing of the modulated Tx output signal bits. This control is asserted by the MSK modem with a data clock signal which is output by the modem to pace the Tx data source (e.g. a microcontroller). The data clock signal, in effect, indicates when the Tx data source should provide the next Tx data bit to the modem. See Figure 7. Because this type of interface involves the use of a modem generated bit clock signal to control the timing of when new Tx data bits must be supplied from the data source, the interface is called synchronous.

Another characteristic of a synchronous modem is that, to receive data, it must first learn the data bit timing of the Rx signal stream before it can accurately demodulate Rx data bits. Accordingly, a synchronous modem undergoes a period of training or synchronization when it first begins to receive a stream of MSK modulated signal. During this initial receive phase, the received signal is evaluated over several bit times as the modem 'locks on' and achieves proper receive synchronization. The training sequence, called a preamble, is a specific data pattern which must be added to the 'front' of a transmit data stream with the start of each new transmission. A specific preamble data pattern (e.g. 16 bits of alternating 0,1,0,1... for the MX469) is used to optimize the training accuracy while minimizing the number of preamble bits required.

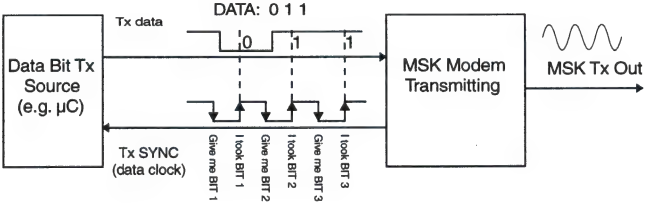


Figure 7: Synchronous Transmit Operation

Non-synchronous or asynchronous interfaces are commonly found in wired applications which do not have the bandwidth efficiency requirements of wireless systems. A well known example is the serial port of a personal computer which can transmit a 1200 bps (or faster) data signal over a single Tx signal without using an additional data clock signal to control the precise rate and timing of data bits being transmitted to a typical telephone line data modem. Popular modem standards such as Bell 202 and v.23 use FSK signaling to pass such asynchronous serial port data signals over telephone systems.

Another aspect of asynchronous interfaces and modems is that they can carry data streams which are not at the exact, nominal data rate. For example, a 1200 bps FSK modem will typically operate properly when supplied with transmit data streams of 1201 bps or 1199 bps.

Because of the differences in synchronous and asynchronous interfaces, they cannot successfully operate if directly connected. In other words, a personal computer's RS232 serial port cannot directly interface to an MSK modem. This is because:

- The asynchronous interface may provide data bits too fast or too slow compared to the precise rate required for MSK signaling (a bit rate, or pacing, incompatibility).
- The timing of each specific data bit presented by an asynchronous interface will not be aligned with the precise bit timing required for MSK signaling (a bit timing incompatibility).

Synchronous and asynchronous interface can be successfully interfaced for applications requiring the advantages of both. This typically involves the use of data buffering and retiming circuits to resolve the timing and pacing issues.

5.2 Bit Error Rate

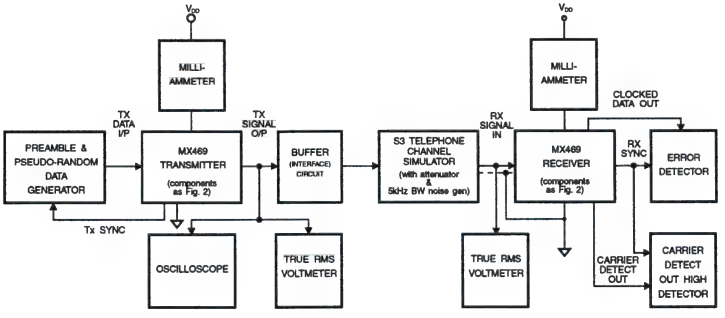


Figure 8: MX469 Test Set-Up

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

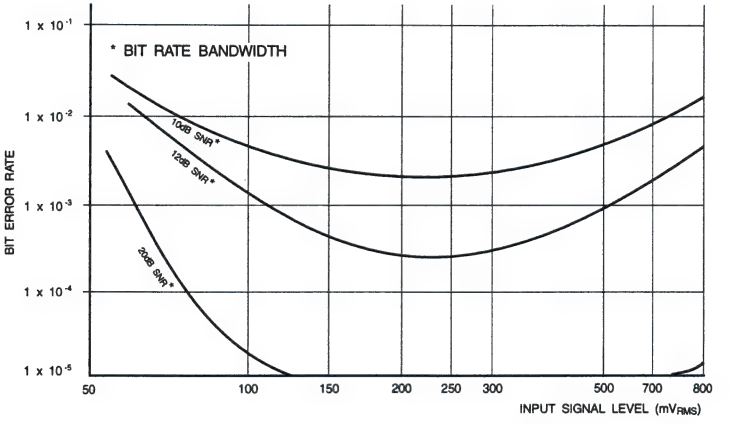


Figure 9: Typical Variation of Bit Error Rate with Input Level

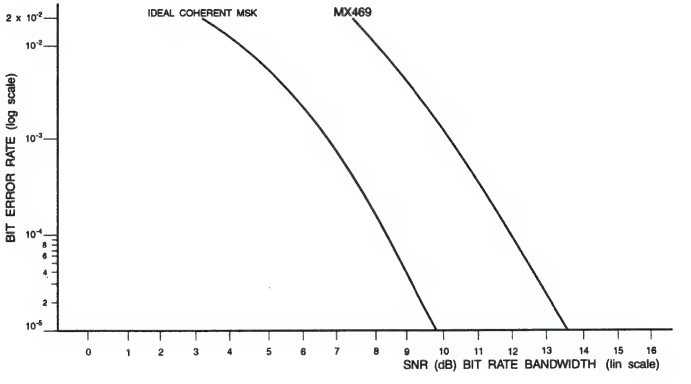


Figure 10: RX Bit-Error-Rate vs Signal-to-Noise Ratio

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6. Performance Specifications

6.1 Electrical Specifications

6.1.1 Absolute Maximum Limits

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
DW / LH / J / P Packages					
Total allowable Power dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			10		mW/°C above 25°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal Frequency		1.008		4.032	MHz

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified.

V_{DD} = 5.0V @ T_{AMB} = 25°C
Audio Level 0dB ref. = 300mV_{RMS}, Xtal/Clock Frequency = 4.032MHz
Signal-to-Noise Ratio measured in the Bit-Rate Bandwidth
1200bps BRB = 1200Hz
2400bps BRB = 2400Hz

Static Values	Notes	Min.	Typ.	Max.	Units
Supply Current			3.6		mA
RX Enabled, TX Disabled					
RX and TX Enabled			4.5		mA
RX and TX Disabled			650		µA
Logic '1' Level	1	4.0			V
Logic '0' Level	1			1.0	V
Digital Output Impedance			4.0		kW
Analog and Digital Input Impedance		100			kW
TX Output Impedance			10.0		kW
On-Chip Xtal Oscillator					
R_{IN}		10.0			MW
R_{OUT}			10.0		kW
Inverter d.c. Voltage Gain			10.0		V/V
Gain Bandwidth Product			10.0		MHz
Dynamic Values					
Receiver					
Signal Input Dynamic Range	3, 4	100	230	1000	mV_{RMS}
SNR = 50dB					
Bit Error Rate					
SNR = 12dB	4		7.0		10-4
SNR = 20dB	4		1.0		10-8
Receiver Synchronization **SNR =12dB**	7				
Probability of Bit 8 Being Correct			99		%
Probability of Bit 16 Being Correct			99.5		%
Carrier Detect			5		
Sensitivity	7, 8			150	mV_{RMS}
Probability of C.D. Being High					
After Bit 8 (1200 bps) SNR = 12dB	5, 9		98		%
After Bit 16 SNR = 12dB	5, 9		99.5		%
0dB Noise No Signal	9		5		%

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

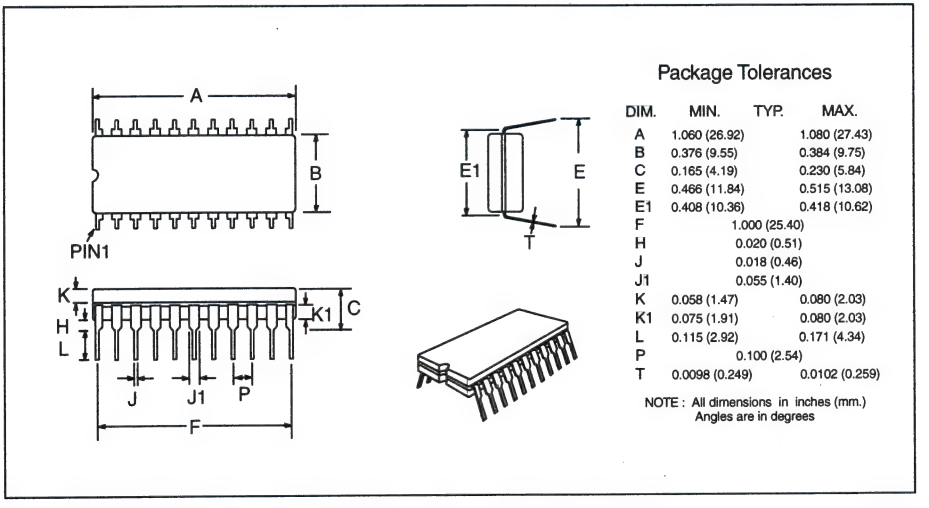
	Notes	Min.	Typ.	Max.	Units
Transmitter Output					
TX Output Level			775		mV_{RMS}
Output Level Variation					
1200/1800Hz or 1200/2400Hz		0		±1.0	dB
Output Distortion			3.0	5.0	%
3rd Harmonic Distortion			2.0	3.0	%
Logic '1' Carrier Frequency					
1200 bps	6		1200		Hz
2400 bps	6		1200		Hz
Logic '0' Carrier Frequency					
1200 bps	6		1800		Hz
2400 bps	6		2400		Hz
Isochronous Distortion					
1200Hz - 1800Hz/1200Hz - 2400Hz			25.0	40.0	µs
1800Hz - 1200Hz/2400Hz - 1200Hz			20.0	40.0	µs

Operating Characteristics Notes:

1. With reference to V_{DD} = 5.0 volts.
2. Xtal frequency (ref. Clock Rate pin), type and tolerance depends upon system requirements.
3. See Figure 4 (variation of BER with Input Signal Level).
4. SNR = Signal-to-Noise in the Bit-Rate Bandwidth.
5. See Figure 2.
6. Dependent upon Xtal tolerance.
7. 10101010101 ...01 pattern.
8. Measured with a 150mVrms input signal (no noise).
9. 9.Reference (0dB) level for C.D. probability measurements is 230mV_{RMS}.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.1.4 Packages

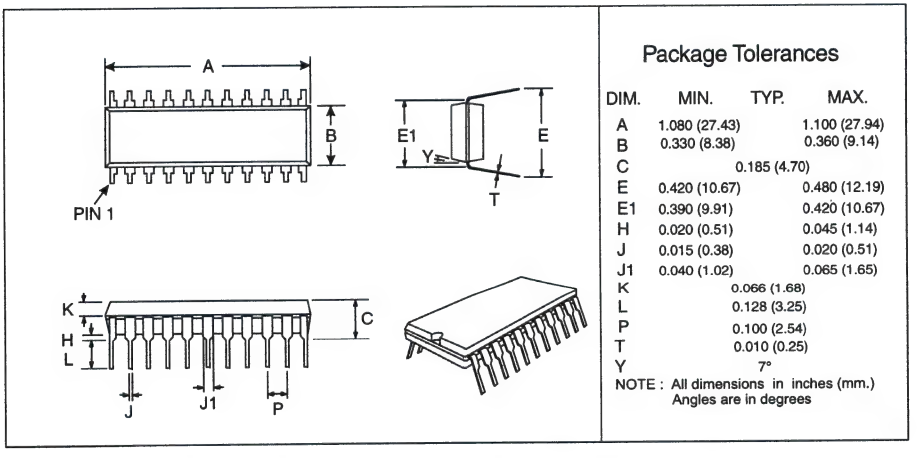


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.060 (26.92)		1.080 (27.43)
B	0.376 (9.55)		0.384 (9.75)
C	0.165 (4.19)		0.230 (5.84)
E	0.466 (11.84)		0.515 (13.08)
E1	0.408 (10.36)		0.418 (10.62)
F		1.000 (25.40)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.40)	
K	0.058 (1.47)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 22-pin CDIP Mechanical Outline: order as part no. MX469J



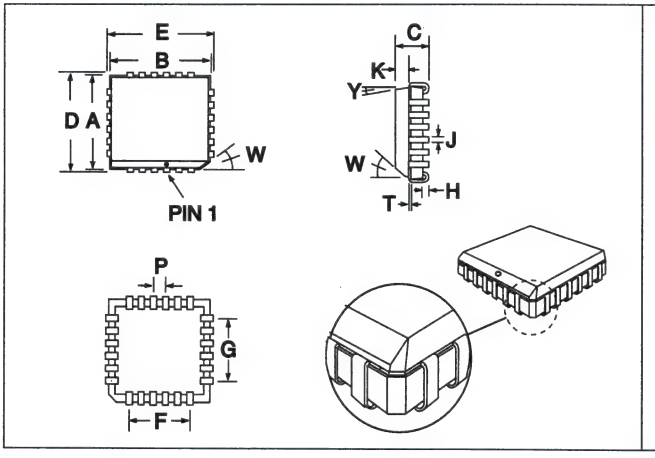
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.080 (27.43)		1.100 (27.94)
B	0.330 (8.38)		0.360 (9.14)
C		0.185 (4.70)	
E	0.420 (10.67)		0.480 (12.19)
E1	0.390 (9.91)		0.420 (10.67)
H	0.020 (0.51)		0.045 (1.14)
J	0.015 (0.38)		0.020 (0.51)
J1	0.040 (1.02)		0.065 (1.65)
K		0.066 (1.68)	
L		0.128 (3.25)	
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 12: 22-pin PDIP Mechanical Outline: order as part no. MX469P

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

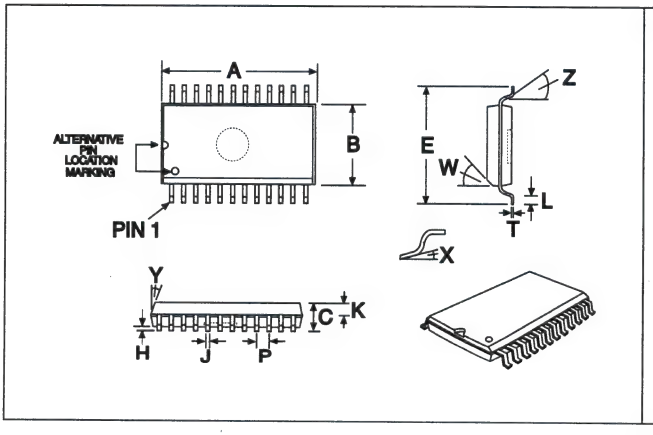


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 13: 24-pin PLCC Mechanical Outline: order as part no. MX469LH



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 14: 24-pin SOIC Mechanical Outline: order as part no. MX469DW

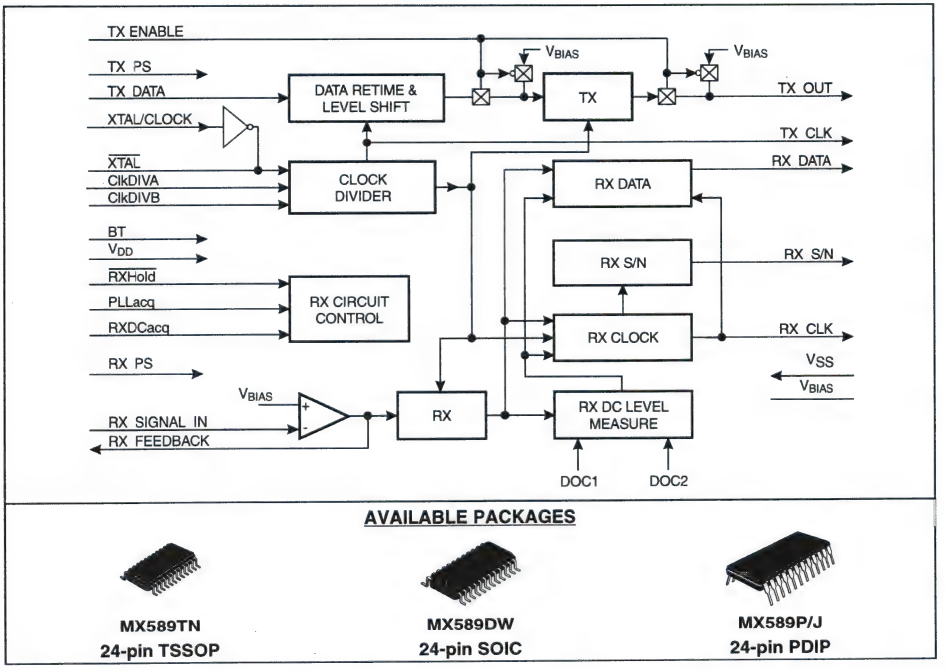
© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480081.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX589 High Speed GMSK Modem

- **Data Rates from 4kbps to 64kbps**
- **Full or Half Duplex Gaussian Minimum Shift Keying (GMSK) Operation**
- **Selectable BT: (0.3 or 0.5)**
- **Low Power:**
  3.0V, 32kbps, 1.5mA typ.
  5.0V, 64kbps, 4.0mA typ.
- **Low Cost**
- **Point of Sale Terminals**
- **Low Power Wireless Data Link for PCs, Laptops, and Printers**
- **Data for GPS/Differential GPS**
- **Portable Wireless Data Applications:**
  Cellular Digital Packet Data (CDPD)
  Mobitex™ Mobile Data System
- **Low Current Non-DSP Solution**



AVAILABLE PACKAGES

MX589TN
24-pin TSSOP

MX589DW
24-pin SOIC

MX589P/J
24-pin PDIP

The MX589 is a single-chip synchronous modem designed for wireless data applications. Employing Gaussian Minimum Shift Keying (GMSK) baseband modulation, the MX589 features a wide range of available data rates: 4kbps to 64kbps.

Data rates and choice of BT (0.3 or 0.5) are pin-programmable to provide for different system requirements.

The Tx and Rx digital data interfaces are bit serial, synchronized to Tx and Rx data clocks generated by the modem. Separate Tx and Rx Powersave inputs allow full or half-duplex operation. Rx input levels can be set by a suitable AC and DC level adjusting circuit built with external components around an on-chip Rx Input Amplifier.

Acquisition, lock and hold of Rx data signals are made easier and faster by the use of Rx Control Inputs to clamp, detect and/or hold input data levels and can be set by the µProcessor as required. The Rx S/N output provides an indication of the quality of the received signal.

All trademarks and service marks are held by there respective companies.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480103.009

Contents

Section **Page**

1. Block Diagram **1-39**

2. Signal List **1-40**

3. External Components **1-41**

4. General Description **1-42**

4.1 Clock Oscillator Divider 1-42
4.2 Receive 1-43
4.3 Transmit 1-47
4.4 Data Formats 1-49
4.5 Acquisition and Hold Modes 1-49

5. Application **1-49**

5.1 Radio Channel Requirements 1-49
5.2 AC Coupling of Tx and Rx Signals 1-51

6. Performance Specifications **1-52**

6.1 Electrical Performance 1-52
6.2 Packaging 1-55

MXCOM, Inc. reserves the right to change specifications at any time without notice.

1. Block Diagram

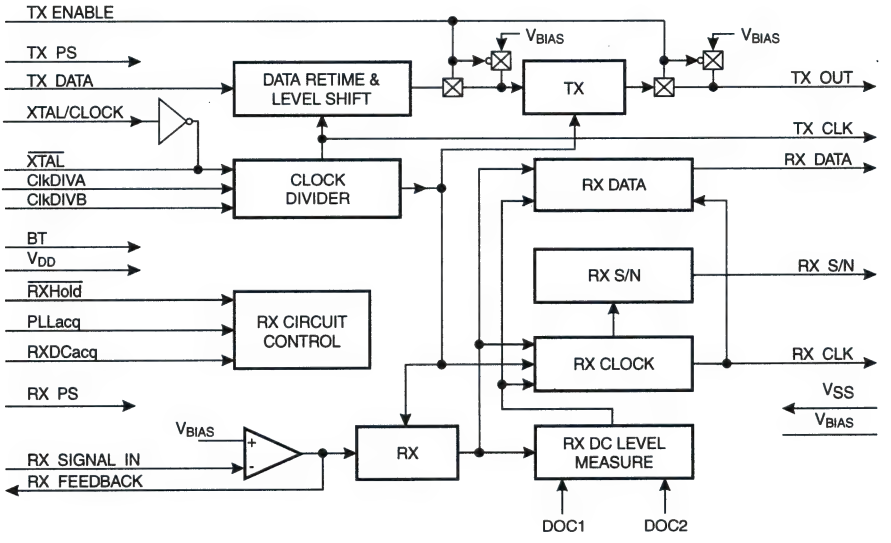


Figure 1: Device Block Diagram

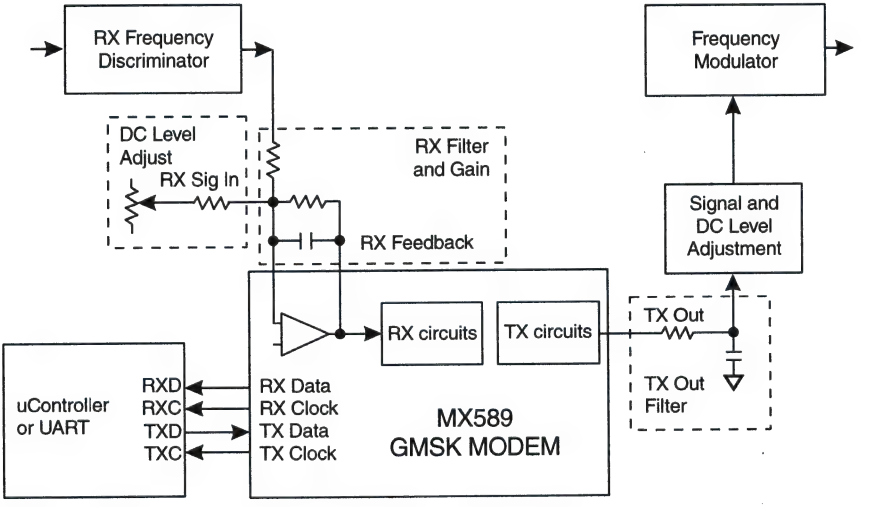


Figure 2: System Block Diagram

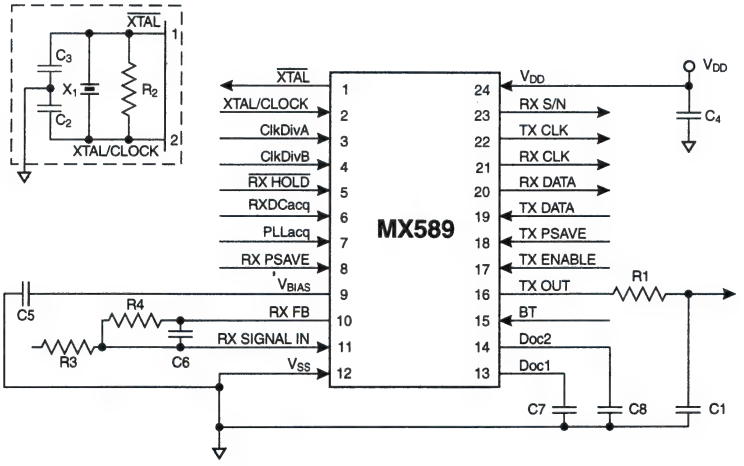
© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc.# 20480103.009

2. Signal List

Pin No.	Name	Type	Description
1	$\overline{XTAL}$		The output of the on-chip clock oscillator.
2	Xtal/Clock		The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock (f_{XTAL}) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the $\overline{XTAL}$ pin left unconnected
3	ClkDivA		Logic level inputs control the internal clock divider and therefore the transmit and receive data rate. See Table 1
4	ClkDivB		Logic level inputs control the internal clock divider and therefore the transmit and receive data rate. See Table 1
5	$\overline{Rx\ HOLD}$		A logic 0 applied to this input will freeze the Clock Extraction and Level Measurement circuits unless they are in Acquire mode.
6	RxDCacq		A logic 1 applied to this input will set the RX Level Measurement circuitry to the Acquire mode.
7	PLLacq		A logic 1 applied to this input will set the Rx Clock Extraction circuitry to Acquire mode (see Table 2).
8	Rx PSAVE		A logic 1 applied to this input will powersave all receive circuits except for Rx CLK output (which will continue at the set bit-rate) and cause the Rx Data and Rx S/N outputs to go to a logic 0.
9	V_{BIAS}		The internal circuitry bias line, held at $V_{DD}/2$, this pin must be bypassed to V_{SS} by a capacitor mounted close to the pin.
10	Rx FB		Output of the Rx Input Amplifier.
11	Rx Signal In		Input to Rx Input Amplifier.
12	V_{SS}		Negative supply. Signal ground.
13	Doc1		Connections to the Rx Level Measurement Circuitry. A capacitor should be connected from each pin to V_{SS}. See Figure 3.
14	Doc2		Connections to the Rx Level Measurement Circuitry. A capacitor should be connected from each pin to V_{SS}. See Figure 3.
15	BT		A logic level to select the modem BT (the ratio of the Tx Filter's -3dB frequency to the Bit-Rate). A logic 1 = BT of 0.5, a logic 0 = BT of 0.3.
16	Tx Out		Tx signal output from the MX589 GMSK Modem.
17	Tx Enable		A logic 1 applied to this input enables the transmit data path through the Tx Filter to the Tx Out pin. A logic 0 will place the Tx Out pin at V_{BIAS} via a high impedance.
18	Tx PSAVE		A logic 1 applied to this input will powersave all transmit circuits except for the Tx Clock.
19	Tx Data		The logic level input for the data to be transmitted. This data should be synchronous with Tx CLK.
20	Rx Data		A logic level output carrying the received data, synchronous with Rx CLK.
21	Rx CLK		A logic level clock output at the received data bit-rate.
22	Tx CLK		A logic level clock output at the transmit-data rate.
23	Rx S/N		A logic level output which may be used as an indication of the quality of the received signal.
24	V_{DD}		Positive supply. A single 5.0V power supply is required. Levels and voltages within this modem are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the pin.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc.# 20480103.009

3. External Components



R1	Note 1	±5%
R2	1.0MΩ	±10%
R3	Note 2	±10%
R4	100kΩ	±10%
C1	Note 1	±10%
C2	Note 3	
C3	Note 3	

C4	0.1µF	±20%
C5	1.0µF	±20%
C6	22.0pF	±20%
C7	Note 4	
C8	Note 4	
X1	Note 5	

Figure 3: Recommended External Components

External Components Notes:

1. The RC network formed by R1 and C1 is required between the Tx Out pin and the input to the modulator. This network, which can form part of any DC level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor C1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

   The component values should be chosen so that the product of the resistance and the capacitance is:

   BT of 0.3 = 0.34/bit rate (bps) BT of 0.5 = 0.22/bit rate (bps)

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Data Rate bps	BT = 0.3		BT = 0.5	
	R1	C1	R1	C1
4000	120kΩ	680pF	120kΩ	470pF
4800	100kΩ	680pF	100kΩ	470pF
8000	91kΩ	470pF	120kΩ	220pF
9600	91kΩ	390pF	47kΩ	470pF
16000	47kΩ	470pF	91kΩ	150pF
19200	100kΩ	180pF	91kΩ	120pF
32000	47kΩ	220pF	47kΩ	150pF
38400 *	47kΩ	180pF	47kΩ	120pF
64000 *	56kΩ	100pF	51kΩ	68pF
* $V_{DD} \geq 4.5V$				

Note: In all cases the value of R1 should not be less than 20.0 kΩ, and the calculated value of C1 includes calculated parasitic capacitance.

2. R3, R4 and C6 form the gain components for the Rx Input signal. R3 should be chosen as required by the signal input level.
3. The values chosen for C2 and C3 (including stray capacitance), should be suitable for the applied V_{DD} and the frequency of X1.

   As a guide : C2 = C3 = 33pF at 1.0MHz falling to 18pF at the maximum frequency.

   At 3.0 volts, C2 = C3 = 33pF falling to 18pF at 5.0MHz. The equivalent series resistance of X1 should be less that 2.0kΩ falling to 150Ω at the maximum frequency. Stray capacitance on the Xtal/Clock circuit pins must be minimized.
4. C7 and C8 should both be .015µF for a data rate of 8kbps, and inversely proportional to the data rate for other data rates, e.g. .030µF at 4kbps, .0018µF at 64kbps.
5. The MX589 can operate correctly with Xtal/Clock frequencies between 1.0MHz and 8.2MHz (V_{DD} = 5.0V) and 1.0MHz to 5.0MHz (V_{DD} = 3.0V) see Table 1 for examples. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer. Operation of this device without a Xtal or Clock input may cause device damage.

4. General Description

4.1 Clock Oscillator Divider

The Tx and (nominal) Rx data rates are determined by division of the frequency present at the $\overline{\text{Xtal}}$ pin, which may be generated by the on-chip Xtal oscillator or derived from an external source. Any Xtal/clock frequency in the range 1.0MHz to 5.0MHz for V_{DD} = 3.0V, or 1.0 MHz to 8.2MHz for V_{DD} = 5.0V may be used, depending on the desired data rate.

The division ratio is controlled by the logic level inputs on ClkDivA and ClkDivB pins, as shown in Table 1, together with an indication of how various standard data rates may be derived from common µP Xtal frequencies.

$$\text{Data Rate} = \frac{\text{Xtal/Clock Frequency}}{\text{Division Ratio (Clk Div A/B)}}$$

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

			Xtal/Clock Frequency (MHz)				
			8.192	4.9152	4.096	2.4576	2.048
					(12.288/3)	(12.288/5)	(6.144/3)
Inputs		Division Ratio					
ClkDiv A	ClkDiv B	Xtal Freq. Data Rate	Data Rate (bps)				
0	0	128	64000*	38400*	32000	19200	16000
0	1	256	32000	19200	16000	9600	8000
1	0	512	16000	9600	8000	4800	4000
1	1	1024	8000	4800	4000		

* V_{DD} > = 4.5V

Table 1: Clock/Data Rates

Note: The device operation is not guaranteed above 64kbps or below 4kbps at the relevant supply voltage.

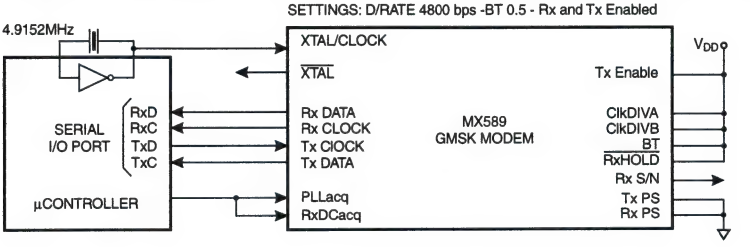


Figure 4: Minimum µController System Connections

4.2 Receive

4.2.1 Rx Signal Path Description

The function of the Rx circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide DC level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide Rx data in a binary form.
6. Assess signal quality and provide Signal-to-Noise information.

The output of the radio receiver's Frequency Discriminator should be fed to the MX589's Rx Filter by a suitable gain and DC level adjusting circuit. This circuit can be built with external components around the on-chip Rx Input Amplifier. The gain should be set so that the signal level at the Rx Feedback pin is nominally 1V peak to peak (for V_{DD} = 5.0V) centered around V_{BIAS} when receiving a continuous 1111000011110000.. data pattern.

Positive going signal excursions at Rx Feedback pin will produce a logic 0 at the Rx Data Output. Negative going excursions will produce a logic 1.

The received signal is fed through the lowpass Rx Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors, one of which measures the amplitude of the positive parts of the received signal. The other measures the amplitude of the negative portions. (Positive refers to signal levels higher than V_{DD}/2, and negative to levels lower than V_{DD}/2.) External capacitors are used by these detectors, via the Doc1 &

Doc2 pins, to form voltage hold or integrator circuits. These two levels are then used to establish the optimum DC level decision-thresholds for the Clock and Data extraction, depending upon the Rx signal amplitude and any DC offset.

4.2.2 Rx Circuit Control Modes

The operating characteristics of the Rx Level Measurement and Clock Extraction circuits are controlled, as shown in Table 2, by logic level inputs applied to the PLLacq, $\overline{\text{Rx HOLD}}$ and RxDCacq pins to suit a particular application, or to cope with changing reception conditions.

With reference to Figure 5, the Rx Mode Control diagram:

In general, a data transmission will begin with a preamble, for example, 1100110011001100, to allow the receive modem to establish timing and level-lock as quickly as possible. After the Rx carrier has been detected, and during the time that the preamble is expected, the RxDCacq and PLLacq Inputs should be switched from a logic 0 to a logic 1 so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The $\overline{\text{Rx HOLD}}$ input should normally be held at a logic 1 while data is being received, but may be driven to a logic 0 to freeze the Level Measuring Clock Extraction circuits during a fade. If the fade lasts for less than 200 bit periods, normal operation can be resumed by returning the $\overline{\text{Rx HOLD}}$ input to a logic 1 at the end of the fade. For longer fades , it may be better to reset the Level Measuring circuits by placing the RxDCacq to a logic 1 for 10 to 20 bit periods.

$\overline{\text{Rx HOLD}}$ has no effect on the level Measuring circuits while RxDCacq is at a logic 1, and has no effect on the PLL while PLLacq is at a logic 1.

A logic 0 on $\overline{\text{Rx HOLD}}$ does not disable the Rx Clock output, and the Rx Data Extraction and S/N Detector circuits will continue to operate.

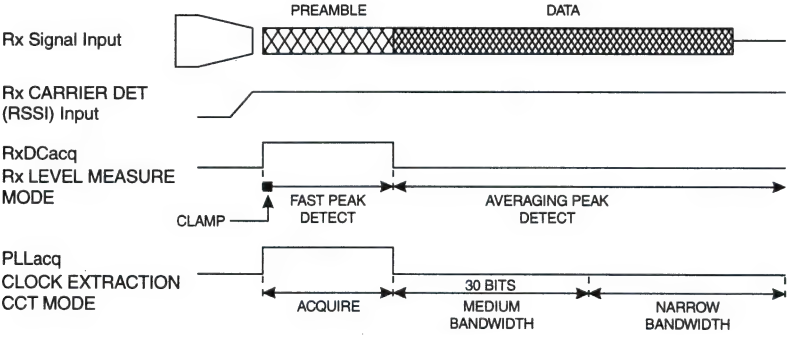


Figure 5: Rx Mode Control Diagram

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

PLLacq	$\overline{\text{Rx HOLD}}$	PLL Action	
1	1	Acquire	Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. This mode will operate as long as PLLacq is a logic 1
1 to 0	1	Medium Bandwidth	The correction applied to the extracted clock is limited to a maximum of ± 1/16th bit-period for every two received zero crossings. The PLL operates in this mode for a period of about 30 bits immediately following a 1 to 0 transition of PLLacq input, provided that the $\overline{\text{Rx HOLD}}$ input is a logic 1.
0	1	Narrow Bandwidth	The correction applied to the extracted clock is limited to a maximum of ± 1/64th bit-period for every two received zero crossings. The PLL operates in this mode whenever the $\overline{\text{Rx HOLD}}$ input is a logic 1 and PLLacq has been a logic 0 for at least 30 bit periods (after Medium Bandwidth operation for instance)
0	0	Hold	The PLL feedback loop is broken, allowing the Rx Clock to freewheel during signal fade periods.
RxDCacq	**$\overline{\text{Rx HOLD}}$**	**Rx Level Measure Action**	
0 to 1	X	Clamp	Operates for one bit-time after a 0 to 1 transition of the RxDCacq input. The external capacitors are rapidly charged towards a voltage mid way between the received signal input level and V_{BIAS} with the charge time-constant being of the order of 0.5 bit-time.
1	X	Fast Peak Detect	The voltage detectors act as peak detectors, one capacitor is used to capture the positive -going signal peaks of the Rx Filter output signal and the other capturing the negative-going peaks. The detectors operate in this mode whenever the RxDCacq input is at a logic 1 except for the initial 1-bit Clamp Mode time.
0	1	Averaging Peak Detect	Provides a slower but more accurate measurement of the signal peak amplitudes.
0	0	Hold	The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000 bits] towards V_{BIAS})

X = Don't care

Table 2: PLL and Rx Level Measurement Operational Modes

4.2.3 Rx Clock Extraction

Synchronized by a PLL circuit to zero-crossings of the incoming data, the Rx Clock Extraction circuitry controls the Rx Clock output. The Rx Clock is also used internally by the Data Extraction circuitry. The PLL parameters can be varied by the Rx Circuit Control inputs PLLacq and Rx HOLD to operated in one of four PLL modes as described in Table 2

4.2.4 Rx Data Extraction

The Rx Data Extraction circuit decides whether each received bit is a 1 or 0 by sampling the received signal, after filtering, and comparing the sample values to an adaptive threshold derived from the Level Measuring circuit. This threshold is adapted from bit to bit to compensate for intersymbol interference caused by the bandlimiting of the overall transmission path and the Gaussian premodulation filter. The extracted data is output from the Rx Data pin, and should be sampled externally on the rising edge of the Rx CLK.

4.2.5 Rx S/N Detection

The Rx S/N Detector system classifies the incoming zero-crossings as GOOD or BAD depending upon the time when each crossing actually occurs with respect to its expected time as determined by the Clock Extraction PLL. This information is then processed to provide a logic level output at the Rx S/N pin. A high level indicates a series of GOOD crossings; a low level indicates a BAD crossing.

By averaging this output it is possible to derive a measure of the Signal-to-Noise-Ratio and therefore the Bit-Error-Rate of the received signal.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

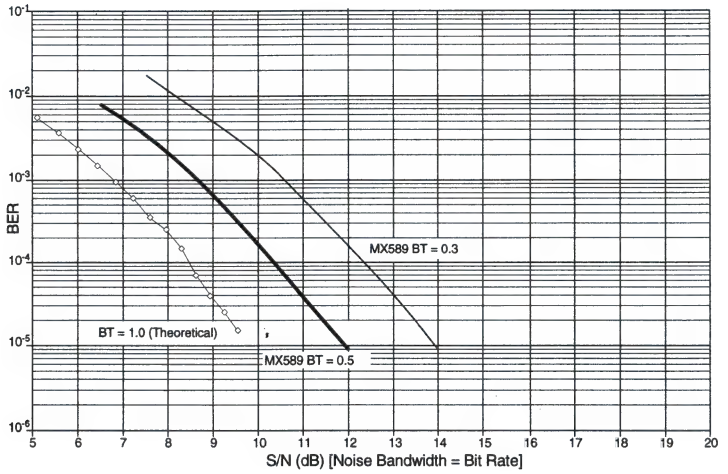


Figure 6: Typical Bit-Error-Rate Performance

4.2.6 Rx Signal Quality

The effect of input Rx signal quality on the Rx S/N output is shown in Figure 7.

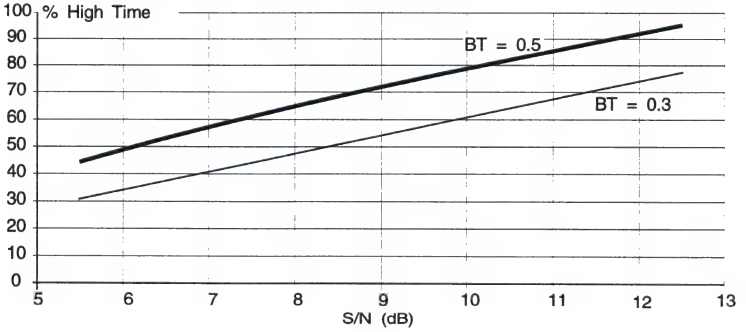


Figure 7: Typical Rx S/N Output High time (%) vs Input S/N

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.3 Transmit

4.3.1 Tx Signal Path Description

The binary data applied to the Tx Data input is retimed within the chip on each rising edge of the Tx Clock and then converted to a 1-volt peak-to-peak binary signal centered about V_{BIAS} (for V_{DD} = 5.0V)

If the Tx Enable input is high, then this internal binary signal will be connected to the input of the lowpass Tx Filter, and the output of the filter connected to the Tx Out pin.

Tx Enable	Tx Filter Input	Tx Out Pin
1	$V_{DD}/5$ V_{P-P} Data	Filtered Data
0	V_{BIAS}	V_{BIAS} via 500kΩ

A low input to the Tx Enable will connect the input of the Tx Filter to V_{BIAS}, and disconnect the Tx Out pin from the filter, connecting it instead to V_{BIAS} through a high resistance (nominally 500kΩ).

The Tx Filter has a lowpass frequency response, which is approximately gaussian in shape as shown in Figure 9, to minimize amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency-components which would otherwise cause interference into adjacent radio channels. The actual filter bandwidth to be used in any particular application will be determined by the overall system requirements. The attenuation-vs-frequency response of the transmit filtering provided by the MX589 have been designed to meet the specifications for most GMSK modem systems, having a -3dB bandwidth switchable between 0.3 and 0.5 times the data bit-rate (BT).

Note: An external RC network is required between the Tx Out pin and the input to the Frequency Modulator (see Figure 2 and Figure 3). This network, which can form part of any DC level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to capacitor C1 should be positioned to give maximum attenuation of high-frequency noise into the modulator.

The signal at Tx Out is centered around V_{BIAS}, going positive for logic 1 (high) level inputs to the Tx Data input and negative for logic 0 (low) inputs.

When the transmit circuits are put into a powersave mode (by a logic 1 to the Tx PS pin) the output voltage of the Tx Filter will go to V_{SS}. When power is subsequently restored to the Tx Filter, its output will take several bit-times to settle. The Tx Enable input can be used to prevent these abnormal voltages from appearing at the Tx Out pin.

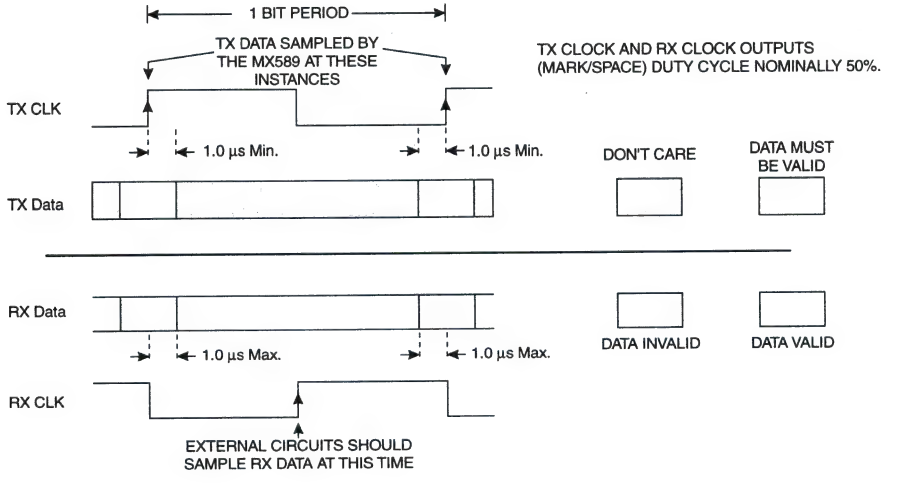


Figure 8: Rx and Tx Clock Data Timings

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

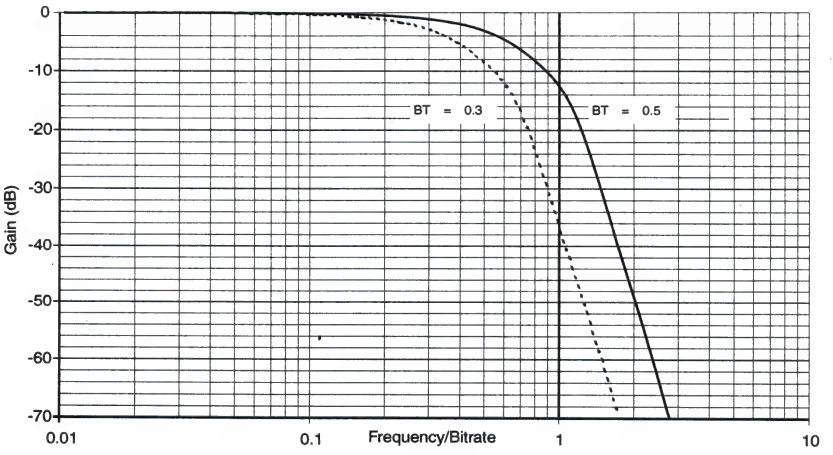


Figure 9: Tx Filter Response

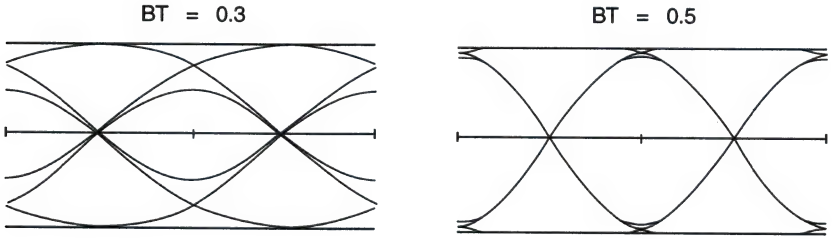


Figure 10: Typical Transmit Eye Patterns

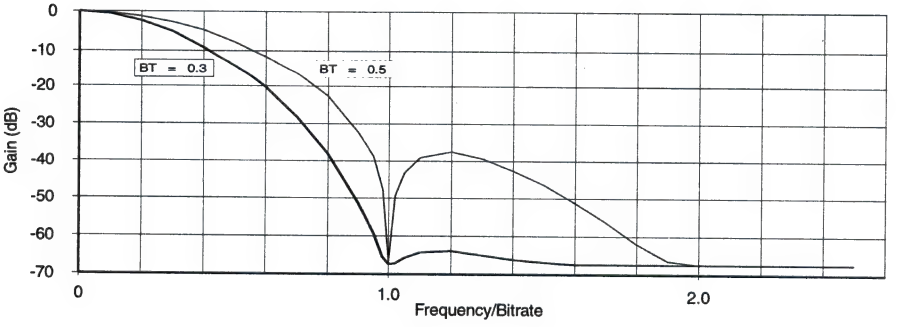


Figure 11: Tx Output spectrum (Random Data)

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.4 Data Formats

The receive section of the MX589 works best with data which has a reasonably random structure --the data should contain approximately the same number of ones as zeroes with no long sequences (>100 bits) of consecutive ones or zeroes. Also, long sequences (>100 bits) of 10101010 ... patterns should be avoided.

For this reason, it is recommended that data is made random in some manner before transmission, for example by exclusive-ORing it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble for BT = 0.3 should be at least 16 bits long, and should preferably consist of alternating pairs of ones and zeroes i.e. 110011001100 .....; the eye of pattern 10101010 .... has the most gradual slope and will yield poor peak levels for the Rx circuits. For BT = 0.5 the eye pattern of 10101010... has reduced intersymbol interference and may be used as the preamble (DC Acq pin should be held high during preamble). See Fig. 6.

4.5 Acquisition and Hold Modes

The RxDCacq and PLLacq inputs must be pulsed High for about 16 bits at the start of reception to ensure that the DC measurement and timing extraction circuits lock-on to the received signal correctly. Once lock has been achieved, then the above inputs should be taken Low again.

In most applications, there will be a DC step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the remote transmitter is turned on.

The MX589 can tolerate DC offsets in the received signal of at least ±0.5V with respect to V_{BIAS}, (measured at the Rx Feedback pin). However, to ensure that the DC offset compensation circuit operates correctly and with minimum delay, the Low to High transition of the RxDCacq and PLLacq inputs should occur after the mean input voltage to the MX589 has settled to within about 0.1V of its final value.

Note: This can place restrictions on the value of any series signal coupling capacitor.

As well as using the Rx Hold input to freeze the Level Measuring and Clock Extraction circuits during a signal fade, it may also be used in systems which use a continuously transmitting control channel to freeze the Rx circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this, the MX589 Xtal clock needs to be accurate enough that the derived RxClock output does not drift by more than about 0.1 bit time from the actual received data-rate during the time that the RxHold input is Low.

The RxDCacq input, however, may need to be pulsed high for 2 bit durations to re-establish the level measurements if the RxHold input is low for more that a few hundred bit-times (exact number depends on system crystal tolerances).

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude.

Note: These pins are driven from very high-impedance circuits, so that the DC load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

5. Application

5.1 Radio Channel Requirements

To achieve legal adjacent channel performance at high bit-rates, a radio with an accurate carrier frequency and an accurate modulation index is required. For optimum channel utilization, (e.g. low BER and high data-rates) attention must be paid to the phase and frequency response of both the IF and baseband circuitry.

5.1.1 Bitrate, BT and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on the following:

Channel spacing

Allowable adjacent channel interference

Tx filter bandwidth

Peak carrier deviation (Modulation Index)

Tx and Rx carrier frequency accuracies

Modulator and Demodulator linearity

Rx IF filter frequency and phase characteristics

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Use of error correction techniques

Acceptable error-rate

As a guide to MOBITEX operation, a raw data-rate of 8kbps at 12.5kHz channel spacing may be achievable -depending on local regulatory requirements- using a ±2kHz maximum deviation, a BT of 0.3, and no more than 1.5kHz discrepancy between Tx & Rx carrier frequencies. Forward error correction (FEC) could then be used with interleaving to reduce the effect of burst errors.

Reducing the data-rate to 4.8kbps would allow the BT to be increased to 0.5, improving the error-rate performance.

5.1.2 FM Modulator, Demodulator and IF

For optimum performance, the eye pattern of the received signal (when receiving random data) applied to the MX589 should be as close as possible to the Transmit eye pattern examples shown in Figure 11.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening.

To achieve this, attention must be paid to -

Linearity and frequency/phase response of the Tx frequency modulator. Unless the transmit data is especially encoded to remove low frequency components, the modulator frequency response should extend down to a few hertz. This is because two-point modulation is necessary for synthesized radios.

Bandwidth & phase response of the Rx IF filters.

Accuracy of the Tx and Rx carrier frequencies -any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally, the Rx demodulator should be DC coupled to the MX589 Rx Signal In pin (with a DC bias added to center the signal at the Rx Feedback pin around $V_{DD}/2$ [V_{BIAS}]). However AC coupling can be used provided that:

The 3 dB cut-off frequency is 20Hz or below (i.e. a 0.1µF capacitor in series with 100kΩ).

The data does not contain long sequences of consecutive ones or zeroes.

Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of an RF carrier) for the voltage into the MX589 to settle before the RxDCacq line is strobed.

5.1.3 Two Point Modulation

When designing the MX589 into a radio that uses a frequency synthesizer, a two-point modulation technique is recommended. This is both to prevent the radio's PLL circuitry from counteracting the modulation process, and to provide a clean flat modulation response down to DC

Figure 12 shows a suggested basic configuration to provide a two-point modulation drive from the MX589 Tx Output using MX•COM's MX019 Digitally Controlled Quad Amplifier Array. The MX019 elements provide individual set-up, calibration and dynamic control of modulation levels. Level setting control of the amplifiers/attenuators of the MX019 is via an 8-bit data word.

With reference to Figure 12:

The buffer amplifier is required to prevent loading of the MX589 external RC circuit.

Stage B, with R1/R2, provides suitable signal and DC levels for the VCO varactor; C1 is RF decoupling. The drive level should be adjusted (digitally) to provide the desired deviation.

Stage C, with R3/R4, provides the Reference Oscillator drive (application dependent). This parameter is set by adjusting for minimum AC signal on the PLL control voltage with a low-frequency modulating signal (inside the PLL bandwidth) applied.

Stage D could be used with the components shown if a negative reference drive is required.

Stage A provides buffering and overall level control.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

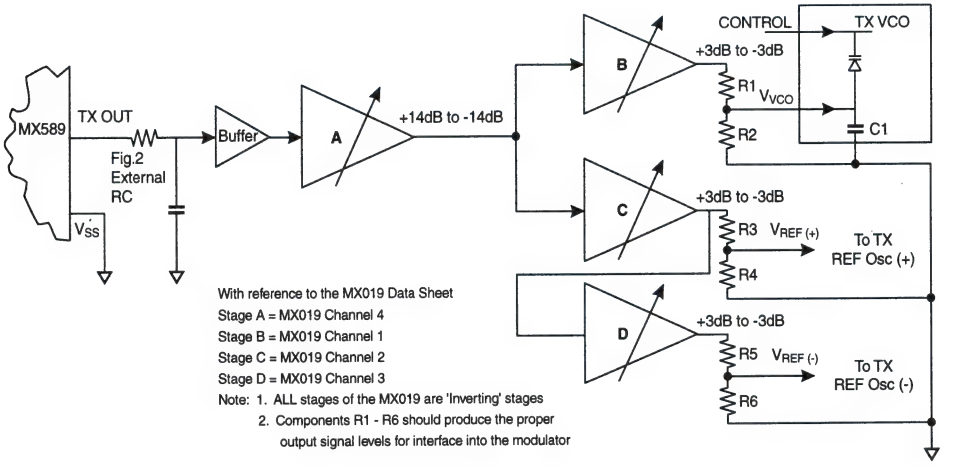


Figure 12: An Example of Two-Point Modulation Drive with Individual Adjustment Using the MX019

5.2 AC Coupling of Tx and Rx Signals

In practical applications, it will usually be possible to arrange for any AC coupling between the MX589 Tx Output and the frequency modulator to cut-off at a very low frequency such as 5.0Hz, but Ac coupling between the receive discriminator and the input of the MX589 may need to have a shorter time-constant to avoid problems from voltage steps at the output of the discriminator when changing channels or when the distant transmitter turns on.

For these reasons, as well as to maintain reasonable BER, the optimum -3dB cut-off frequencies are around 5.0Hz in the Tx path and 20.Hz in the Rx path.

Figure 13 shows the typical static Bit-Error-Rate performance of the MX589 operating under nominal conditions for various degrees of AC coupling at the Rx input and the Tx Output:

Data Rate = 8kbps V_{DD} = 5.0V T_{AMB} = 25°C Tx BT = 0.3

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

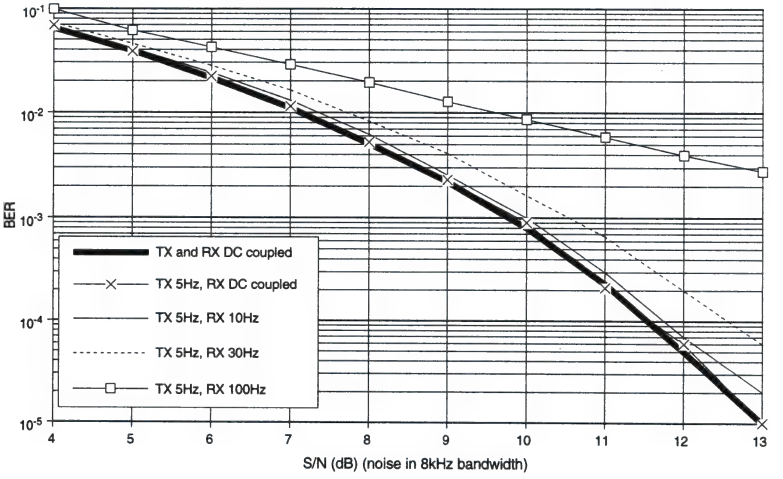


Figure 13: Effect of AC Coupling on Typical Bit-Error Rate

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / PDIP Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	85	°C
Operating Temperature	-40	85	°C
TN Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	85	°C
Operating Temperature	-40	85	°C

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Temperature		-40	85	°C
Rx and Tx Data Rate				
$V_{DD} \geq 3.0V$		4	32	kbps
$V_{DD} \geq 4.5V$		4	64	kbps
Xtal/Clock Frequency				
$V_{DD} \geq 3.0V$		1.0	5.0	MHz
$V_{DD} \geq 4.5V$		1.0	10.3	MHz
High Pulse Width	1	40		ns
Low Pulse Width	1	40		ns

Operating Limits Notes:

1. Timing for an external clock input to the Xtal/Clock pin.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V @ T_{AMB} = 25°C

Xtal Frequency = 4.096mhz Data Rate = 8kbps Noise Bandwidth = Bit Rate

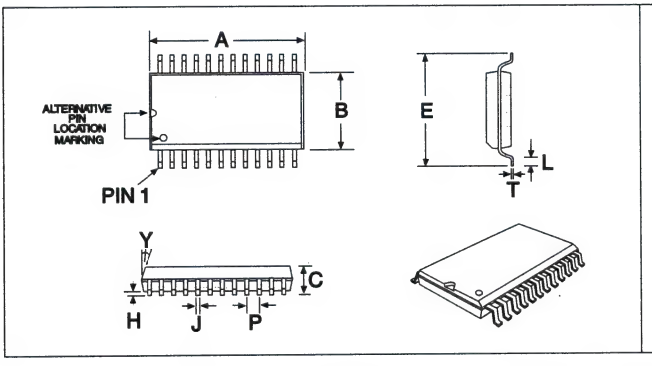
			Notes	Min.	Typ.	Max	Units
Static Values							
Supply Current	Tx PS	Rx PS	1				
I_{DD} (V_{DD} = 3.0V)							
	1	1			0.5		mA
	0	1			1.0		mA
	1	0			1.0		mA
	0	0			1.5		mA
I_{DD}							
	1	1			1.0		mA
	0	1			2.0		mA
	1	0			3.0		mA
	0	0			4.0		mA
Input Logic Level							
Logic 1 Input Level				3.5			V
Logic 0 Input Level						1.5	V
Logic Input Current			2	-5.0		5.0	µA
Logic 1 Output Level (I_{OH} = -120µA)				4.6			V
Logic 0 Output Level (I_{OL} = -120µA)						0.4	V
Transmit Parameters							
Tx OUT, Output Impedance			3		1.0		kΩ
Tx OUT, Level			4,10	0.8	1.0	1.2	V_{P-P}
Tx Data Delay							
BT = 0.3			5		2.0	2.5	bit-periods
BT = 0.5			5		1.5	2.0	bit-periods
Tx PS to Output-Stable time			6		4.0		
Receive Parameters							
Rx Amplifier-							
Input Impedance				1.0			MΩ
Output Impedance			7		10.0		kΩ
Voltage Gain					50.0		dB
Rx Filter Signal Input Level			8, 10	0.7	1.0	1.3	V_{P-P}
Rx Time Delay			9			3.0	bit-periods
On-Chip Xtal Oscillator							
R_{IN}				10.0			MΩ
R_{OUT}			11		50.0		kΩ
Voltage Gain			11		25.0		dB

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Operating Characteristics Notes:

1. Not including current drawn from the MX589 pins by external circuitry. See Absolute Maximum Ratings.
2. For V_{IN} in the range V_{SS} to V_{DD}.
3 For a load of 10kW or greater. Tx PS input at logic 0; Tx Enable = 1.
4. Data pattern of 1111000011110000 ..
5. Measured between the rising edge of Tx Clock and the center of the corresponding bit at Tx Out.
6. Time between the falling edge of Tx PS and the Tx Out voltage stabilizing to normal output levels.
7. For a load of 10kW or greater. Rx PS input at logic 0.
8. For optimum performance, Measured at the Rx Feedback pin for a 1111000011110000 ... pattern.
9. Measured between the center of bit at Rx Signal In and corresponding rising edge of the Rx Clock.
10 Levels are proportional to applied V_{DD}.
11. Small signal measurement at 1.0kHz with no load on Xtal output.

6.2 Packaging

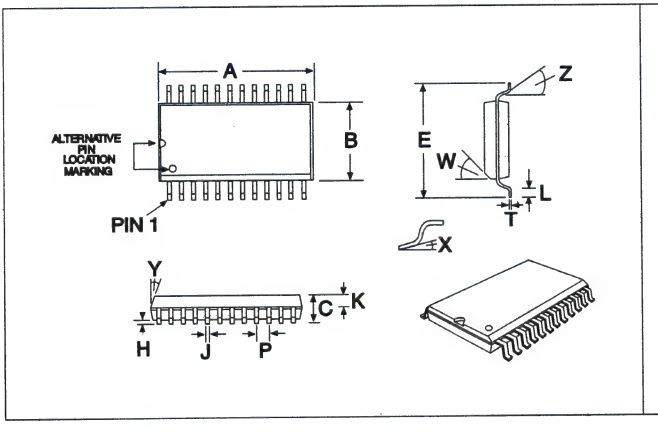


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 14: 24-pin TSSOP Mechanical Outline: ***Order as part no. MX589TN***



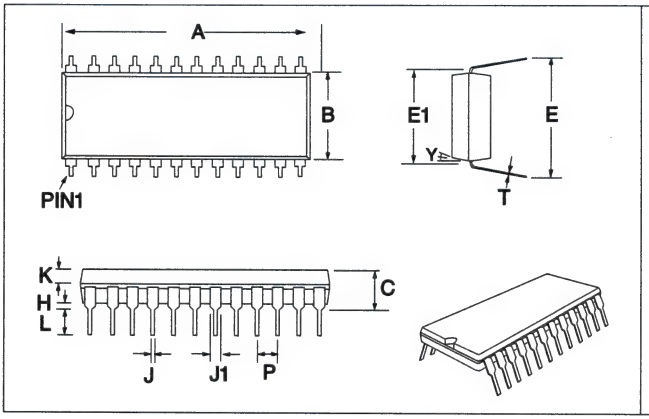
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 24-pin SOIC Mechanical Outline: ***Order as part no. MX589DW***

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 24-pin PDIP Mechanical Outline: *Order as part no. MX589P*

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

MX•COM, INC. MiXed Signal ICs

DATABULLETIN

MX809 MSK MODEM

C-BUS COMPATIBLE

PRELIMINARY INFORMATION

DESCRIPTION

The MX809 is an intelligent, half-duplex 1200 baud MSK Modem which operates under C-BUS control. This modem provides software selectable checksum generation and error checking in accordance with MPT1327.

MX809J
24-pin CDIP

MX809LH
24-pin PLCC

In TX Mode the MX809 will:

1. a) Accept from the host and transmit 8-bit bytes of data as instructed (preamble, sync, address and data).

b) Internally calculate and insert a 2 byte checksum based on the preceding 6 bytes of data, or

c) Disable the internal checksum generator and continuously transmit the data supplied.

2. Transmit 1 hang-bit and go to TX Idle when all loaded data bytes have been transmitted.

In RX Mode the MX809 will:

1. Detect and carry out bit synchronization within 16 bits.

2. a) Search and detect the user-programmed Sync (or its opposite logic sense) Word and carry out frame synchronization. Data will then be output in 8-bit bytes via the RX Data Buffer.

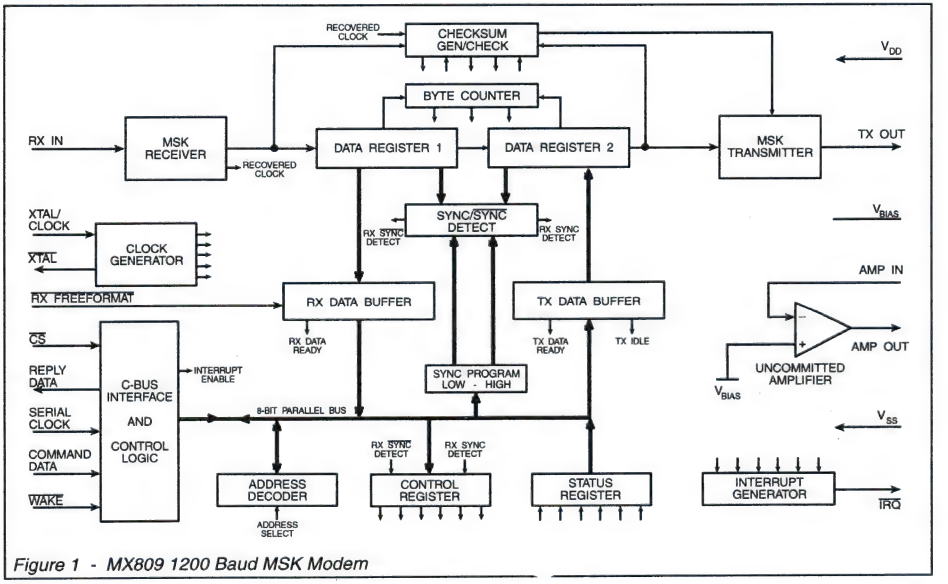


Figure 1 - MX809 1200 Baud MSK Modem

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

DESCRIPTION...

b) Use the received checksum to calculate the presence of any errors, setting the Status Register accordingly.

3. Make the incoming data directly available via the RX Data Buffer (RX Freeformat), overriding the synchronization requirements.

RX input timing is achieved by recovering an RX clock from the incoming data stream. Output tones are timed to the internally generated TX clock. Filter, register clocks, and transmit MSK tone frequencies are derived internally from the external Xtal or clock pulse input.

A 4.032 MHz Xtal or clock input is required for compliance with the MPT1327 Signalling Specification. *Note: All information contained in this data bulletin is specified using a 4.032 MHz Xtal, 1200 bps baud rate, with Mark and Space frequencies of 1200 Hz and 1800 Hz.* The MX809 has a non-committed amplifier on-chip for general applications in the DBS 800 serie. The MX809 is a low-power 5V integrated circuit that incorporates Powersave modes to further reduce power requirements. It is available in 24-pin Cerdip and 24-lead SMT Packages.

PIN FUNCTION CHART

Pin	Function
1	**$\overline{\text{Xtal}}$**: This is the output of the on-chip clock oscillator. External components are required at this input when a Xtal input is used. See Figure 2, Inset.
2	**Xtal/Clock**: This is the input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2, Inset.
3	**Interrupt Request ($\overline{\text{IRQ}}$)**: The output of this pin indicates an interrupt condition to the microcontroller by going to a logic "0." This is a "wire-or able" output that enables the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin is an open-drain output, and therefore has a low impedance pulldown to logic "0" when active and a high impedance when inactive. The conditions that cause interrupts are indicated in the Status Register and are shown below: TX Idle — RX Data Ready — TX Data Ready RX SYNC Detect — RX $\overline{\text{SYNC}}$ Detect Interrupt outputs can be disabled by bit 3 of the Control Register.
4	**N/C**
5	**N/C**
6	**$\overline{\text{RX Freeformat}}$**: When this input is logic "0" in the RX Mode, it allows received data to be read from the RX Data Buffer via the Reply Data line without having to achieve byte synchronization (SYNC/$\overline{\text{SYNC}}$) first. Data will continue to be available after this input goes to a logic "1" until either a SYNC or $\overline{\text{SYNC}}$ Prime Bit is set or the modem is set to TX Mode. When held at a logic "1" the modem operates normally. This pin has an internal 1MΩ pullup resistor. Note: If this input is held at a logic "0" in the TX Mode, the RX Data Ready bit in the Status Register may occasionally be set, but not cause an interrupt. If this input is a logic "0" when going into the RX Mode, an RX Data Ready interrupt may be generated immediately (in this case the first byte of RX data should be ignored).
7	**V_{BIAS}**: The internal circuitry bias line, this is held at $V_{DD}/2$. This pin must be decoupled to V_{SS} by capacitor C_3. See Figure 2.
8	**Amp In**: The inverting input to the on-chip uncommitted amplifier.
9	**Amp Out**: The output of the on-chip uncommitted amplifier.
10	**RX In**: This is the 1200 baud, 1200Hz/1800Hz received MSK signal input. The input signal to this pin must be a.c. coupled via capacitor C_4. See Figure 2.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

PIN FUNCTION CHART

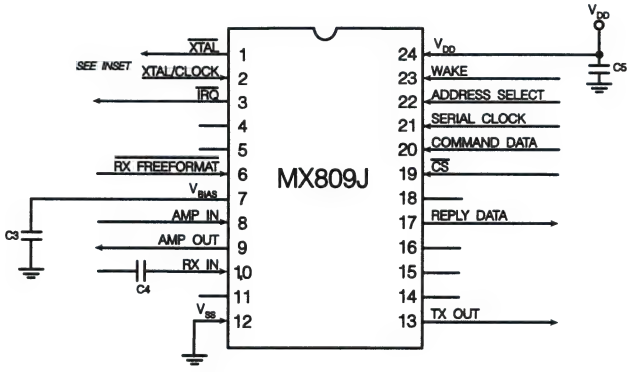
Pin	Function
11	**N/C**
12	V_{SS}: Negative Suply (GND).
13	**TX Out**: This is the 1200 baud, 1200Hz/1800Hz MSK TX output. When not transmitting data the output impedance of this pin is high. On power-up this output can be any level. A General Reset command is required to ensure that this output attains V_{BIAS} initially.
14	**N/C**
15	**N/C**
16	**N/C**
17	**Reply Data**: This is the C-BUS serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the microcontroller. See Timing Diagrams.
18	**N/C**
19	**Chip Select ($\overline{CS}$)**: The C-BUS data loading control function, this input is provided by the microcontroller. Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See Timing Diagrams.
20	**Command Data**: This is the C-BUS serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (bit7) first, and LSB (bit 0) last, synchronized to the Serial Clock. See Timing Diagrams.
21	**Serial Clock**: This is the C-BUS serial clock input. This clock, produced by the microcontroller, is used for transfer timing of commands and data to and from the MSK Modem. See Timing Diagrams.
22	**Address Select**: This pin enables two MX809s to be used on the same C-BUS, providing full-duplex operation. When at a logic "1" Address/Command bytes (with the exception of a General Reset) must have bit 3 set to a logic "1" to address this device. See Tables 1 and 2.
23	**$\overline{Wake}$**: This input can be used to reactivate the MX809 from Powersave. The device will be in Powersave when both this pin and bit 2 of the Control Register are set to a logic "1." Recovery from Powersave is achieved by putting either the $\overline{Wake}$ pin or the Powersave bit in the Control Register to logic "0." This allows MX809 activation by the microcontroller or an external signal, such as R.S.S.I. or Carrier Detect.
24	V_{DD}: Positive supply. A single +5V power supply is required. Levels and voltages within the MSK Modem are dependent upon this supply.

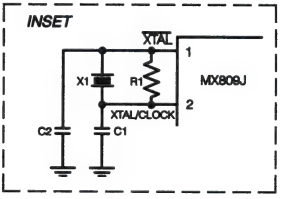
Powersave (CR bit 2)	$\overline{Wake}$	MX809 Condition
1	1	Powersave
0	1	Enabled
1	0	Enabled
0	0	Enabled

Note: Pins 4, 5, 11, 14, 15, 16 and 18 may be connected to V_{SS} to improve screening.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

External Components





Component	Value
R_1	1.0MΩ
C_1	33.0pF
C_2	33.0pF
C_3	1.0µF
C_4	0.1µF
C_5	1.0µF
X_1	4.032MHz

Tolerance: R = ±10%; C = ±20%

NOTE: XTAL circuit capacitors C_1 (C_D) and C_2 (C_G) shown in the inset are recommended in accordance with MX-COM's Crystal Oscillator Application Note, March 1990.

Figure 2 - External Components

Modem Performance

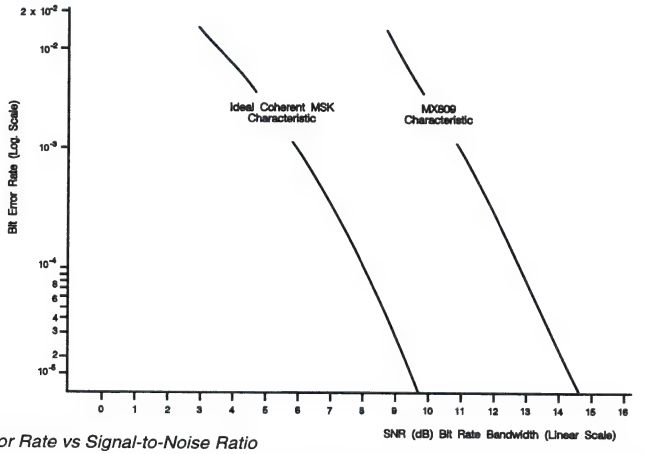


Figure 3 - Bit Error Rate vs Signal-to-Noise Ratio

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol

Control of the functions within the MX809 MSK Modem is by a group of Address/Commands (A/Cs) and appended data to and from the system microcontroller via the C-BUS. Two separate MSK Modems can be addressed. The use of these A/Cs is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB		Notes
General Reset	01	0 0 0 0 0 0 0 1	+	Control Register bits set to logic "0"
Write to Control Register	40	0 1 0 0 0 0 0 0	+	1 byte instruction to Control Register
Read Status Register	41	0 1 0 0 0 0 0 1	+	1 byte reply from Status Register
Read RX Data Buffer	42	0 1 0 0 0 0 1 0	+	1 byte of data from RX Data Buffer
Write to TX Data Buffer	43	0 1 0 0 0 0 1 1	+	1 byte of data to TX Data Buffer
Write to SYNC Program	44	0 1 0 0 0 1 0 0	+	2 bytes of SYNC Word to SYNC Prog. Reg.

Table 1 - Modem No. 1 C-BUS Address/Commands - (Address Select input at a logic "0")

Address/Commands

Instructions and data transactions to and from the MX809 consist of an Address/Command (A/C) byte followed by either further instructions or data, or a Status or RX data Reply.

Control and configuration is by writing instructions from the microcontroller to the Control Register [40_H (48_H)].

Reporting of the MX809 configurations is by reading the Status Register [41_H (49_H)]. Instructions and data are transferred via C-BUS in accordance with the timing information given in Figure 4.

Data to be transmitted as MSK is sent to the TX Data Buffer via the Command Data line. Received data is read from the RX Data Buffer via the Reply Data line.

Instructions and data transactions to and from this device are preceded by the relevant A/C.

C-BUS allocations for the MX809 are shown in Tables 1 and 2.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB		Notes
General Reset	01	0 0 0 0 0 0 0 1	+	Control Register bits set to logic "0"
Write to Control Register	48	0 1 0 0 1 0 0 0	+	1 byte instruction to Control Register
Read Status Register	49	0 1 0 0 1 0 0 1	+	1 byte reply from Status Register
Read RX Data Buffer	4A	0 1 0 0 1 0 1 0	+	1 byte of data from RX Data Buffer
Write to TX Data Buffer	4B	0 1 0 0 1 0 1 1	+	1 byte of data to TX Data Buffer
Write to SYNC Program	4C	0 1 0 0 1 1 0 0	+	2 bytes of SYNC Word to SYNC Prog. Reg.

Table 2 - Modem No. 2 C-BUS Address/Commands - (Address Select input at a logic "1")

Address Select

This input allows 2 MSK Modems on the same BUS, using the correct addressing.

When operating in a system using 2 MSK Modems, one MSK Modem is designated No. 1 and requires its Address Select input to be held at a logic "0." The second Modem (No. 2) requires its Address Select input to be held at logic "1."

All C-BUS transactions with Modem 1 will use Address/Command allocations 40_H to 44_H (Table1) and transactions with Modem 2 will use 48_H to $4C_H$ (Table 2).

For explanation purposes, further descriptions of MX809 MSK Modem internal register functions will deal primarily with MSK Modem No. 1 (Address Select at logic "0").

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol

"Write to Control Register" This "Write Only" register directs the Modem's operation.

Setting	Control Bits
MSB Bit 7	***Transmitted First*** Not used Set to "0"
6	Not used Set to "0"
5	**$\overline{\text{SYNC}}$ Prime**
0	
1	Primed
4	**SYNC Prime**
0	
1	Primed
3	**Interrupt Enable**
0	Disable
1	Enable
2	**Powersave**
0	Normal Operation
1	Powersave
1	**Checksum Enable**
0	Disable
1	Enable
0	**RX/TX Mode**
0	RX
1	TX

Table 3 - Control Register

$\overline{\text{SYNC}}$ Prime: When set, this bit enables $\overline{\text{SYNC}}$ Word detection. It is cleared on a successful $\overline{\text{SYNC}}$ Word detection.

SYNC Prime: When set, this bit enables SYNC Word detection. It is cleared on a successful SYNC Word detection.

Interrupt Enable: When set, this bit allows interrupts to be output by the MX809 on the $\overline{\text{IRQ}}$ line.

Powersave: Used in conjunction with the $\overline{\text{Wake}}$ input (see Pin Functions) to control the Powersave state of the MX809.

Checksum Enable: When set:

In TX: A 2-byte checksum is generated and transmitted after every 6 bytes transmitted.

In RX: After every 8 received bytes (6 information + 2 checksum) the checksum word is checked. If the checksum is correct, the RX Checksum True bit in the Status Register is set to a logic "1." When this bit is a logic "0" no checksums are generated or checked.

NOTE: Checksum operation is inhibited during the SYNC/$\overline{\text{SYNC}}$ search period.

"Read RX Data Buffer"

MSB							LSB
7	6	5	4	3	2	1	0
RX Data Buffer							

RX Data Buffer

This "Read Only" register contains the last byte of data received from the Data Register. Data is received Bit 7 (MSB) first.

"Write to TX Data Buffer"

MSB							LSB
7	6	5	4	3	2	1	0
TX Data Buffer							

TX Data Buffer

This "Write Only" register contains the next byte of data to be transmitted. Bit 7 (MSB) is transmitted first.

"Write to SYNC Program"

MSB	BYTE 1								BYTE 0							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
SYNC High								SYNC Low								

SYNC Program

This "Write Only" register is loaded with the required SYNC word. This word (or its opposite logic sense, $\overline{\text{SYNC}}$) is compared with the received synchronization word. If the required SYNC Word is less than 16 bits, the remaining bits must be programmed as preamble (10101010...etc.). Bit 15 (MSB) is loaded first.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol

"Read Status Register" This "Read Only" register indicates the source of MX809 interrupts ($\overline{IRQ}$s).

Reading	Status Bits
MSB	*Received First*
Bit 7	**Undefined**
0	"0" or
1	"1"
6	**Undefined**
0	"0" or
1	"1"
5	**RX $\overline{SYNC}$ Detect**
0	
1	$\overline{SYNC}$
4	**RX SYNC Detect**
0	
1	SYNC
3	**TX Idle**
0	
1	Idle
2	**TX Data Ready**
0	
1	TX Data Ready
1	**RX Checksum True**
0	
1	True
0	**RX Data Ready**
0	
1	RX Data Ready

Table 4 - Status Register

RX $\overline{SYNC}$ Detect
This is set and an Interrupt is generated when the correct $\overline{SYNC}$ Word is detected (if $\overline{SYNC}$ Prime is set).

It is cleared by (1) reading the Status Register, and (2) setting $\overline{RX}$/TX to logic "1."

RX SYNC Detect
This is set and an Interrupt is generated when the correct SYNC Word is detected (if SYNC Prime is set).

It is cleared by (1) reading the Status Register, and (2) setting $\overline{RX}$/TX to logic "1."

TX Idle
This is set and an Interrupt is generated when all loaded TX data and 1 "hang-bit" have been transmitted.

It is cleared by (1) writing to the TX Data Buffer, and (2) setting $\overline{RX}$/TX to logic "0."

TX Data Ready
This is set and an Interrupt generated indicating that a byte of data should be written to the TX Data Buffer.

It is cleared by (1) reading the Status Register and writing a byte of data to the TX Data Buffer, and (2) setting $\overline{RX}$/TX to logic "0."

RX Checksum True
This is set and an Interrupt is generated by a successful comparison of the received and self-generated checksums.

It is cleared by (1) reading the Status Register and the RX Data Buffer, and (2) $\overline{RX}$/TX being taken to logic "1."

RX Data Ready
When this is set and an Interrupt generated, it indicates that the RX Data Buffer is full, and that a byte of data is to be read from the RX Data Buffer. This must be read within 8 bit periods.

It is cleared by (1) reading the Status Register and the RX Data Buffer, and (2) Setting $\overline{RX}$/TX to logic "1."

Interrupt Requests ($\overline{IRQ}$)

The conditions that cause interrupts to be output (if enabled by the Control Register) from the MX809 are:

TX Idle
TX Data Ready
RX $\overline{SYNC}$ Detect
RX Data Ready
RX SYNC Detect

The Status Register should be read to find the cause of the interrupt. Interrupts are cleared by (1) reading the Status Register, or (2) changing the state of the $\overline{RX}$/TX bit.

General Reset

Upon power-up, the bits in the MX809 Modem register, and buffers will be random (either "0" or "1"). The General Reset command (01_H) will "reset" all microcircuits on the C-BUS and has the following effect on the MX809:

All bits in the Control Register will be set to logic "0." The TX Out output will be set to V_{BIAS}.

NOTE: The Status Register, RX Data Buffer, TX Data Buffer, and SYNC Program register are not affected by the General Reset Command.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

C-BUS Timing Information

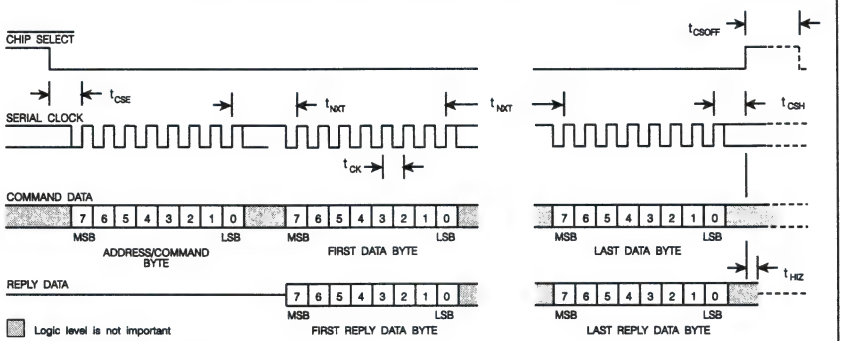


Figure 4 - C-BUS Timing

Parameter		Min.	Max.	Unit
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0	-	µs
t_{CSH}	Last Serial Clock Rising Edge to Chip Select High	4.0	-	µs
t_{HIZ}	Chip Select High to Reply Data High - Z	-	2.0	µs
t_{CSOFF}	Chip Select High	2.0	-	µs
t_{NXT}	Command Data Inter-Byte Time	4.0	-	µs
t_{CK}	Serial Clock Period	2.0	-	µs

Notes:

1. Depending on the command, 1 or 2 bytes of Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the peripheral MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into and out of the peripheral on the rising Serial Clock edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing microcontroller serial interface formats, C-BUS compatible ICs are able to work with either polarity Serial Clock pulses.

Modem Timing Information

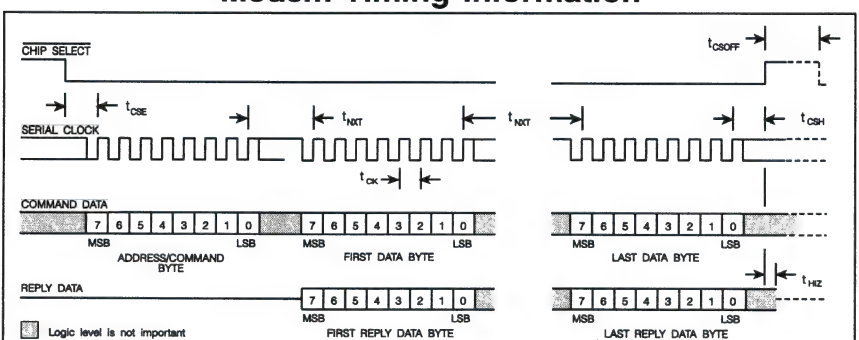


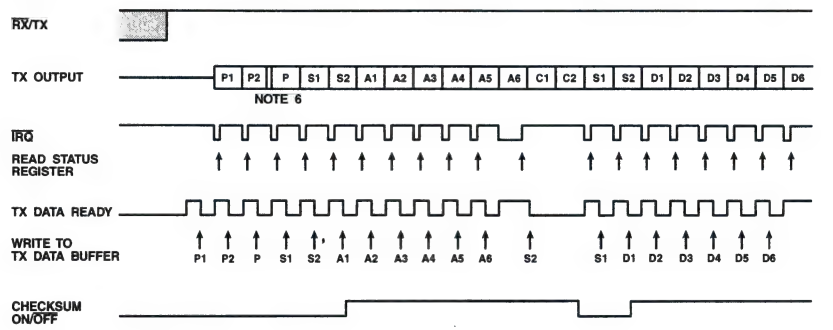
Figure 5 - Modem Timing

Notes: 1. The SYNC and $\overline{\text{SYNC}}$ detector searches the incoming bit stream starting at the end of the byte in which SYNC/$\overline{\text{SYNC}}$ Prime was set.
2. After detection of a SYNC/$\overline{\text{SYNC}}$ word, the SYNC/$\overline{\text{SYNC}}$ prime bits automatically go low (control bits 5 and 6: detector off).
3. The checksum checker is inhibited during the time SYNC/$\overline{\text{SYNC}}$ search is operating.
4. The status register will indicate whether SYNC or $\overline{\text{SYNC}}$ was detected here.
5. Any number of preamble bits can occur here.
6. Any number of bits can occur here.
7. $\overline{\text{RX}}$ Freeformat set high.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

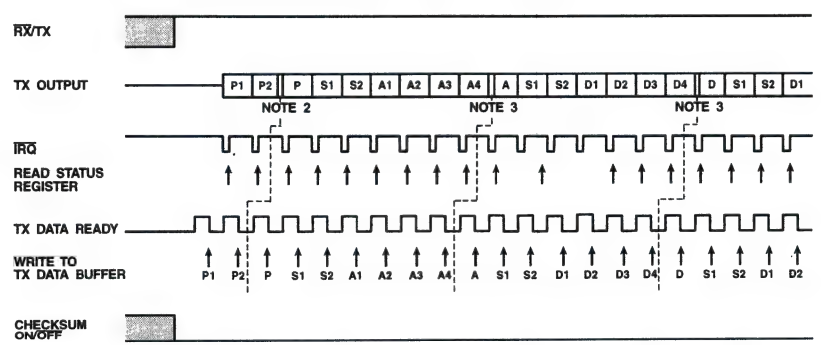
TX Timing Information

(a) TX MORE THAN ONE MESSAGE, SYNC BEFORE EVERY MESSAGE, TX CHECKSUM ENABLED


RX/TX
TX OUTPUT
P1 P2 P S1 S2 A1 A2 A3 A4 A5 A6 C1 C2 S1 S2 D1 D2 D3 D4 D5 D6
NOTE 6
IRQ
READ STATUS REGISTER
TX DATA READY
WRITE TO TX DATA BUFFER
P1 P2 P S1 S2 A1 A2 A3 A4 A5 A6 S2 S1 D1 D2 D3 D4 D5 D6
CHECKSUM ON/OFF

NOTES
1. Preamble and SYNC bytes are loaded as data from the microcontroller.
2. The TX output will be held at bias level when no data is being transmitted.
3. TX byte synchronization is established by the loading of the first preamble byte from the microcontroller.
4. Checksum must be turned off during preamble and SYNC words.
5. When RX/TX is low, TX output is at bias.
6. Any number of preamble bytes can occur here.

(b) TX MORE THAN ONE MESSAGE, TX CHECKSUM NOT ENABLED


RX/TX
TX OUTPUT
P1 P2 P S1 S2 A1 A2 A3 A4 A S1 S2 D1 D2 D3 D4 D S1 S2 D1
NOTE 2
NOTE 3
NOTE 3
IRQ
READ STATUS REGISTER
TX DATA READY
WRITE TO TX DATA BUFFER
P1 P2 P S1 S2 A1 A2 A3 A4 A S1 S2 D1 D2 D3 D4 D S1 S2 D1 D2
CHECKSUM ON/OFF

NOTES
1. Preamble, SYNC words and checksums are supplied by the microcontroller in this format as data bytes.
2. Any number of preamble bytes can occur here.
3. Any number of address/data bytes can occur here.

A - Address bytes
C - Checksum bytes
D - Data bytes
H - Hang bit
P - Preamble bytes

- Don't care state

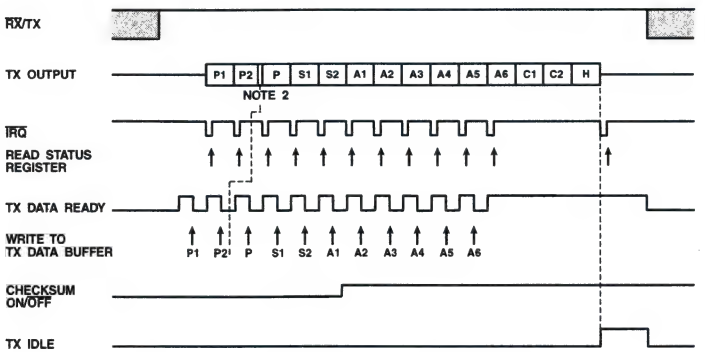
TX only - In TX, Preamble and SYNC are loaded as data from the microcontroller

Figure 6 - TX Timing

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

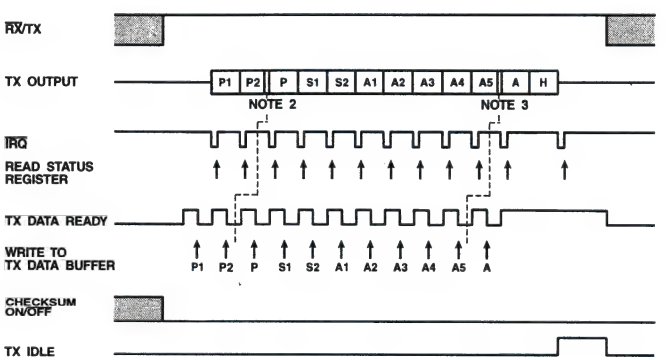
TX Timing Information

(a) TX ONE MESSAGE, TX CHECKSUM ENABLED


RX/TX
TX OUTPUT
P1 P2 P S1 S2 A1 A2 A3 A4 A5 A6 C1 C2 H
NOTE 2
IRQ
READ STATUS REGISTER
TX DATA READY
WRITE TO TX DATA BUFFER
P1 P2 P S1 S2 A1 A2 A3 A4 A5 A6
CHECKSUM ON/OFF
TX IDLE

NOTES
1. H is the "Hangover bit" (Logic 1) appended to the transmitted message before transmission is terminated.
2. Any number of preamble bytes can occur here.
3. Transmission terminates after C1, C2 and H. Termination occurs when no further data bytes are written to the TX data buffer.

(b) TX ONE MESSAGE, TX CHECKSUM NOT ENABLED



NOTES
1. H is the "Hangover bit" (Logic 1) appended to the transmitted message before transmission is terminated.
2. Any number of preamble bytes can occur here.
3. Any number of address/data bytes can occur here.
4. Transmission terminates when no further data bytes are loaded into the TX data buffer.

A - Address bytes
C - Checksum bytes
D - Data bytes
H - Hang bit
P - Preamble bytes

- Don't care state

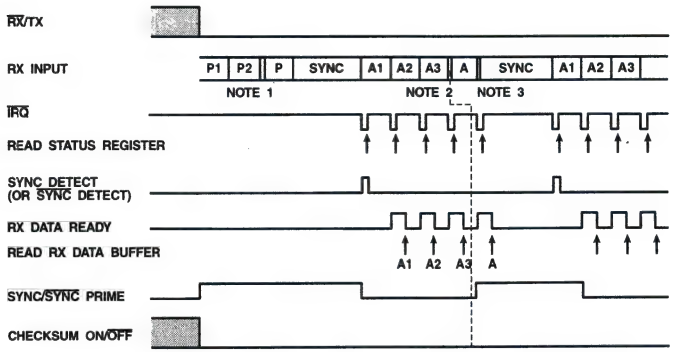
TX only - In TX, Preamble and SYNC are loaded as data from the microcontroller

Figure 7 -- TX Timing

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

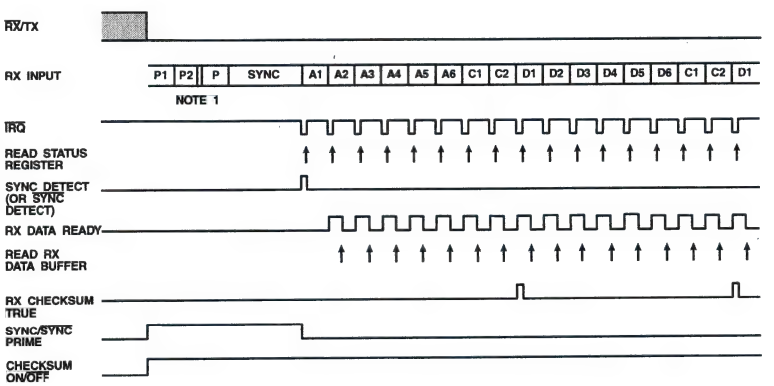
RX Timing Information

(a) RX SYNC/$\overline{\text{SYNC}}$ REQUIRED BEFORE EVERY MESSAGE, RX CHECKSUM NOT ENABLED



NOTES
1. Any number of preamble bits can occur here.
2. Any number of address/data bytes can occur here.
3. Any number of bits can occur here.
4. RX Freeformat set high.

(b) RX ADDITIONAL DATA FOLLOWS INITIAL ADDRESS (6 DATA & 2 CHECKSUM BYTES) DATA, RX CHECKSUM ENABLED


RX/TX
RX INPUT
P1 P2 P SYNC A1 A2 A3 A4 A5 A6 C1 C2 D1 D2 D3 D4 D5 D6 C1 C2 D1
NOTE 1
IRQ
READ STATUS REGISTER
SYNC DETECT (OR SYNC DETECT)
RX DATA READY
READ RX DATA BUFFER
RX CHECKSUM TRUE
SYNC/SYNC PRIME
CHECKSUM ON/OFF

NOTES
1. Any number of preamble bits can occur here.
2. RX Freeformat set high.

A - Address bytes
C - Checksum bytes
D - Data bytes
H - Hang bit
P - Preamble bytes

- Don't care state

TX only - In TX, Preamble and SYNC are loaded as data from the microcontroller

Figure 8 - RX Timing

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin	-0.3V to (V_{DD}+0.3 V)
Sink/source current	
(supply pins)	±30mA
(other pins)	±20mA
Total device dissipation (@T_{AMB} 25°C)	800 mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/clock f_0 = 4.032MHz

Audio level 0dB ref = 308 mVrms @ 1kHz

Bit Rate = 1200 bps

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply current (enabled)		-	5.0	-	mA
Supply current (powersave)		-	2.0	-	mA
Dynamic Values					
Digital Interface					
Input Logic "1"	1	3.5	-	-	V
Input Logic "0"	1	-	-	1.5	V
Output Logic "1" (IOH = -120µA)	2	4.6	-	-	V
Output Logic "0" (IOL = 360µA)	2,3	-	-	0.4	V
Digital Input Current					
V_{IN} = Logic "1" or "0"	1	-	-	1.0	µA
Digital Input Capacitance	1	-	-	7.5	pF
Tri-state "Off" Leakage Current	8	-4.0	-	4.0	µA
Analog Impedance					
Input Impedance		100	-	-	kΩ
Output Impedance					
Transmitting Data		-	6.0	10.0	kΩ
Not Transmitting Data		-	1.0	-	MΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}		5.0	-	15.0	kΩ
Gain		-	15.0	-	dB
Frequency	4	-	4.032	-	MHz
Receiver					
Signal Input Levels	5	-9.0	-2.0	10.5	dB
Bit Error Rate					
at 12dB SNR		-	7.0	-	10^{-4}
at 20dB SNR		-	1.0	-	10^{-5}
Synchronization at 12dB SNR	6				
Probability of Bit 8 being correct		-	99.0	-	%
Probability of Bit 16 being correct		-	99.5	-	%

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Transmitter					
Output Level		-	0	-	dB
Output Level Variation		-1.0	-	1.0	dB
Output Distortion		-	3.0	5.0	%
Third Harmonic Distortion		-	2.0	3.0	%
Logic "1" Frequency	7	-	1200	-	Hz
Logic "0" Frequency	7	-	1800	-	Hz
Isochronous Distortion					
1200Hz-1800Hz		-	25.0	40.0	µs
1800Hz-1200Hz		-	20.0	40.0	µs
Uncommitted Amplifier					
Bandwidth		-	200	-	kHz
Gain		-	50.0	-	dB
Input Impedance		1.0	-	-	MΩ
Output Impedance		-	-	10.0	kΩ

Notes
1. Device control pins: Serial Clock, Command Data, $\overline{\text{Wake}}$ and $\overline{\text{CS}}$.
2. Reply Data output.
3. $\overline{\text{IRQ}}$ output.
4. For baud rate specified (1200 baud).
5. Signal-to-Noise Ratio = 50dB.
6. The response time is measured using a 10101010....101 signal input pattern at 230mVrms (-2.5dB) with no noise.
7. Dependant upon Xtal tolerance.
8. $\overline{\text{IRQ}}$ and Reply Data outputs for $V_{SS} < V_{OUT} < V_{DD}$.

Checksum Generation and Checking

Generation

The checksum generator takes the 48 bits from the 6 bytes loaded into the TX Data Buffer and divides them modulo-2 by the generating polynomial:

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted). This 16 bit word is used as the "Checksum."

Checking

The checksum checker does two things:

1) It takes the first 63 bits of a received messge, inverts bit 63, and divides them modulo-2 by the generating polynomial:

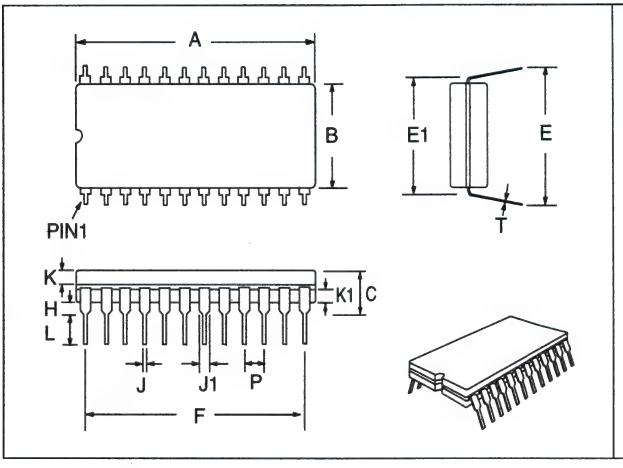
$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

The 15 bits remaining in the polynomial divider are checked to make sure that they are all zero.

2) It generates an even parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64).

If the 15 bits in the polynomial divider are all zero and the two parity bits are equal, then the RX Checksum True (Status Register bit 1) is set.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

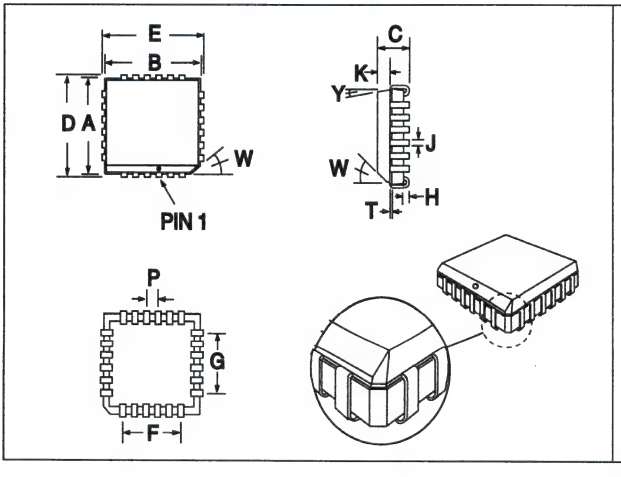


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 24-pin CDIP Mechanical Outline: order as part no. MX809J



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin PLCC Mechanical Outline: order as part no. MX809LH

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480036.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

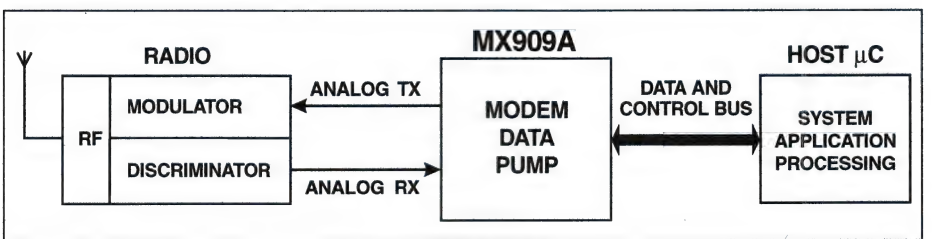
MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX909A Wireless Modem Data Pump

PRELIMINARY INFORMATION

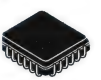
- **GMSK Modulation**
- **RX or TX up to 19.2k bits/sec**
- **Full Data Packet Framing**
- **Mobitex™ Compatible**
- **Flexible Operating Modes**
- **Host μC Interface**
- **Low Power 3.3V/5.0V Operation**
- **24-Pin Small Form Package Option**



AVAILABLE PACKAGES

MX909ADS
24-pin SSOP

MX909ADW
24-pin SOIC



MX909ALH
24-pin PLCC

MX909AP
24-pin PDIP

The MX909A is a low power CMOS device containing all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for a high performance GMSK Wireless Packet Data Modem. The MX909A interfaces with a host μC and radio modulation/demodulation circuits to deliver reliable two-way transfer of application data over a wireless link.

The MX909A assembles application data received from the host μC, adds forward error correction (FEC), and error detection (CRC) codes, time-spreads this data by interleaving (burst-error protection) and scrambles (randomizes) the bit pattern. After automatically adding bit and frame sync codewords, the data packet is converted into analog GMSK signals for modulating into the radio transmitter.

In the receive mode, the MX909A performs the reverse function using the analog signals from the receivers discriminator. After error correction and removal of the packet overhead, the recovered application data is supplied to the host μC. Any CRC detected residual uncorrected errors in the data will be flagged. A readout of the SNR value during receipt of a packet is also provided.

The MX909A uses data block sizes and FEC/CRC algorithms compatible with the Mobitex™ Wide Area Network over-air standard. The format used is suitable for other private applications where the high-speed transfer of data over narrow-band wireless links is required. The MX909A is programmable to operate at standard bit-rates from a wide choice of XTAL/CLOCK frequencies.

©1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054
Doc.# 20480134.002

CONTENTS

Section ..... Page

1. Block Diagram 1-73

2. Signal List 1-74

3. External Components 1-75

4. General Description 1-76
4.1 Description of Blocks 1-76
4.2 Modem - µC Interaction 1-79
4.3 Data Formats 1-79
4.4 The Programmer's View 1-81
4.5 CRC, FEC, Interleaving and Scrambling Information 1-92

5. Application 1-95
5.1 Transmit Frame Example 1-95
5.2 Receive Frame Example 1-96
5.3 Clock Extraction and Level Measurement Systems 1-99
5.4 AC Coupling 1-100
5.5 Radio Performance 1-102

6. Performance Specification 1-103
6.1 Electrical Performance 1-103
6.2 Packaging 1-107

7. Errata 1-109

MX•COM, Inc. Reserves the right to change specifications at any time and without notice.

1. Block Diagram

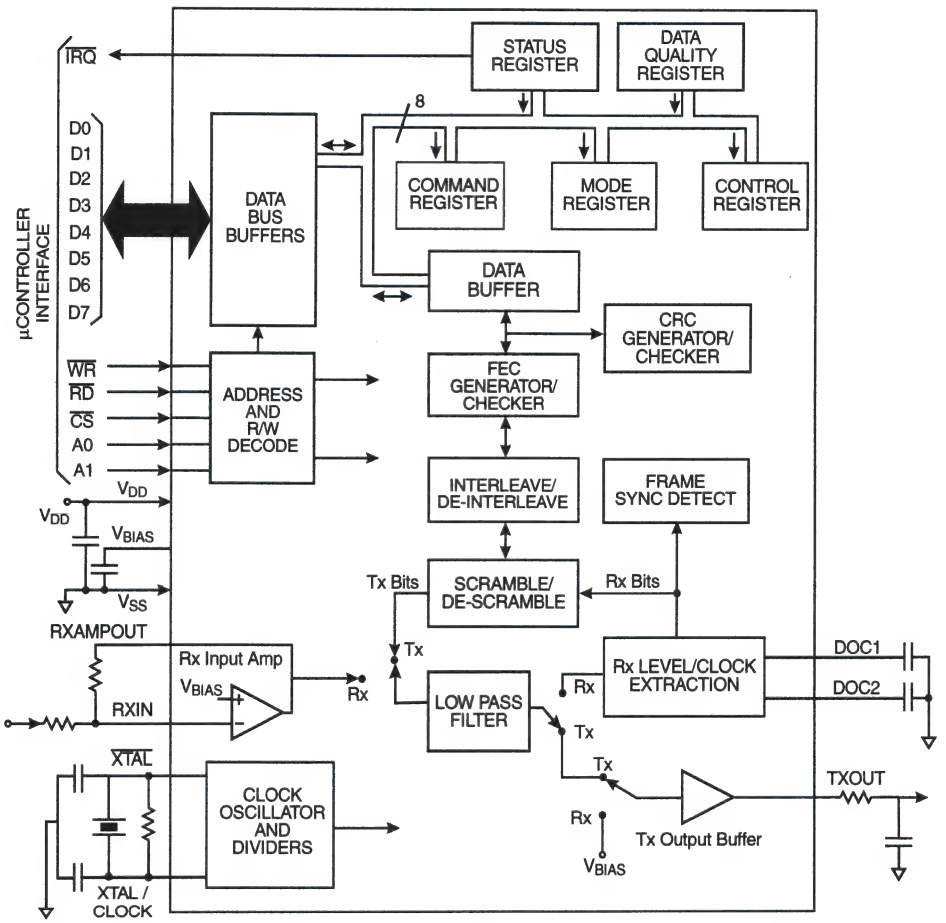


Figure 1: Block Diagram

2. Signal List

Pin No	Signal	Type	Description
1	$\overline{IRQ}$	output	This pin is a 'wire-ORable' output for connection to the host µC's Interrupt Request input. When active, this output has a low impedance pull down to V_{SS}. It has a high impedance when inactive.
2	D7	BUS	Pins 2-9 (D7 - D0) are 8-bit, bi-directional, 3-state µC interface data lines
3	D6	BUS	
4	D5	BUS	
5	D4	BUS	
6	D3	BUS	
7	D2	BUS	
8	D1	BUS	
9	D0	BUS	
10	$\overline{RD}$	input	Read. An active low logic level input used to control the reading of data from the modem into the host µC.
11	$\overline{WR}$	input	Write. An active low logic level input used to control the writing of data into the modem from the host µC.
12	V_{SS}	power	Negative supply. (ground).
13	$\overline{CS}$	input	Chip Select. An active low logic level input to the modem. It is used to enable a data read or write operation.
14	A0	input	Logic level modem register select input.
15	A1	input	Logic level modem register select input.
16	$\overline{XTAL}$	output	Output of the on-chip oscillator.
17	XTAL/CLOCK	input	Input to the on-chip oscillator, for an external CLOCK or XTAL circuit.
18	DOC 2	output	Connects to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}.
19	DOC 1	output	Connects to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}.
20	TXOUT	output	Tx output signal from the modem.
21	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed to V_{SS} by a capacitor mounted close to the device pins.
22	RXIN	input	Input to the Rx input amplifier.
23	RXAMPOUT	output	The output of the Rx input amplifier.
24	V_{DD}	power	Positive supply. Voltage levels are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

©1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054

3. External Components

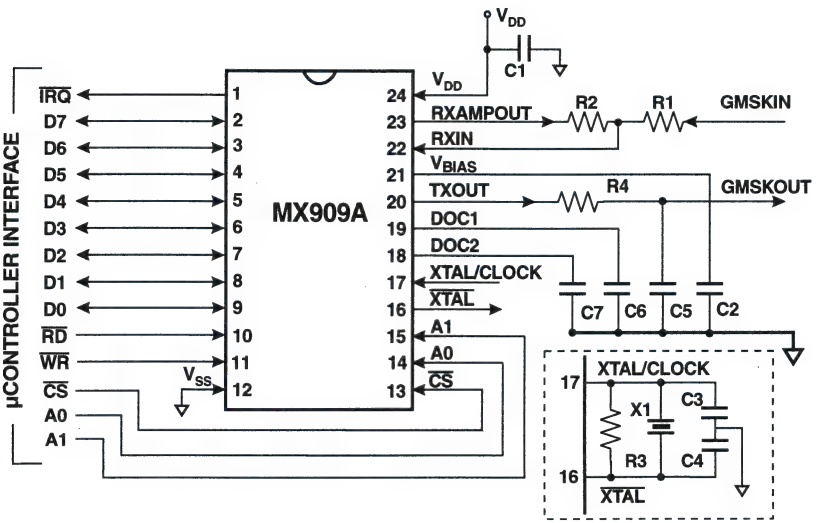


Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1	1		±20%
R2		100kΩ	±10%
R3		1MΩ	±20%
R4	2		±5%
C1		0.1 µF	±20%
C2		0.1 µF	±20%
C3	3		±20%
C4	3		±20%
C5	2		±10%
C6	4		±20%
C7	4		±20%
X1	3		

Recommended External Component Notes:

1. See section 4.1.10 - Rx Input Amp.
2. See section 4.1.12- Tx Output Buffer
3. See section 4.4.3 - Control Register
4. C6 and C7 values should satisfy the following formula:

$$C \text{ (Farads)} = 120 \times 10^{-6} / \text{Data Rate (bits/second)}$$

Data Rate (kbits/sec)	4.0	4.8	8.0	9.6	16.0	19.2
C6 / C7 (uF)	0.03	0.022	0.015	0.012	0.0068	0.0068

©1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054

4. General Description

This product has been designed to be compliant with the appropriate sections of the "Mobitex™ Interface Specification".

4.1 Description of Blocks

4.1.1 Data Bus Buffers

8 bi-directional, 3-state logic level buffers between the modem's internal registers and the host µC's data bus lines.

4.1.2 Address and R/W Decode

This block controls the transfer of data bytes between the µC and the modem's internal registers, according to the state of the Write and Read Enable inputs ($\overline{WR}$ and $\overline{RD}$), the Chip Select input ($\overline{CS}$) and the Register Address inputs A0 and A1.

The Data Bus Buffers, Address and R/W Decode blocks provide a byte-wide parallel µC interface, which can be memory-mapped, as shown in Figure 3.

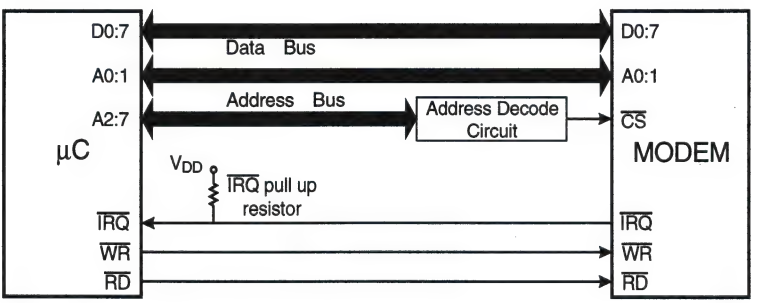


Figure 3: Typical Modem µC Connections

4.1.3 Status and Data Quality Registers

8-bit registers which the µC can read to determine the status of the modem and the received data quality.

4.1.4 Command, Mode and Control Registers

The values written by the µC to these 8-bit registers control the operation of the modem.

4.1.5 Data Buffer

An 18-byte buffer used to hold receive or transmit data to or from the µC.

4.1.6 CRC Generator/Checker

A circuit which generates (in transmit mode) or checks (in receive mode) the Cyclic Redundancy Checksum bits, which are included in transmitted Mobitex™ data blocks so the receive modem can detect transmission errors.

4.1.7 FEC Generator/Checker

In transmit mode this circuit calculates and adds the Forward Error Correction (4 bits) to each byte presented to it. In receive mode the FEC information is used to correct most transmission errors that have occurred in a Mobitex™ Data Block or in the Frame Head control bytes.

4.1.8 Interleave / De-interleave Buffer

This circuit interleaves data bits within a data block before transmission and de-interleaves the received data block so the FEC system is best able to handle short noise bursts or signal fades.

4.1.9 Frame Sync Detect

This circuit, (only active in receive mode), is used to look for the user specified 16-bit Frame Synchronization pattern which is transmitted to mark the start of every frame.

4.1.10 Rx Input Amp

This amplifier allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components R1 and R2. The value of R1 should be calculated to give (0.2 x V_{DD})V_{P-P} at the RXAMPOUT pin for a received '...11110000...' sequence.

A capacitor may be fitted if ac coupling of the received signal is desired (see section 5.4- AC Coupling), otherwise the dc level of the received signal should be adjusted so that the signal at the modem's RXAMPOUT pin is centered around V_{BIAS} (V_{DD}/2).

4.1.11 Tx/Rx Low Pass Filter

This filter, which is used in both transmit and receive modes, is a low pass transitional Gaussian filter having a loss of 3dB at 0.3 times the selected bit rate (BT = 0.3). See Figure 4.

In transmit mode, the bits are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

In receive mode this filter is used with an increased BT factor (0.56) to reject HF noise, so the signal is suitable for extraction of the received data.

4.1.12 Tx Output Buffer

This is a unity gain amplifier used in transmit mode to buffer the output of the Tx low pass filter. In receive mode, the input of this buffer is connected to V_{BIAS}. When changing from Rx to Tx mode the input to this buffer will be connected to V_{BIAS} for 2 bit periods to prevent unwanted signals, from the low pass filter, at the output. When the modem is set to powersave mode, the buffer is turned off and the TXOUT pin connected to V_{BIAS} via a high value resistance. When exiting from power save mode the Tx output is only reconnected to the buffer after 2 bit periods, to prevent unwanted signals, from the low pass filter, at the output.

Note: The RC low pass filter formed by the external components R4 and C5 between the Tx Output Buffer and the input to the radio's frequency modulator forms an important part of the transmit signal filtering. These components may form part of any dc level-shifting and gain adjustment circuitry. The ground connection to the capacitor C5 should be positioned to give maximum attenuation of high frequency noise into the modulator. R4 and C5 should be chosen so that the product of the resistance of R4 and capacitance of C5 is 0.34/bit rate (bit rate in bits per second). R4 should be not less than 47kΩ and the value used for the external capacitor should take into account parasitic capacitance.

Suitable values being:

	R4	C5
8000 bits/sec	100kΩ	430pF
4800 bits/sec	100kΩ	710pF

The signal at the TXOUT pin is centered around V_{BIAS} and is approx. (0.2 x V_{DD})V_{P-P}, going positive for a logic '1' and negative for a logic '0', if the modem is not inverting the Tx data.

A capacitor may be fitted if ac coupling of the input to the frequency modulator is desired, see section 5.4 -AC Coupling.

The 'eye' diagram of the transmitted signal (after the external R4/C5 network) is shown in Figure 5.

©1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054

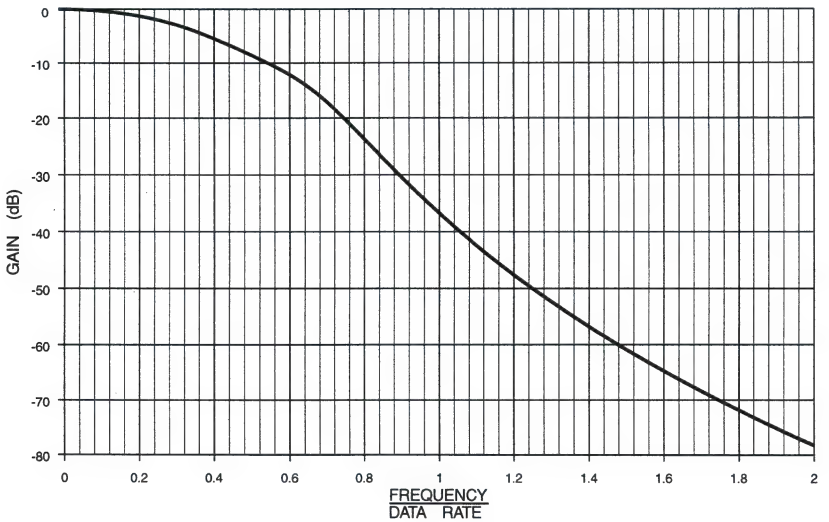


Figure 4: Typical Tx Filter Frequency Response (after the external RC Filter)

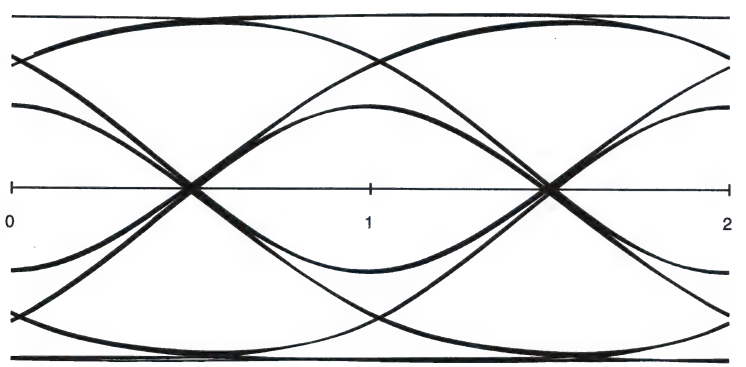


Figure 5: Transmitted Eye Signal Diagram (after the external RC Filter)

4.1.13 Rx Level/Clock Extraction

These circuits, which operate only in receive mode, extract a bit rate clock from the received signal and measure the received signal amplitude and dc offset. This information is then used to extract the received bits and also to provide an input to the received Data Quality measuring circuit. The external capacitors C6 and C7 form part of the received signal level measuring circuit.

4.1.14 Clock Oscillator and Dividers

This circuit derives the transmit bit rate (and the nominal receive bit rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or applied from an external source.

Note: If the on-chip Xtal oscillator is to be used, then the external components X1, C3, C4 and R3 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin, the $\overline{\text{XTAL}}$ pin should be left unconnected, and X1, C3, C4 and R3 not fitted.

4.1.15 Scramble/De-scramble

This block may be used to scramble/de-scramble the transmitted/received data blocks. It does this by modulating the data with a 511-bit pseudorandom sequence, as described in section 4.5.4.-Scrambling smoothes the transmitted spectrum, especially when repetitive sequences are to be transmitted.

4.2 Modem - µC Interaction

In general, data is transmitted over air in the form of messages, or 'Frames', consisting of a 'Frame Head' optionally followed by one or more formatted data blocks. The Frame Head includes a Frame Synchronization pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (Cyclic Redundancy Checksum) generation, Forward Error Correction coding, Interleaving and Scrambling. Details of the message formats handled by this modem are given in section 4.3- Data Formats.

To reduce the processing load on the host µC, this modem has been designed to perform as much as possible of the computationally intensive work involved in Frame formatting / de-formatting and (when in receive mode) in searching for and synchronizing onto the Frame Head. In normal operation the modem will only require servicing by the µC once per received or transmitted data block.

Thus, to transmit a block, the host µC has only to load the unformatted (raw) binary data into the modem's data buffer then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result with Forward Error Correction coding, interleave then scramble the bits before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received bits, de-scramble and de-interleave the bits, check and correct them (using the FEC coding) and check the resulting CRC before placing the received binary data into the Data Buffer for the µC to read.

The modem can also handle the transmission and reception of unformatted data, to allow the transmission of special Bit and Frame Synchronization sequences or test patterns.

4.3 Data Formats

4.3.1 General Purpose Formats

In a proprietary system the user may employ the data elements provided by this device to construct a custom, over-air data structure.

For example, 16 bits of bit sync + 2 bytes of frame sync + 4 bytes of receiver and sender address + n data blocks would be: transmitted as:

TQB (bit and frame sync) + TQB (addresses) + (n x TDB) + TSB

received as:

SFS + RSB + RSB + RSB + RSB + (n x RDB)

Note: It is important to have established frame Synchronization before receiving data to enable the receiving device to decode synchronously. The user may add, by way of algorithms performed on the controlling device, additional data correction with the bytes in the data block task.

4.3.2 Mobitex™ Frame Structure

The Mobitex™ format for transmitted data is in the form of a Frame Head immediately followed by a number of Data Blocks (0 to 32).

The Frame Head consists of 7 bytes:

2 bytes of bit sync:

1100110011001100 from base,
0011001100110011 from mobile
bits are transmitted from left to right

Mobitex™ Frame Structure cont...

2 bytes of frame sync:
System specific.
2 bytes of control data.
1 byte of FEC code, 4 bits for each of the control bytes:
bits 7-4 (leftmost) operate on the first control byte.
bits 3-0 (rightmost) operate on the second control byte.
Each byte in the Frame Head is transmitted bit 7 (MSB) first to bit 0 (LSB) last.

The Data Block consists of:

18 bytes of data.
2 bytes of CRC calculated from the 18 data bytes.
4 bits of FEC code for each of the data and CRC bytes
The resulting 240 bits are interleaved and scrambled before transmission.

The over air signal is composed of Frame Sync and Bit Sync patterns, Control bytes, and Data Blocks as shown in Figure 6.

The binary data transferred between the modem and the host µC is shown in the Frame Head and Data Block of Figure 6 as shaded areas.

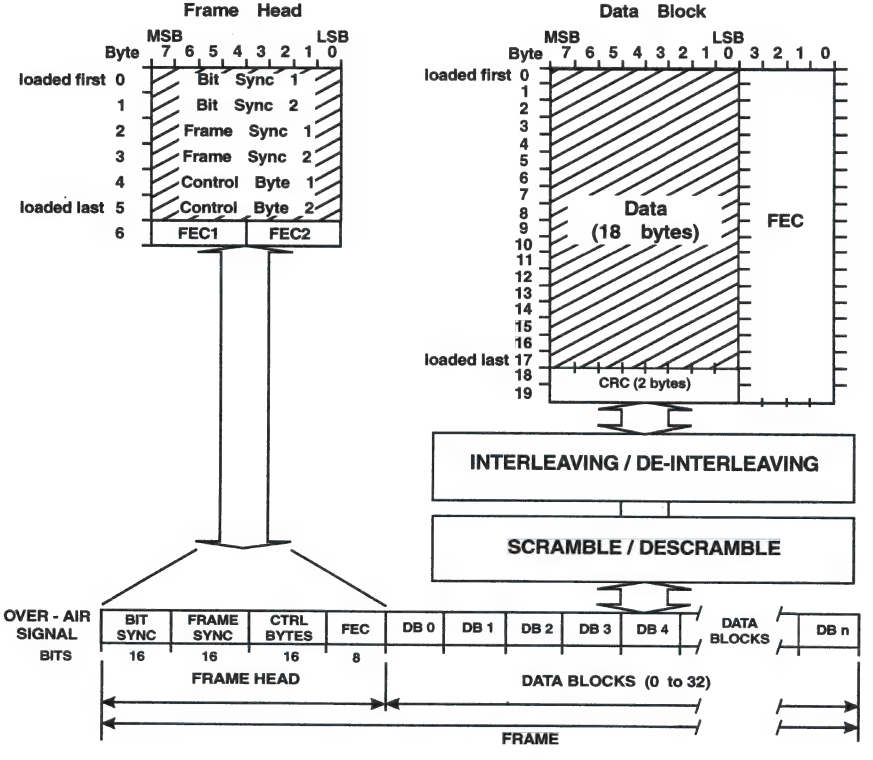


Figure 6: Mobitex™ Over Air Signal Format

4.4 The Programmer's View

The modem appears to the programmer as 4 write only 8-bit registers shadowed by 3 read only registers, individual registers being selected by the A0 and A1 chip inputs:

A1	A0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	Data Quality Register
1	1	Mode Register	not used

4.4.1 Data Buffer

This is an 18-byte read/write buffer which is used to transfer data (as opposed to command, status, mode, data quality and control information) between the modem and the host µC.

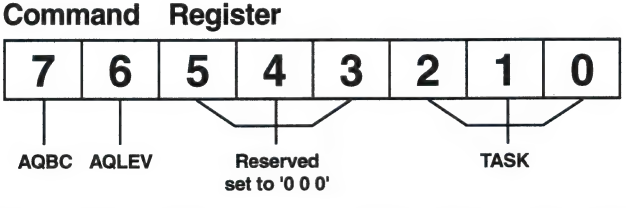
It appears to the µC as a single 8-bit register; the modem ensuring that sequential µC reads or writes to the buffer are routed to the correct locations within the buffer.

The µC should only access this buffer when the Status Register BFREE (Buffer Free) bit is '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode (except when loading Frame Sync detection bytes while in Rx mode).

4.4.2 Command Register

Writing to this register tells the modem to perform a specific action or actions, depending on the setting of the TASK, AQLEV and AQBC bits.



When there is no action to perform and not 'powersaved', the modem will be in an 'idle' state. If the modem is in transmit mode the input to the Tx filter will be connected to V_{BIAS}. In receive mode the modem will continue to measure the received data quality and extract bits from the received signal, supplying them to the de-interleave buffer, otherwise the received data is ignored.

4.4.2.1 Command Register B7: AQBC - Acquire Bit Clock

This bit has no effect in transmit mode.

In receive mode, when a byte with AQBC bit set to '1' is written to the Command Register, and TASK is not set to RESET, it initiates an automatic sequence designed to achieve bit timing Synchronization with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing Synchronization is achieved, until the 'normal' value set by the PLLBW bits of the Control Register is reached.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however note that the acquisition sequence will be re-started every time that a byte written to the Command Register has the AQBC bit set to '1'.

The AQBC bit will normally be set up to 12 bits before an SFS (Search for Frame Sync) or SFH (Search for Frame Head) task, however it may also be used independently to re-establish clock Synchronization quickly after a long fade. Alternatively, an SFS or SFH task may be written to the Command Register with the AQBC bit '0' if it is known that clock Synchronization does not need to be re-established. More details of the bit clock acquisition sequence are given in section 5.3-Clock Extraction and Level Measurement Systems.

4.4.2.2 Command Register B6: AQLEV - Acquire Receive Signal Levels

This bit has no effect in transmit mode.

In receive mode, when a byte with AQLEV bit set to '1' is written to the Command Register and TASK is not set to RESET, it initiates an automatic sequence designed to measure the amplitude and dc offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then

Command Register B6: AQLEV - Acquire Receive Signal Levels (cont...)

gradually increasing their response time, thereby improving the measurement accuracy, until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however the acquisition sequence will be re-started every time a byte written to the Command Register has the AQLEV bit set to '1'.

The AQLEV bit will normally be set up to 12 bits before an SFS (Search for Frame Sync) or SFH (Search for Frame Head) task is initiated, however it may also be used independently to re-establish signal levels quickly after a long fade. Alternatively, an SFS or SFH task may be written to the Command Register with the AQLEV bit at '0' if it is known that there is no need to re-establish the received signal levels. Further information of the level measurement acquisition sequence is provided in section 5.3 - Clock Extraction and Level Measurement Systems.

The error rate is highest immediately after an AQBC and AQLEV sequence is triggered and rapidly reduces to its static value soon after. These erroneous bits could incorrectly trigger the frame sync detection circuits. It is suggested that an SFH or SFS task be set 12 bits after setting either of the AQLEV or AQBC sequences.

4.4.2.3 Command Register B5, B4, B3

These bits should be set to '0'.

4.4.2.4 Command Register B2, B1, B0: TASK - Task

Operations such as transmitting a data block are treated by the modem as 'tasks' and are initiated when the µC writes a byte to the Command Register with the TASK bits set to anything other than the 'NULL' code.

The µC should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is '0'.

Different tasks apply in receive and transmit modes.

When the modem is in transmit mode, all tasks other than NULL, RESET and TSO instruct the modem to transmit data from the Data Buffer, formatting it as required. For these tasks the µC should wait until the BFREE (Buffer Free) bit of the Status Register is '1', before writing the data to the Data Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Buffer, byte number 0 of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE (Buffer Free) bit of the Status Register to '0'.

Take the data from the Data Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

Once all of the data has been transferred from the Data Buffer the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the chip $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may write new data and the next task to the modem.

In this way the µC can write a task and the associated data to the modem while the modem is still transmitting the data from the previous task. See Figure 7.

When the modem is in receive mode, the µC should wait until the BFREE bit of the Status Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to '0'.

Wait until enough received bits are in the De-interleave Buffer.

Decode them as needed, and transfer any resulting data to the Data Buffer

Then the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may read from the Data Buffer and write the next task to the modem. If more than 1 byte is contained in the Data Buffer, byte number '0' of the data will be read first.

In this way the µC can read data and write a new task to the modem while the received bits needed for this new task are being stored in the De-interleave Buffer. See Figure 8.

The above is not true for loading the Frame Sync detection bytes (LFSB): the bytes to be compared with the incoming data must be loaded prior to the task bits being written.

Detailed timings for the various tasks are given in Figure 9 and Figure 10.

©1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054

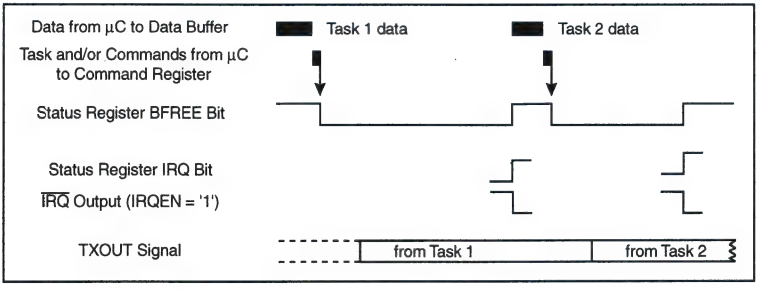

Data from µC to Data Buffer
Task 1 data
Task 2 data
Task and/or Commands from µC to Command Register
Status Register BFREE Bit
Status Register IRQ Bit
IRQ Output (IRQEN = '1')
TXOUT Signal
from Task 1
from Task 2

Figure 7: Transmit Process

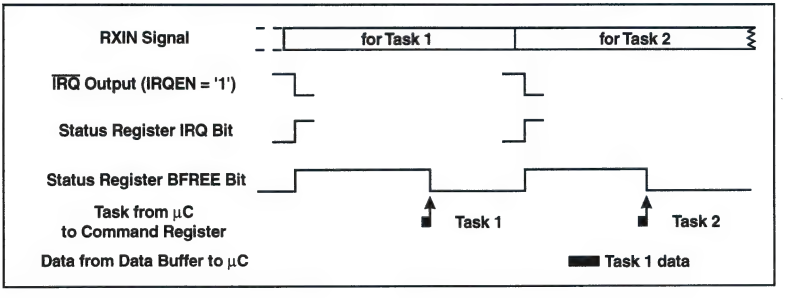


Figure 8: Receive Process

Mobitex™ Modem Tasks

B2	B1	B0	Receive Mode		Transmit Mode	
0	0	0	NULL		NULL	
0	0	1	SFH	Search for Frame Head	T7H	Transmit 7 byte Frame Head
0	1	0	R3H	Read 3 byte Frame Head		Reserved
0	1	1	RDB	Read Data Block	TDB	Transmit Data Block
1	0	0	SFS	Search for Frame Sync	TQB	Transmit 4 Bytes
1	0	1	RSB	Read Single Byte	TSB	Transmit Single Byte
1	1	0	LFSB	Load Frame Sync Bytes	TSO	Transmit Scrambler Output
1	1	1	RESET	Cancel any current action	RESET	Cancel any current action

4.4.2.5 NULL - No effect

This task is provided so that a AQBC or AQLEV command can be initiated without loading a new task.

4.4.2.6 SFH - Search for Frame Head

Causes the modem to search the received signal for a Frame Head. The Frame Head will consist of a 16-bit Frame Sync followed by control data (see Figure 6). The search will continue until a Frame Head has been found, or until the RESET task is loaded.

SFH - Search for Frame Head cont...

The search is carried out by first attempting to match the incoming bits against the previously programmed (task LFSB) 16-bit Frame Sync pattern (allowing up to any one bit (of 16) in error). When a match has been found, the modem will read the next 3 received bytes as Frame Head bytes, these bytes will be checked, and corrected if necessary, using the FEC bits. The two Frame Head Data bytes are then placed into the Data Buffer.

The BFREE and IRQ bits of the Status Register will then be set to a logic '1' to indicate that the µC may read the 2 Frame Head Data bytes from the Data Buffer and write the next task to the Command Register. If the FEC indicates uncorrectable errors the modem will set the CRCFEC bit in the Status Register to a logic '1'. The MO/$\overline{BA}$ bit (Mobile or Base) in the Status Register will be set according to the polarity of the 3 bits preceding the Frame Sync pattern.

4.4.2.7 R3H - Read 3-byte Frame Head

This task, which would normally follow an SFS task, will place the next 3 bytes directly into the Data Buffer. It also causes the modem to check the 3 bytes as Frame Head control data bytes and will set the CRCFEC bit to a logic '1' only if the FEC bits indicate uncorrectable errors.

Note: This task will not correct any errors and, due to the Mobitex™ FEC specification, will not detect all possible uncorrectable error patterns. The BFREE and IRQ bits of the Status Register will be set to '1' when the task is complete to indicate that the µC may read the data from the Data Buffer and write the next task to the modem's Command Register.

The CRCFEC bit in the Status Register will be set according to the validity of the received FEC bits.

4.4.2.8 RDB - Read Data Block

This task causes the modem to read the next 240 bits as a Mobitex™ Data Block.

It will de-scramble and de-interleave the bits, FEC correct and CRC check the resulting 18 data bytes and place them into the Data Buffer, setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete to indicate that the µC may read the data from the Data Buffer and write the next task to the modem's Command Register. The CRCFEC bit will be set according to the outcome of the CRC check.

Note: In receive mode the CRC checksum circuits are initialized on completion of any task other than NULL.

4.4.2.9 SFS - Search for Frame Sync

This task, which is intended for special test and channel monitoring purposes, performs the first part only of a SFH task. It causes the modem to search the received signal for a 16-bit sequence which matches the Frame Synchronization pattern with up to any 1 bit in error.

When a match is found the modem will set the BFREE and IRQ bits of the Status Register to '1' and update the MO/$\overline{BA}$ bit. The µC may then write the next task to the Command Register.

4.4.2.10 RSB - Read Single Byte

This task causes the modem to read the next 8 bits and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Buffer (B7 will represent the earliest bit received). The BFREE and IRQ bits of the Status Register will then be set to '1' to indicate that the µC may read the data byte from the Data Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by an SFS task.

4.4.2.11 LFSB - Load Frame Sync Bytes

This task takes 2 bytes from the Data Buffer and updates the Frame Sync detect bytes. The MSB of byte '0' is compared to the first bit of a received Frame Sync pattern and the LSB of byte '1' is compared to the last bit of a received Frame Sync pattern. This task does not enable Frame Sync detection.

Unlike other Rx tasks, the data buffer must be loaded before the task is issued and the task must only be issued 'between' received messages, i.e. before the first task for receiving a message and after the last data is read out of the data buffer.

Once the modem has read the Frame Sync bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task to the modem.

4.4.2.12 T7H - Transmit 7-byte Frame Head

This task takes 6 bytes of data from the Data Buffer, calculates and appends 8 bits of FEC from bytes '4' and '5' then transmits the result as a complete Mobitex™ Frame Head.

Bytes '0' and '1' form the bit sync pattern, bytes '2' and '3' form the frame sync pattern and bytes '4' and '5' are the frame head control bytes. Bit 7 of byte '0' of the Data Buffer is sent first, bit 0 of the FEC byte last.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

©1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054

4.4.2.13 TQB - Transmit 4 Bytes

This task takes 4 bytes of data from the Data Buffer and transmits them, bit 7 first.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

4.4.2.14 TDB - Transmit Data Block

This task takes 18 bytes of data from the Data Buffer, calculates and applies a 16-bit CRC and forms the FEC for the 18 data bytes and the CRC. This data is then interleaved and passed through the scrambler, if enabled, before being transmitted as a Mobitex™ Data Block.

Once the modem has read the data bytes from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

Note: In transmit mode the CRC checksum circuit is initialized on completion of any task other than NULL.

4.4.2.15 TSB - Transmit Single Byte

This task takes a byte from the Data Buffer and transmits the 8 bits, bit 7 first.

Once the modem has read the data byte from the Data Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the next task and its data to the modem.

4.4.2.16 TSO - Transmit Scrambler Output

This task, intended for channel set-up, enables the scrambler and transmits its output.

When the modem has started the task, the Status Register bits will not be changed and an IRQ will not be raised. The µC may write the next task and its data to the modem at any time and the scrambler output will stop when the new task has produced its first data.

4.4.2.17 RESET - Stop any current action

This task takes effect immediately, and terminates any current action (task, AQBC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to '1', without setting the IRQ bit. It should be used when V_{DD} is applied to set the modem into a known state.

Note: Due to delays in the internal switched capacitor filter, it will take approximately 3 bit times for any change to become apparent at the TXOUT pin.

4.4.2.18 Task Timings

The device should not be given a new task for at least 2 bit times after the following:

Changing from powersave state to normal operation.

Changing the Tx/$\overline{Rx}$ bit.

Resetting or after power is applied to the device.

This is to ensure that the internal operation of the device is initialized correctly for the new task.

Note: This only applies to the Command Register, other registers may be accessed as normal.

Ref. Figure 9 and Figure 10		Task	Typical (bit-times)
t_1	Time from writing first task (modem in 'idle' state) to application of first transmit bit to Tx Low Pass filter	Any	1
t_2	Time from application of first bit of task to TX Low Pass Filter until BFREE goes to a logic 1	T7H TQB TDB TSB	36 24 20 1
t_3	Time to transmit all bits of task	T7H TQB TDB TSB	56 32 240 8
t_4	Max time allowed from BFREE going to a logic 1 for next task (and data) to be written to the modem	T7H TQB TDB TSB	18 6 218 6
t_5	Time to receive all bits of task	SFH R3H RDB RSB	56 24 240 8
t_6	Maximum time between first bit of task entering de-interleave circuit and task being written to modem	SFH R3H RDB RSB	14 18 218 6
t_7	Time from last bit of task entering de-interleave circuit to BFREE going to a logic '1'	Any	1

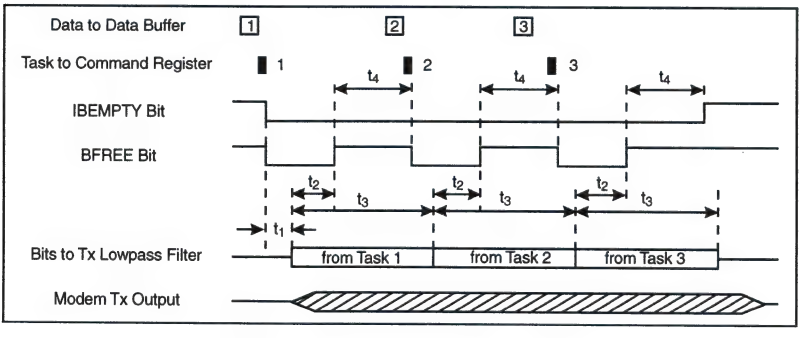


Figure 9: Transmit Mode Timing Diagram

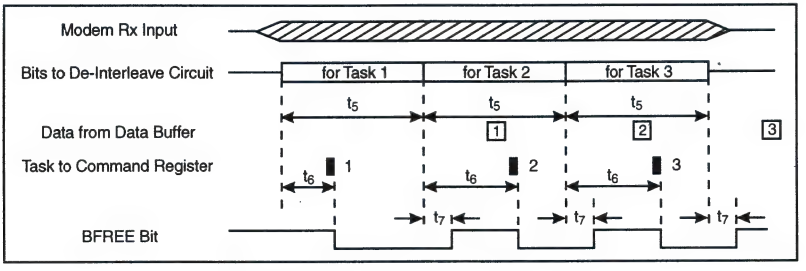


Figure 10: Receive Mode Timing Diagram

4.4.2.19 Tx/Rx Low Pass Filter Delay

The previous task timing figures are based on the signal at the input to the Tx Low Pass filter (in transmit mode) or the input to the de-interleave buffer (in receive mode). There is an additional delay of about 2 bit times in both transmit and receive modes due to the Tx/Rx Low Pass filter, as illustrated in Figure 11.

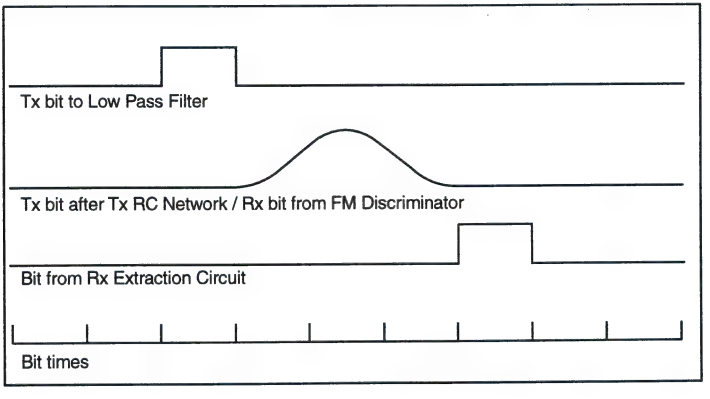
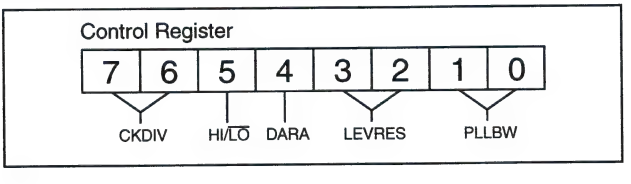


Figure 11: Low Pass Filter Delay

4.4.3 Control Register

This 8-bit write only register controls the modem's bit rate, the response times of the receive clock extraction and signal level measurement circuits and the internal analog filters.



4.4.3.1 Control Register B7, B6: CKDIV - Clock Division Ratio and B5: HI/$\overline{LO}$ - Xtal Range Selection

These bits control a frequency divider driven from the clock signal present at the $\overline{XTAL}$ pin, which determines the nominal bit rate. The table below shows how bit rates of 4000/8000/16000 or 4800/9600/19200 bits/sec may be obtained from common Xtal frequencies:

		B5		XTAL / CLOCK Frequency (MHz)					
		1		8.192	9.8304	4.096 (12.288/3)	4.9152	2.048 (6.144/3)	2.4576 (12.288/5)
			0	4.096 (12.288/3)	4.9152	2.048 (6.144/3)	2.4576 (12.288/5)	1.024	1.2288
B7	B6	Division Ratio XTAL Frequency Data Rate		Data Rates (bits per second)					
0	0	256	128			16000	19200	8000	96000
0	1	512	256	16000	19200	8000	9600	4000	4800
1	0	1024	512	8000	9600	4000	4800		
1	1	2048	1024	4000	4800				

Note: Device operation is not guaranteed below 4000 or above 19200 bits/sec.

The values used for C3 and C4 should be suitable for the frequency of the crystal X1. As a guide; C3 = C4 = 33pF for X1 < 5MHz, and C3 = C4 = 18pF for X1 > 5MHz.

4.4.3.2 Control Register B4: DARA - Data Rate

This bit operates in both transmit and receive modes, optimizing the modem's internal signal filtering according to the relevant bit rate.

If the bit rate used is above 10k bits/sec then this bit should be set to '1' , if not, then it should be set to '0'.

4.4.3.3 Control Register B3, B2: LEVRES - Level Measurement Response Time

These two bits have no effect in transmit mode.

In receive mode, they set the 'normal' response time of the Rx signal amplitude and dc offset measuring circuits. This setting will be temporarily overridden by the automatic sequencing of an AQLEV command.

B3	B2		
0	0	Hold	Keep current values of amplitude and offset
0	1	Peak Averaging	Track input signal using bit peak averaging
1	0	Peak Detect	Track input signal using peak detect
1	1	Lossy Peak Detect	Track input signal using lossy peak detection

For Mobitex™ systems, and most general purpose applications using the modem, these bits should normally be set to 'Peak Averaging', except when the µC detects a receive signal fade, when 'Hold' should be selected.

The 'Lossy Peak Detect' setting is intended for systems where the µC cannot detect signal fades or the start of a received message, as it allows the modem to respond quickly to fresh messages and recover rapidly after a fade without µC intervention - although at the cost of reduced Bit Error Rate versus Signal to Noise performance.

Note: Since the measured levels are stored on the external capacitors C6 and C7, they will decay gradually towards V_{BIAS} when the 'Hold' setting is chosen, the discharge time-constant being approximately 2000 bit times. Further information of the level measurement system is provided in section 5.3 - Clock Extraction and Level Measurement Systems.

4.4.3.4 Control Register B1, B0: PLLBW

These two bits have no effect in transmit mode.

In receive mode, they set the 'normal' bandwidth of the Rx clock extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the automatic sequencing of an AQBC command.

©1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054

B1	B0	PLL Bandwidth	Suggested use
0	0	Hold	Signal fades
0	1	Narrow	± 20ppm or better Xtals
1	0	Medium	Wide tolerance Xtals or long preamble acquisition
1	1	Wide	Quick acquisition

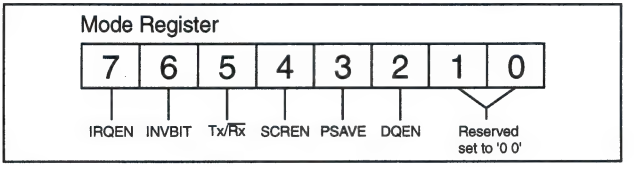
The 'hold' setting is intended for use during signal fades, otherwise the minimum bandwidth consistent with the transmit and receive modem bit rate tolerances should be chosen.

The wide and medium bandwidth settings are intended for systems where the µC cannot detect signal fades or the start of a received message, as they allow the modem to respond rapidly to fresh messages and recover rapidly after a fade without µC intervention - although at the cost of reduced Bit Error Rate versus Signal to Noise performance.

Note: Further information of the clock extraction system is provided in section 5.3 - Clock Extraction and Level Measurement Systems.

4.4.4 Mode Register

The contents of this 8-bit write only register control the basic operating modes of the modem:



4.4.4.1 Mode Register B7: IRQEN- $\overline{IRQ}$ Output Enable

When this bit is set to '1', the $\overline{IRQ}$ chip output pin is pulled low (to V_{SS}) whenever the IRQ bit of the Status Register is a '1'.

4.4.4.2 Mode Register B6: INVBIT - Invert Bits

This bit controls inversion of transmitted and received bit voltages. When set to '1' all data is inverted in the Tx and Rx data paths so a transmitted '1' is a voltage below V_{BIAS} at the TXOUT pin and a received '0' is a voltage above V_{BIAS} at the RXIN pin. Data will be inverted immediately after this bit is set to '1'.

4.4.4.3 Mode Register B5: TX/$\overline{RX}$ - Tx/Rx Mode

Setting this bit to '1' puts the modem into Transmit mode, clearing it to '0' puts the modem into Receive mode. When changing from Rx to Tx there must be a 2-bit pause before setting a new task to allow the filter to stabilize. (See also PSAVE bit).

Note: Changing between receive and transmit modes will cancel any current task

4.4.4.4 Mode Register B4: SCREN - Scramble Enable

The scrambler only takes effect during the transmission or reception of a Mobitex™ Data Block and during a TSO task. Setting this bit to '1' enables scrambling, clearing it to '0' disables scrambling.

The scrambler is only operative, if enabled by this control bit, during TSO, RDB or TDB, it is held in a reset state at all other times.

This bit should not be changed while the modem is decoding or transmitting a Mobitex™ Data Block.

4.4.4.5 Mode Register B3: PSAVE - Powersave

When this bit is a '1', the modem will be in a 'powersave' mode in which the internal filters, the Rx bit and Clock extraction circuits and the Tx output buffer will be disabled, and the TXOUT pin will be connected to V_{BIAS} through a high value resistance. The Xtal Clock oscillator and the µC interface logic will continue to operate.

Setting the PSAVE bit to '0' restores power to all of the chip circuitry.

Note: The internal filters will take approximately 2 bit times to settle after the PSAVE bit is taken from '1' to '0'.

4.4.4.6 Mode Register B2: DQEN - Data Quality IRQ Enable

In receive mode, setting this bit to '1' causes the IRQ bit of the Status Register to be set to '1' whenever a new Data Quality reading is ready. (The DQRDY bit of the Status Register will also be set to '1' at the same time.)

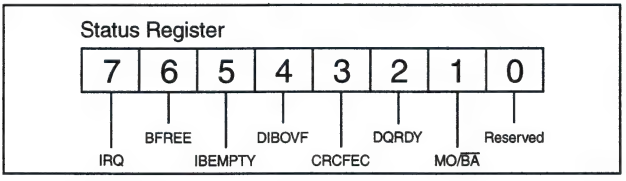
In transmit mode this bit has no effect.

4.4.4.7 Mode Register B1, B0

These bits should be set to '0'.

4.4.5 Status Register

This register may be read by the µC to determine the current state of the modem.



4.4.5.1 Status Register B7: IRQ - Interrupt Request

This bit is set to '1' by:

The Status Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register PSAVE or TX/$\overline{RX}$ bits.

The Status Register IBEMPTY bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register PSAVE or TX/$\overline{RX}$ bits.

The Status Register DQRDY bit going from '0' to '1' (If DQEN = '1').

The Status Register DIBOVF bit going from '0' to '1'.

The IRQ bit is cleared to '0' immediately after a read of the Status Register.

If the IRQEN bit of the Mode Register is '1', then the chip $\overline{IRQ}$ output will be pulled low (to V_{SS}) whenever the IRQ bit is '1'.

4.4.5.2 Status Register B6: BFREE - Data Buffer Free

This bit reflects the availability of the Data Buffer and is cleared to '0' whenever a task other than NULL, RESET or TSO is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status Register IRQ bit to '1') by the modem when the modem is ready for the µC to write new data to the Data Buffer and the next task to the Command Register.

In receive mode, the BFREE bit is set to '1' (also setting the Status Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1', but without setting the IRQ bit, by a RESET task or when the Mode Register PSAVE or TX/$\overline{RX}$ bits are changed.

4.4.5.3 Status Register B5: IBEMPTY - Interleave Buffer Empty

In transmit mode, this bit will be set to '1', also setting the IRQ bit, when less than two bits remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

The bit is also set to '1' by a RESET task or by a change of the Mode Register TX/$\overline{RX}$ or PSAVE bits, but in these cases the IRQ bit will not be set.

The bit is cleared to '0' by writing a task other than NULL, RESET or TSO to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid-level voltage (V_{BIAS}) will be applied to the Tx low pass filter.

In receive mode this bit will be '0'.

4.4.5.4 Status Register B4: DIBOVF - De-Interleave Buffer Overflow

In receive mode this bit will be set to '1' (also setting the IRQ bit) when a task is written to the Command Register too late to allow continuous reception.

The bit is cleared to '0' by reading the Status Register or by writing a RESET task to the Command Register or by changing the PSAVE or TX/$\overline{RX}$ bits of the Mode Register.

In transmit mode this bit will be '0'.

4.4.5.5 Status Register B3: CRCFEC - CRC or FEC Error

In receive mode this bit will be updated at the end of a Mobitex™ Data Block task, after checking the CRC, and at the end of receiving Frame Head control bytes, after checking the FEC. A '0' indicates that the CRC was received correctly or the FEC did not find uncorrectable errors, a '1' indicates that errors are present.

The bit is cleared to '0' by a RESET task or by changing the PSAVE or TX/$\overline{RX}$ bits of the Mode Register.

In transmit mode this bit will be '0'.

4.4.5.6 Status Register B2: DQRDY - Data Quality Reading Ready

In receive mode, this bit is set to '1' whenever a Data Quality reading has been completed. See section 4.4.6 - Data Quality Register.

The bit is cleared to '0' by a read of the Data Quality Register.

Immediately after a RESET task, or a change in the PSAVE or TX/$\overline{RX}$ bits to '0', the DQRDY bit may be set and generate an interrupt. The value in the Data Quality Register will not be valid in this case.

4.4.5.7 Status Register B1: MO/$\overline{BA}$ - Mobile or Base Bit Sync Received

In receive mode this bit is updated at the end of the SFS and SFH tasks. This bit is set to '1' whenever the 3 bits immediately preceding a detected Frame sync are '011' (received left to right), with up to any one bit in error. The bit is set to '0' if the bit pattern is '100', again with up to any one bit in error. Thus, if this bit is set to '1' then the received message is likely to have originated from a Mobile and if it is set to '0' from a Base Station. See section 4.3- Data Formats

In transmit mode this bit is a logic '0'.

4.4.5.8 Status Register B0

This bit will always be set to '0'.

4.4.6 Data Quality Register

This is intended to indicate the quality of the receive signal during a Mobitex™ Data Block or 30 single bytes. In receive mode, the modem measures the 'quality' of the received signal by comparing the actual received zero crossing time against an internally generated time. This value is averaged over 240 bits and at the end of the measurement the Data Quality Register and the DQRDY bit in the Status Register is updated.

Note: An interrupt will only occur at this time if the DQEN bit = '1'.

To provide Synchronization with Data Blocks, and to ensure the Data Quality Register is updated in preparation to be read when the RDB task finishes, the measurement process is reset at the end of tasks SFH, SFS, RDB and R3H.

In transmit mode all bits of the Data Quality Register will be '0'.

Figure 12 shows how the value (0-240) read from the Data Quality Register varies with received signal to noise ratio.

©1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054

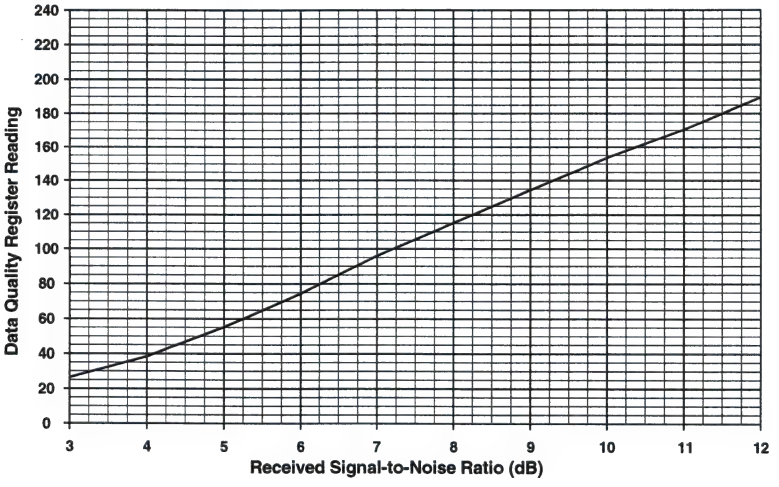


Figure 12: Typical Data Quality Reading (after 240 bits) vs. S/N, (noise in bit rate bandwidth)

4.5 CRC, FEC, Interleaving and Scrambling Information

4.5.1 CRC

This is a 16-bit CRC code used in the Mobitex™ Data Block. In transmit it is calculated by the modem from the 18 data bytes using the following generator polynomial:

$$g(x) = x^{16} + x^{12} + x^5 + 1$$

i.e. CRC - CCITT X.25.

This code detects all (single) error bursts of up to 16 bits in length and about 99.998% of all other error patterns.

The CRC register is initialized to all '1s' and the CRC is calculated octet by octet starting with the least significant bit of 'byte 0'. The CRC calculated is bit-wise inverted and appended to the data bytes with the most significant bit transmitted earliest.

In receive mode, a 16-bit CRC code is generated from the 18 data bytes of each Mobitex™ Data Block as above and the bit-wise inverted value is compared with the received CRC bytes. If a mismatch is present, then an error has been detected.

4.5.2 FEC

In transmit mode, during T7H and TDB, the modem generates a 4-bit Forward Error Correction code for each coded byte. The FEC is defined by the following H matrix:

	7_____0	3___0
	11101100	1000
H =	11010011	0100
	10111010	0010
	01110101	0001

Generation of the FEC consists of logically ANDing the byte to be transmitted with bits 7 to 0 of each row of the H matrix. Even parity is generated for each of the 4 results and these 4 parity bits, in the positions indicated by the last 4 columns of the H matrix, form the FEC code.

In checking the FEC, the received 12-bit word is logically ANDed with each row of the H matrix (earliest bit received compared with the first column). Again even parity is generated for the 4 resulting words and these parity bits form a 4-bit nibble. If this nibble is all zero then no errors have been detected. Other results 'point' to the bit in error or indicate that uncorrectable errors have occurred.

This code can correct any single error that has occurred in each 12-bit (8 data + 4 FEC) section of the message.
Example:
If the byte to be coded is '00101100' then the FEC is derived as follows:

H matrix row:	1	2	3	4
A	11101100	11010011	10111010	01110101
B	00101100	00101100	00101100	00101100
A AND B	00101100	00000000	00101000	00100100
Even Parity:	1	0	0	0

Where A is bits 7 - 0 of one row of the H matrix and B is the byte to be coded. The even parity bits apply to the result of 'A AND B'.

So the word formed will be: '00101100 1000' sent left to right

When the same process is carried out on these 12 bits as above, using all 12 bits of each H matrix row, the resulting 4 parity bits will be '0000'.

4.5.3 Interleaving

The 240 bits of a Mobitex™ Data Block are interleaved by the modem before transmission to give protection against noise bursts and short fades. Interleaving is not performed on any bits in the Mobitex™ Frame Head.

Considering the 240 bits to be numbered sequentially before interleaving as 0 to 239 ('0' = bit 7 of byte 0, '11' = bit 0 of FEC for byte 0, ... ,'239' = bit 0 of FEC for byte 19 - see Figure 6), then they will be transmitted as shown in Figure 13.

The modem performs the inverse operation (de-interleaving) in receive mode on Mobitex™ Data Blocks.

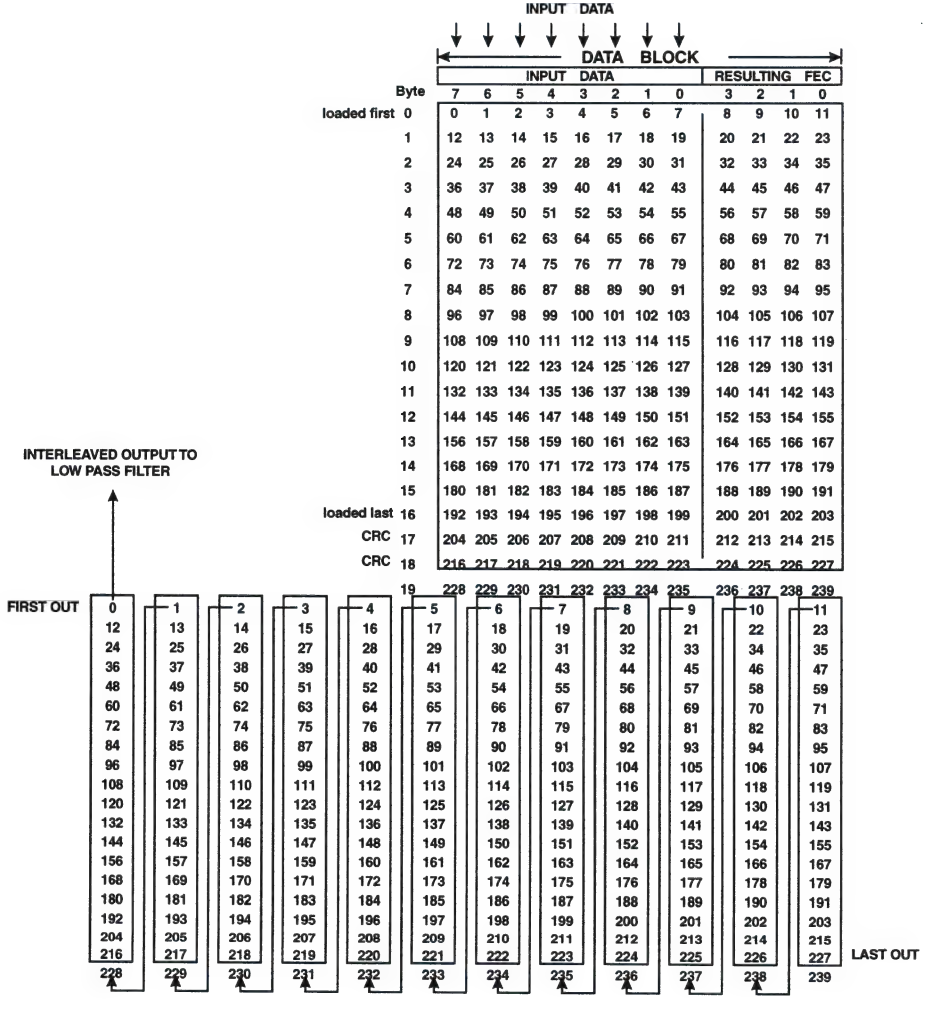


Figure 13: Interleaving - Input / Output

4.5.4 Scrambling

All formatted bits of a Mobitex™ Data Block are passed through a 9-bit scrambler. This scrambler is initialized at the beginning of the first Data Block in every Frame. The 511-bit sequence is generated with a 9-bit shift register with the output of the 5th and 9th stages XOR'ed and fed back to the input of the first stage. The scrambler is disabled during all other tasks, apart for TSO.

5. Application

5.1 Transmit Frame Example

If the device is required to send a Mobitex™ Frame the following control signals and data should be issued to the modem, provided the device is not starting from a powersave state, TX/$\overline{RX}$ is set to '1' and that SCREN, DARA, CKDIV, and DQEN have been set as required after power was applied to the device:

1. 6 bytes forming the Frame Head are loaded into the Data Buffer, followed by a 2-bit pause to let the filter stabilize, followed by setting T7H task.
2. Device interrupts host µC with $\overline{IRQ}$ when the 6th byte is read from the Data Buffer.
3. Status Register is read and 18 bytes are loaded, followed by setting TDB task.
4. Device interrupts host µC with $\overline{IRQ}$ when 18th byte is read from the Data Buffer.
5. Status Register is read, host may load data and set next task as required:
   - GOTO '1' if the last Data Block for this Frame has been transmitted and another Frame is to be immediately transmitted
   - GOTO '3' if another Data Block in this Frame is to be transmitted
   - GOTO '6' if no more data is to be immediately sent
6. 1 byte representing the 'hang byte' is loaded into the Data Buffer, followed by setting the TSB task.

If the 'hang byte' has been transmitted and no further data is to be sent, then a new task does not need be written and the µC can wait for the IBEMPTY interrupt ,when after a few bits, to allow for the Tx filter delay, it can shut down the Tx RF circuits.

A top level flowchart of the transmit process is shown in Figure 14.

5.1.1 Hang Byte

The filtering required to reduce the transmitted bandwidth causes energy from each bit of information to be spread across 3 bit times. To ensure that the last bit transmitted is received correctly it is necessary to add an 8-bit 'hang byte' to the end of each message. Thus the tasks required to transmit an isolated Mobitex™ frame are:

$$T7H + (n \times TDB) + TSB$$

When receiving this data, the extra byte can be ignored as its only function is to ensure integrity of the last bit and not to carry any information itself.

It is suggested that a '00110011' or '11001100' pattern is used for this 'hang byte'.

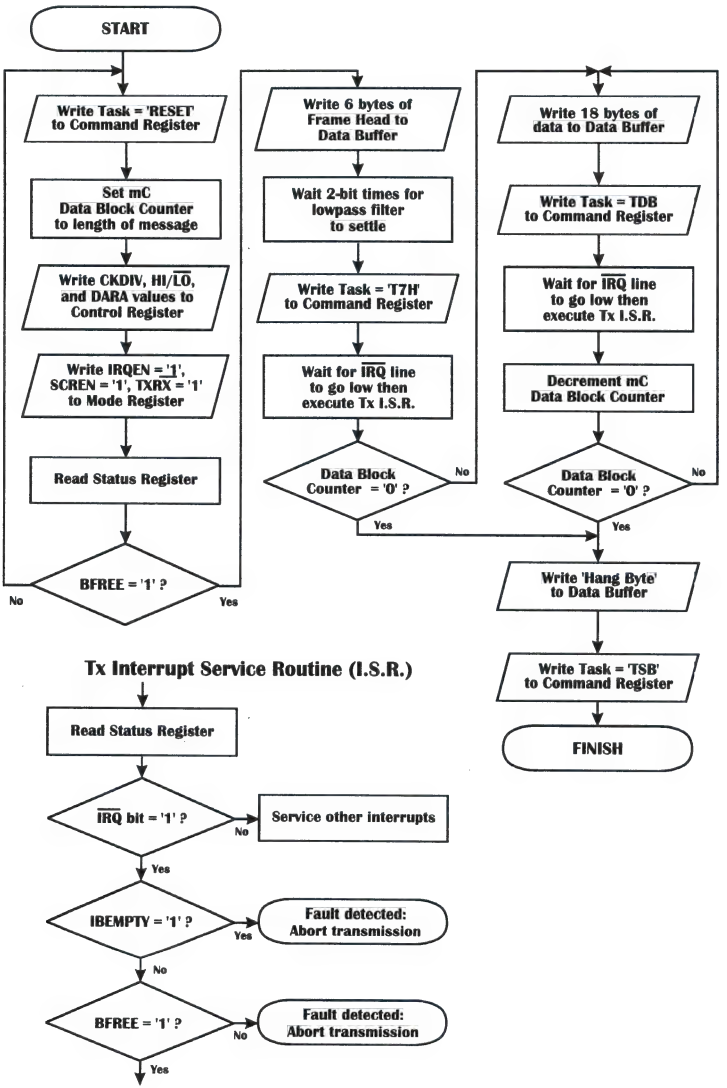

START
Write Task = 'RESET' to Command Register
Set mC Data Block Counter to length of message
Write CKDIV, HI/LO, and DARA values to Control Register
Write IRQEN = '1', SCREN = '1', TXRX = '1' to Mode Register
Read Status Register
BFREE = '1' ?
No
Yes
Write 6 bytes of Frame Head to Data Buffer
Wait 2-bit times for lowpass filter to settle
Write Task = 'T7H' to Command Register
Wait for IRQ line to go low then execute Tx I.S.R.
Data Block Counter = '0' ?
No
Yes
Write 18 bytes of data to Data Buffer
Write Task = TDB to Command Register
Wait for IRQ line to go low then execute Tx I.S.R.
Decrement mC Data Block Counter
Data Block Counter = '0' ?
No
Yes
Write 'Hang Byte' to Data Buffer
Write Task = 'TSB' to Command Register
FINISH
Tx Interrupt Service Routine (I.S.R.)
Read Status Register
IRQ bit = '1' ?
No
Service other interrupts
Yes
IBEMPTY = '1' ?
Yes
Fault detected: Abort transmission
No
BFREE = '1' ?
No
Fault detected: Abort transmission
Yes

Figure 14: Transmit Process Flow Chart

5.2 Receive Frame Example

If the device is required to decode a Mobitex™ Frame the following control signals should be issued to the modem, assuming the device is initially not in powersave, PLLBW, LEVRES, SCREN are set as required, TX/$\overline{RX}$

bit is set to '0', the Frame Sync bytes have not been set and the carrier has been detected, or a Frame Head is expected:

1. 2 Frame Sync bytes are loaded.
2. 2 bits after the carrier has been detected, an LFSB task is loaded, along with setting the AQLEV and AQBC bits, to initiate the level acquisition and bit clock extraction sequences.
3. Device interrupts host µC with $\overline{IRQ}$ when 2nd byte is read from Data Buffer.
4. Status Register is read, 12 bits later task is set to SFH to search for a Mobitex™ Frame Head.
5. Device will interrupt host µC with $\overline{IRQ}$ when valid Frame Sync is detected and header bytes decoded.
6. Host µC reads Status Register, checks MO/$\overline{BA}$ and CRCFEC bit and reads out 2 Frame Head control bytes.
7. Host µC sets the task to RDB to receive a Mobitex™ Data Block.
8. Device will interrupt host µC with $\overline{IRQ}$ when the Data Block has been received and the CRC has been calculated.
9. Host µC reads Status Register, checks CRC validity and reads 18 Data Block bytes. The Data Quality Register can also be read to obtain the received S/N level.
10. Host µC sets task if more information is expected:
    - GOTO '4' if last Data Block and another Frame Head are expected.
    - GOTO '7' if another Mobitex™ Data Block is expected.

If the last Data Block has been decoded and no further information is expected, then the task bits do not need to be set, as the device will automatically select the idle state.

A top level flowchart of the receive process is shown in Figure 15.

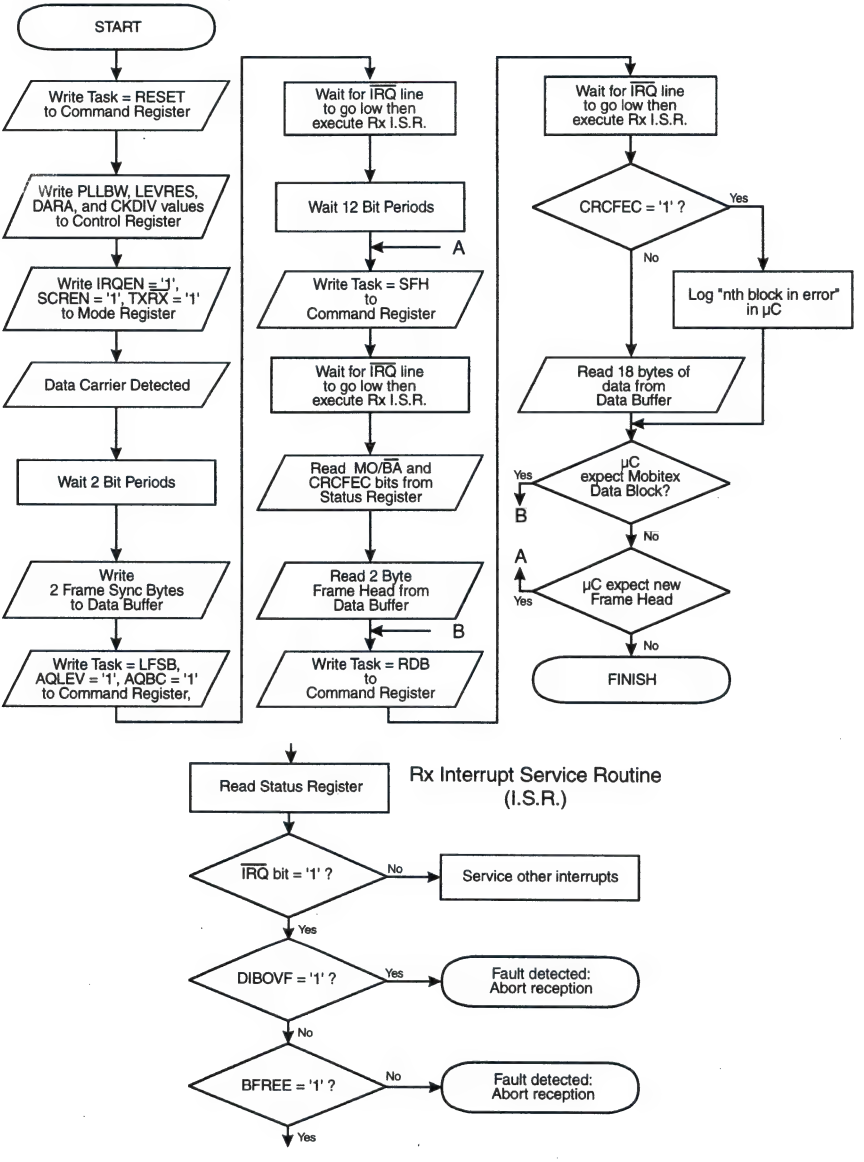

START
Write Task = RESET to Command Register
Write PLLBW, LEVRES, DARA, and CKDIV values to Control Register
Write IRQEN = '1', SCREN = '1', TXRX = '1' to Mode Register
Data Carrier Detected
Wait 2 Bit Periods
Write 2 Frame Sync Bytes to Data Buffer
Write Task = LFSB, AQLEV = '1', AQBC = '1' to Command Register,
Wait for IRQ line to go low then execute Rx I.S.R.
Wait 12 Bit Periods
A
Write Task = SFH to Command Register
Wait for IRQ line to go low then execute Rx I.S.R.
Read MO/BA and CRCFEC bits from Status Register
Read 2 Byte Frame Head from Data Buffer
B
Write Task = RDB to Command Register
Wait for IRQ line to go low then execute Rx I.S.R.
CRCFEC = '1' ?
Yes
No
Log "nth block in error" in µC
Read 18 bytes of data from Data Buffer
µC expect Mobitex Data Block?
Yes
B
No
A
µC expect new Frame Head
Yes
No
FINISH
Read Status Register
Rx Interrupt Service Routine (I.S.R.)
IRQ bit = '1' ?
No
Service other interrupts
Yes
DIBOVF = '1' ?
Yes
Fault detected: Abort reception
No
BFREE = '1' ?
No
Fault detected: Abort reception
Yes

Figure 15: Receive Process Flow Chart

5.3 Clock Extraction and Level Measurement Systems

The modem needs to make accurate measurements of the received signal amplitude, dc offset and bit timing to achieve reasonable error rates. Accurate measurements, especially in the presence of noise, are best made by averaging over a relatively long time.

However, in most cases the modem will be used to receive isolated messages from a distant transmitter that is only turned on for a very short time before the message starts. Also, the received baseband signal out of the radio's frequency discriminator will have a dc offset due to small differences between the receiver and transmitter reference oscillators and therefore their 'carrier' frequencies.

To allow for this situation, AQBC and AQLEV (Acquire Bit Clock and Level) commands are provided. When triggered, this causes the modem to follow an automatic sequence designed to perform these measurements as quickly as possible.

The AQLEV sequence always starts with a measurement of the average signal voltage over a period of 1 bit time. The sequence continues by measuring the positive going and negative going peaks of the signal. The attack and decay times used in this 'Lossy Peak Detect' mode are such that a sufficiently accurate measurement can be made within 16 bits of a ' 1100 ...' pattern (i.e. the bit sync sequence) to allow the bit clock extraction circuits to operate.

If SFH or SFS is set within 28 bit times of AQLEV the device will switch to the Residual setting when Frame Sync is found. If an SFH or SFS task is not set then the Residual setting will be active 30 bits after AQLEV was set. The Residual setting is that programmed in the LEVRES bits and is either 'Lossy Peak Detect', 'Peak Detect', 'Peak Averaging' or 'Hold'.

Note: For normal operation the LEVRES bits would only be set to 'hold' for the duration of a fade.

If SFH or SFS is set within 14 bit times of AQBC the device will switch to the Medium setting when Frame Sync is found. If an SFH or SFS task is not set then the Medium setting will be active 16 bits after AQBC was set. The PLLBW will change to the Residual setting 30 bits later.

The complete AQBC and AQLEV sequence, as illustrated in Figure 16, for the situation where the µC can detect the received carrier so that it knows when to issue the AQBC and AQLEV commands.

Note: Due to the delay through the Rx low pass filter, the AQBC and AQLEV sequences should not be started until approximately 2 bit times after the received carrier has been detected at the discriminator output. See Figure 16.

In a system where the host µC is not able to detect the received carrier, the AQBC and AQLEV sequences may be started at any time - possibly when no carrier is being received. However, in this case the clock and level acquisition will take longer since the circuits will have to recover from the change from a large amplitude noise signal at the output of the frequency discriminator to the wanted signal, probably with a dc offset. In this type of system, the time between the turn-on of the transmitter and the start of the Frame Sync pattern should be extended - preferably by extending the Bit Sync sequence to 32 or even 48 bits.

Note: The clock extraction circuits work by detecting the timing of edges, i.e. a change from '0' to '1' or '1' to '0'. They will eventually fail if '1' or '0' is transmitted continuously. Similarly, the level measuring circuits require '00' and '11' bit pairs to be received at reasonably frequent intervals.

©1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054

AQLEV Sequence
SFH or SFS is set up to 28 bits after AQLEV;
Frame Sync is being searched for:
1 bit of clamp.
Lossy Peak detect until Frame Sync is detected.
Residual setting.
SFH or SFS is not set; Frame Sync is not being searched for:
1 bit of clamp.
30 bits of Lossy Peak Detect.
Residual setting.

AQBC Sequence
SFH or SFS is set up to 14 bits after AQBC;
Frame Sync is being searched for:
'Wide' setting until Frame Sync detected.
30 bits of 'Medium' setting.
Residual setting.
SFH or SFS is not set; Frame Sync is not being searched for:
16 bits of 'Wide' setting.
30 bits of 'Medium' setting.
Residual setting.

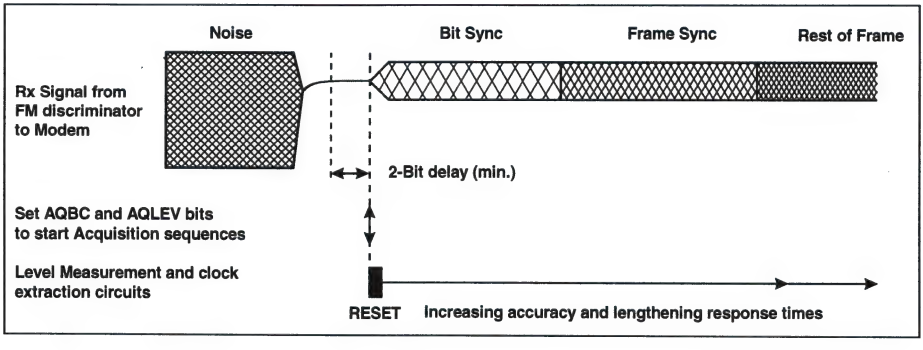

Noise
Bit Sync
Frame Sync
Rest of Frame
Rx Signal from FM discriminator to Modem
2-Bit delay (min.)
Set AQBC and AQLEV bits to start Acquisition sequences
Level Measurement and clock extraction circuits
RESET
Increasing accuracy and lengthening response times

Figure 16: Bit Clock and Level Acquisition Example

5.4 AC Coupling

For a practical circuit, when ac coupling from the modem's transmit output to the Frequency Modulator and between the receiver's Frequency Discriminator and the receive input of the modem may be desired. There are, however, two problems:.

1. AC coupling of the signal degrades the Bit Error Rate performance of the modem (at 8kbits/sec, without FEC, for different degrees of ac coupling). See Figure 17
2. Any ac coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As shown in Figure 18, the time for this step to decay to 37% of its original value is 'RC' when:

   RC = 1/(2 x π x the 3dB cut-off frequency of the RC network) and is 8 ms - or 64 bit times at 8kbits/sec for a 20Hz network.

©1996 MX•COM, INC.

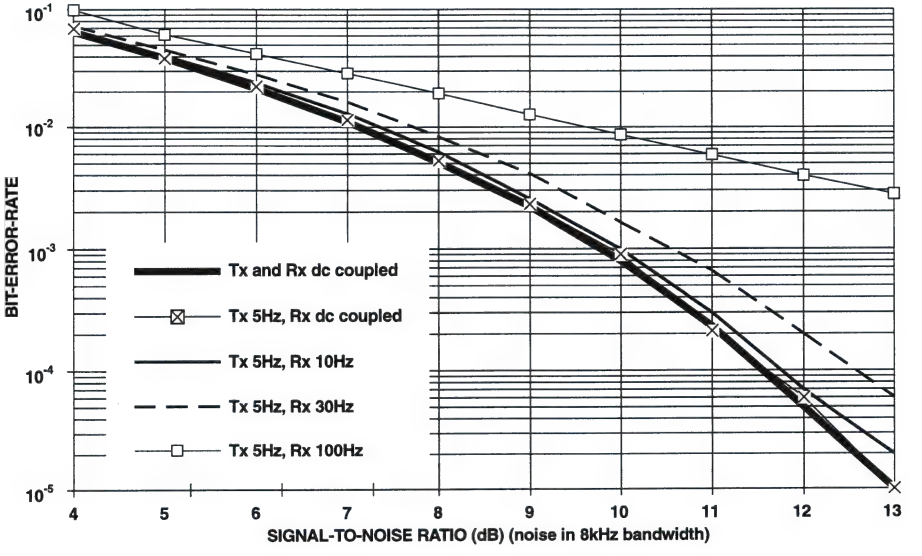


Figure 17: Typical Bit Error Rates (at 8kbits/sec, without FEC, for different degrees of ac decoupling)

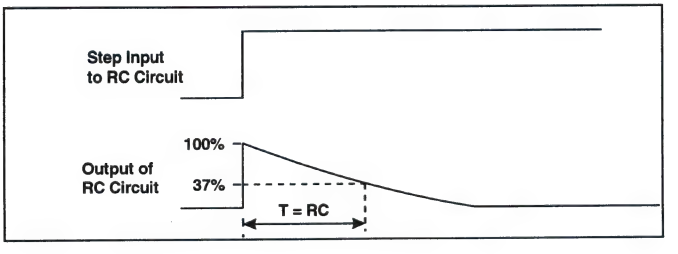


Figure 18: Decay Time - AC Coupling

Note: For these reasons the maximum 3dB cut-off frequencies would appear to be approximately 5Hz in the Tx path and 20Hz in the Rx path at 8kbits/sec.

5.5 Radio Performance

The maximum data rate that can be transmitted over a radio channel using this modem depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Bit rate.
- Peak carrier deviation (modulation index).
- Tx and Rx reference oscillator accuracy's.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 8kbits/sec can be achieved (subject to local regulatory requirements) over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ± 2kHz peak for a repetitive ' 1100... ' pattern and the maximum difference between transmitter and receiver 'carrier' frequencies is less than 1500Hz.

The modulation scheme employed by this modem is designed to achieve high data throughput, by exploiting as much as possible, the RF channel bandwidth. This does, however, place constraints on the performance of the radio. In particular, attention must be paid to:

- Linearity, frequency and phase response of the Tx Frequency Modulator.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a dc offset at the discriminator output.

Viewing the received signal eye pattern, using the output of the frequency discriminator, gives a good indication of the overall transmitter/receiver performance.

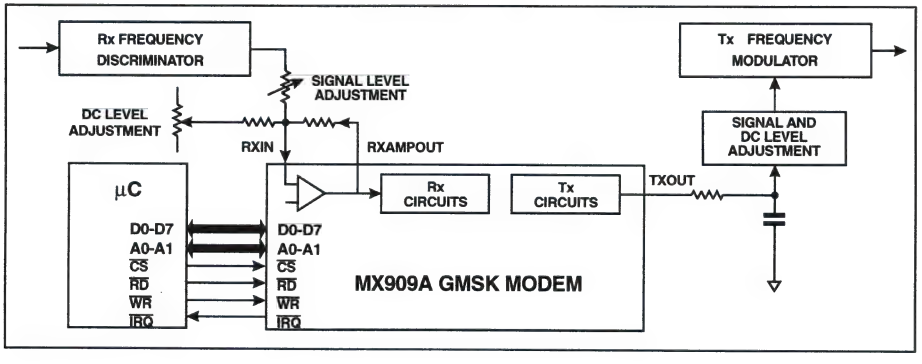


Figure 19: Typical System Installation

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device. Operation of the device outside the operating limits is not implied

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW, LH, P Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (VDD - VSS)		3.0	5.5	V
Temperature		-40	85	°C
Xtal Frequency		1.0	10.0	MHz

Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 4.096MHz, Bit Rate = 8k bits/sec, Noise Bandwidth = Bit Rate,
V_{DD} = 5.0V @ T_{AMB} = 25°C

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (not powersaved) (V_{DD} = 3.3V)	1		2.2	3.3	mA
I_{DD} (powersaved) (V_{DD} = 3.3V)	1		0.4	0.6	mA
I_{DD} (not powersaved)	1		3	4.5	mA
I_{DD} (powersaved)	1		0.9	1.4	mA
AC Parameters					
Tx Output					
TXOUT Impedance (not powersaved)	2		1.0	2.5	kΩ
TXOUT Impedance (powersaved)	2		300		kΩ
Signal Level	3	0.9	1.0	1.1	V_{P-P}
Tx Data Delay	4		4	6	bits
Rx Input					
RXIN Impedance (at 100Hz)		10.0			MΩ
RXIN Amp Voltage Gain (input = 1mV_{RMS} at 100Hz)			500		V/V
Input Signal Level	5	0.7	1.0	1.3	V_{P-P}
Rx Data Delay	6		3.5		bits
Xtal/Clock Input					
'High' Pulse Width	7	40			ns
'Low' Pulse Width	7	40			ns
Input Impedance (at 100Hz)		10.0			MΩ
Gain (input = 1 mV_{RMS} at 100Hz)		20			dB
µC Interface					
Input Logic "1" Level	8, 9	70%			V_{DD}
Input Logic "0" Level	8, 9			30%	V_{DD}
Input Leakage Current (V_{IN} = 0 to V_{DD})	8, 9	−5.0		5.0	µA
Input Capacitance	8, 9		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)	9	90%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)	9,10			10%	V_{DD}
'Off' State Leakage Current (V_{OUT} = V_{DD})	10			10	µA

Operating Characteristics Notes:

1. Not including any current drawn from the modem pins by external circuitry.
2. Small signal impedance
3. For "1111000011110000.." bit sequence (output level is proportional to V_{DD}).
4. Measured between issuing first task after idle and the center of the first bit at TXOUT (see Figure 7)
5. For optimum performance, measured at RXAMPOUT pin, for a "...11110000..." bit sequence
6. Measured between center of last bit of an Rx single byte or Frame Sync at RXIN and an IRQ interrupt to the host µC.
7. Timing for an external input to the CLOCK/XTAL pin.
8. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0 and A1 pins.
9. D0 - D7 pins.
10. $\overline{IRQ}$ pin.

©1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054

Timing

For the following conditions unless otherwise specified:
Xtal Frequency = 4.096MHz, V_{DD} = 5.0V @ T_{AMB} = 25°C

µC Parallel Interface Timings ref (Figure 20)		Notes	Min.	Typ.	Max.	Units
t_{ACSL}	Address valid to $\overline{CS}$ low time		0			ns
t_{AH}	Address hold time		0			ns
t_{CSH}	$\overline{CS}$ hold time		0			ns
t_{CSHI}	$\overline{CS}$ high time	1	6			clock cycles
t_{CSRWL}	$\overline{CS}$ to $\overline{WR}$ or $\overline{RD}$ low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90			ns
t_{RHCSL}	$\overline{RD}$ high to $\overline{CS}$ low time (write)		0			ns
t_{RACL}	Read access time from $\overline{CS}$ low	2			175	ns
t_{RARL}	Read access time from $\overline{RD}$ low	2			145	ns
t_{RL}	$\overline{RD}$ low time		200			ns
t_{RX}	$\overline{RD}$ high to D0-D7 3-state time				50	ns
t_{WHCSL}	$\overline{WR}$ high to $\overline{CS}$ low time (read)		0			ns
t_{WL}	$\overline{WR}$ low time		200			ns

Timing Notes:

1. Xtal/Clock cycles at the XTAL/CLOCK pin.
2. With 30pF max to V_{SS} on D0 - D7 pins.

©1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054

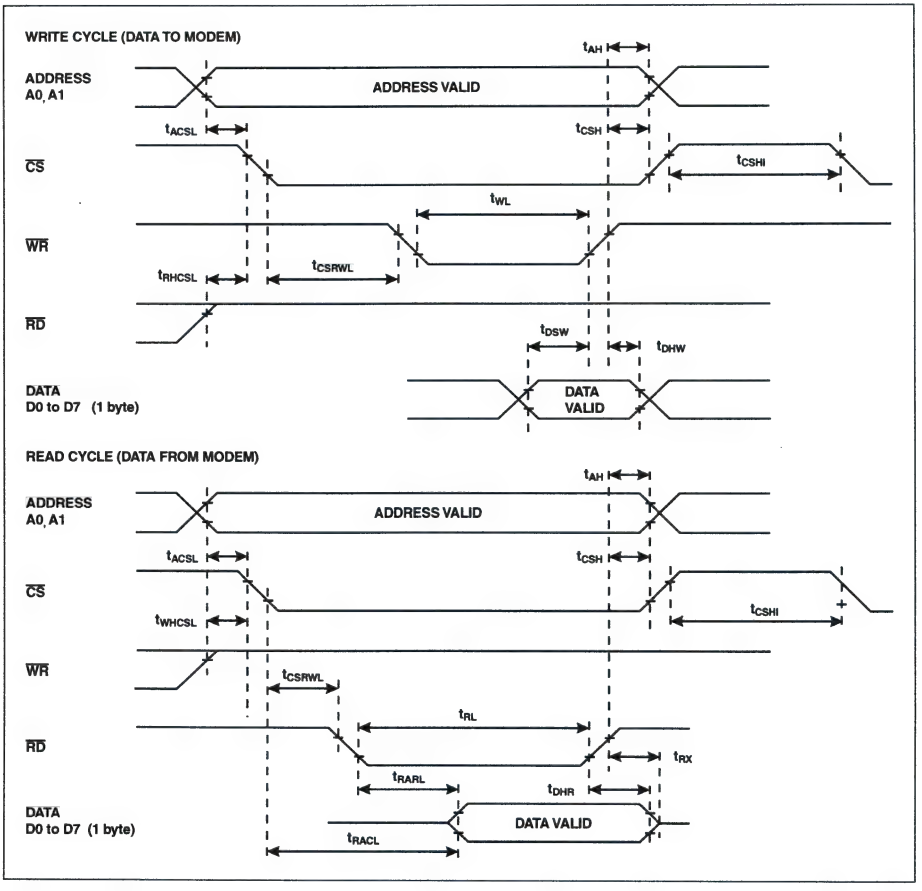
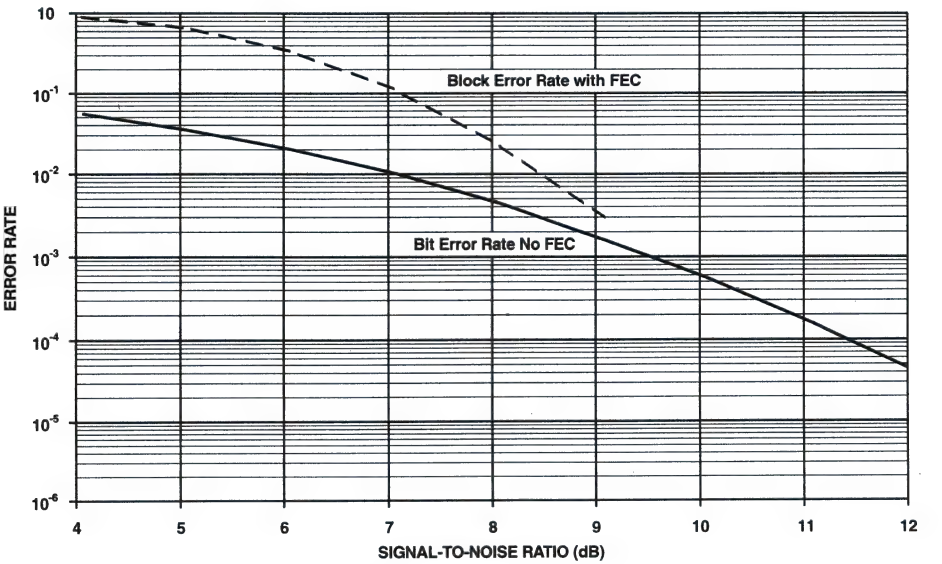


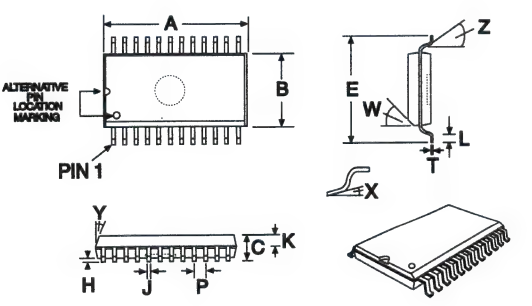
Figure 20: µC Parallel Interface Timing Diagram



NOTE: A block is deemed to be "In Error" if the CRC fails

Figure 21: Typical Bit Error Rate (noise in bit rate bandwidth)

6.2 Packaging

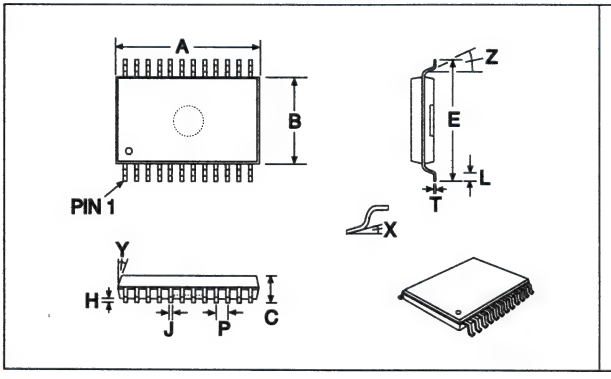


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 22: 24-pin SOIC Mechanical Outline : *Order as part no. MX909ADW*

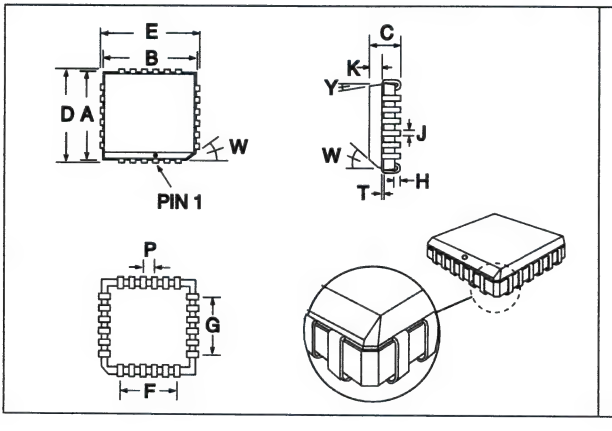


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 23: 24-PIN SSOP Mechanical Outline: *Order as part no. MX909ADS*



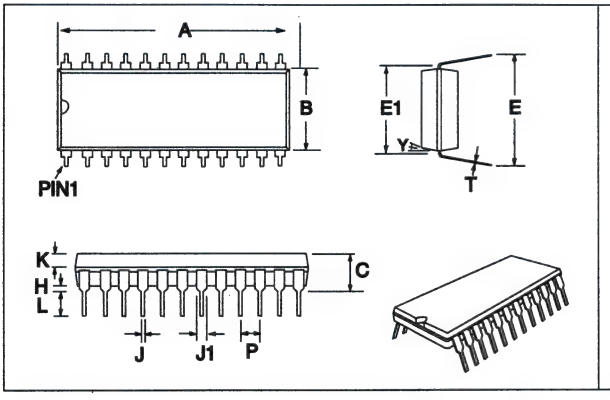
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 24: 24-pin PLCC Mechanical Outline: *Order as part no. MX909ALH*

©1996 MX-COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 25: 24-pin PDIP Mechanical Outline: *Order as part no. MX909AP*

7. Errata

Coincident transitions of the $\overline{WR}$ signal and an internal clock can cause a newly written task to be ignored. In typical applications 1 out of 100,000 tasks may be ignored. Many users may never notice such an infrequent event, but to ensure that each task is loaded correctly, the software must check to see if the BFREE bit is low '0' immediately after every task set. Below is a recommended method for writing tasks.

- Procedure for writing RESET tasks:
  - Write the RESET task twice
- Procedure for writing NULL tasks with either of the Acquire bits set:
  - Write the NULL task twice
- Procedure for writing other tasks:
  - The µC should wait until the BFREE (Buffer Free) bit of the Status Register is '1' before writing the desired task to the Command Register.
  - Immediately after the task is written, the controlling device should check the value of the BFREE bit in the Status Register:
    - If BFREE = '0' then the task has been accepted.
    - If BFREE = '0' then the task needs to be rewritten to the Command Register

Note:

1. In Tx, the Data Buffer contents do not have to be rewritten if the task is not accepted.
2. In Rx, if either of the Acquire bits need to be set, then they will also have to be set in the repeated task.
3. Future revisions of this part will ensure that all newly written tasks will be accepted without requiring any task writes to be repeated.

©1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050 Fax: 910 744 5054
Doc # 20480134.002

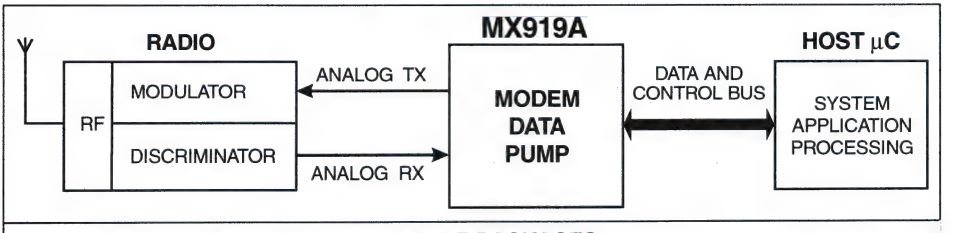
MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX919A 4-Level FSK Modem Data Pump

PRELIMINARY INFORMATION

- **4-Level FSK Modulation**
- **Half Duplex, 4800 to 19.2k bits/sec**
- **Full Data Packet Framing**
- **Increase Channel Bit Rate/Hz**
- **Flexible Operating Modes**
- **Host μC Interface**
- **Low Power 3.3V/5V Operation**
- **24-Pin Small Form Package Option**



AVAILABLE PACKAGES

MX919ADS
24-pin SSOP

MX919ADW
24-pin SOIC

MX919ALH
24-pin PLCC

MX919AP
24-pin PDIP

The MX919A is a low voltage CMOS device containing all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for a high performance 4-level FSK Wireless Packet Data Modem. It interfaces with the modem host μC and the radio modulation/demodulation circuits to deliver reliable two-way transfer of the application data over a wireless link.

The MX919A assembles application data received from the host μC, adds forward error correction (FEC) and error detection (CRC) information and interleaves the result for burst-error protection. After automatically adding symbol and frame sync codewords, the data packet is converted into filtered 4-level analog signals for modulating the radio transmitter.

In receive mode, the MX919A performs the reverse function using the analog signals from the receiver discriminator. After error correction and removal of the packet overhead, the recovered application data is supplied to the host μC. CRC detected residual uncorrected data errors will be flagged. A readout of the SNR value during receipt of a packet is also provided.

The MX919A uses data block sizes and FEC/CRC suitable for applications where high speed transfer of data over narrow-band wireless links is required. The device is programmable to operate at standard bit rates from a wide range of Xtal/clock frequencies..

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc.# 20480151.002

CONTENTS

Section ..... Page

1. Block Diagram 1-113

2. Signal List 1-114

3. External Components 1-115

4. General Description 1-116
4.1 Description of Blocks 1-116
4.2 Modem - µC Interaction 1-119
4.3 Binary to Symbol Translation 1-119
4.4 Frame Structure 1-120
4.5 The Programmer's View 1-121
4.6 CRC, FEC and Interleaving 1-132

5. Application 1-133
5.1 Transmit Frame Example 1-133
5.2 Receive Frame Example 1-136
5.3 Clock Extraction and Level Measurement Systems 1-138
5.4 AC Coupling 1-140
5.5 Radio Performance 1-141

6. Performance Specification 1-142
6.1 Electrical Performance 1-142
6.2 Packaging 1-146

MX•COM, Inc. Reserves the right to change specifications at any time and without notice

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

1. Block Diagram

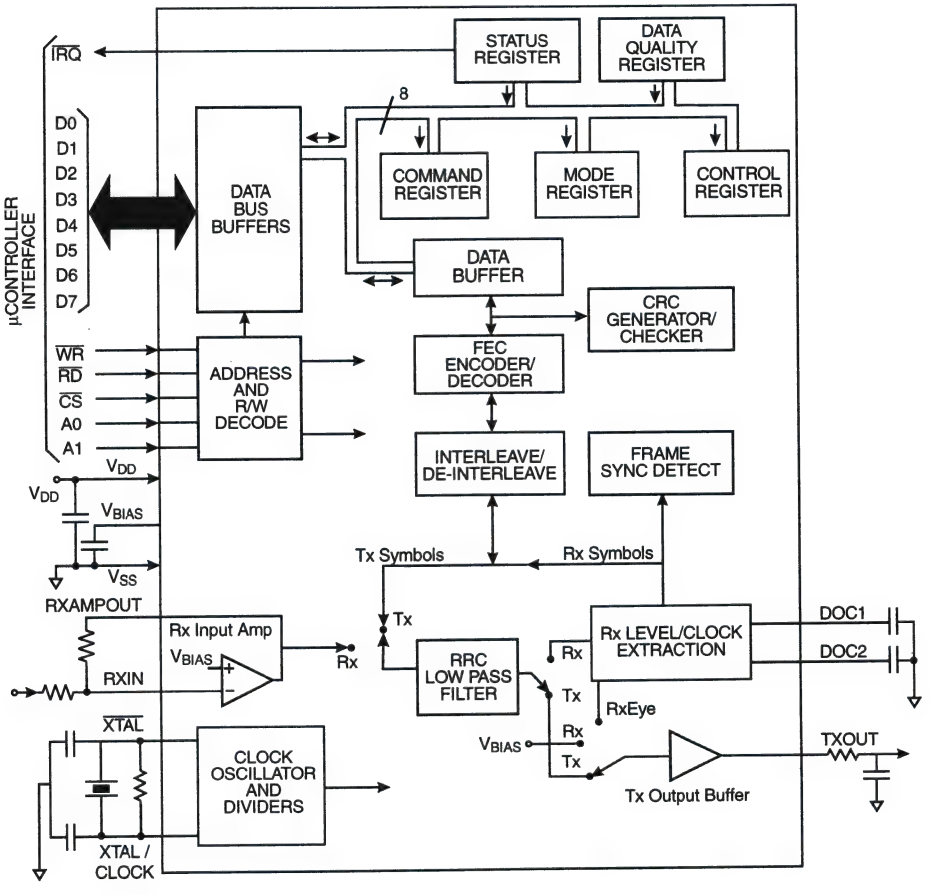


Figure 1: Block Diagram

2. Signal List

Pin No.	Signal	Type	Description
1	$\overline{IRQ}$	output	A 'wire-ORable' output for connection to the host µC's Interrupt Request input. When active this output has a low impedance pull down to V_{SS}. It has a high impedance when inactive.
2	D7	BUS	Pins 2-9 (D7-D0) are 8-bit, bi-directional, 3-state µC interface data lines
3	D6	BUS	
4	D5	BUS	
5	D4	BUS	
6	D3	BUS	
7	D2	BUS	
8	D1	BUS	
9	D0	BUS	
10	$\overline{RD}$	input	Read. An active low logic level input used to control the reading of data from the modem into the host µC.
11	$\overline{WR}$	input	Write. An active low logic level input used to control the writing of data into the modem from the host µC.
12	V_{SS}	power	Negative supply. (ground).
13	$\overline{CS}$	input	Chip Select. An active low logic level input to the modem, used to enable a data read or write operation.
14	A0	input	Logic level modem register select input
15	A1	input	Logic level modem register select input
16	$\overline{XTAL}$	output	Output of the on-chip oscillator.
17	XTAL/CLOCK	input	Input to the on-chip oscillator, for external Xtal circuit or clock.
18	DOC 2	output	Connection to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}
19	DOC 1	output	Connection to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}
20	TXOUT	output	Tx signal output from the modem.
21	V_{BIAS}	output	A bias line for the internal circuitry, held at V_{DD} /2. This pin must be bypassed to V_{SS} by a capacitor mounted close to the device pins.
22	RXIN	input	Input to the Rx input amplifier.
23	RXAMPOUT	output	Output of the Rx input amplifier.
24	V_{DD}	power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

3. External Components

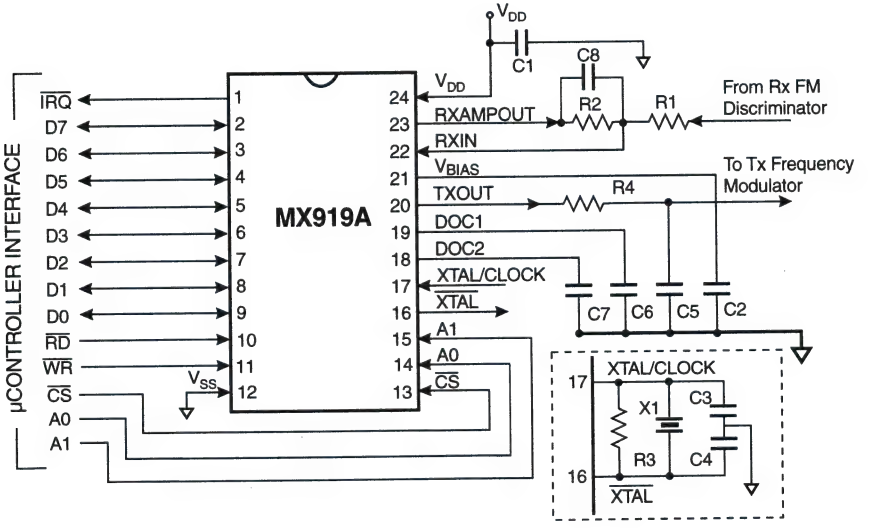


Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1	1		±20%
R2		100kΩ	±5%
R3		1MΩ	±20%
R4		100kΩ	±5%
C1		0.1 µF	±20%
C2		0.1 µF	±20%
C3	2		±20%
C4	2		±20%
C5	3		±5%
C6	4		±20%
C7	4		±20%
C8	3		±5%
X1	5		

Recommended External Component Notes:

1. See Section 4.1.10.
2. The values used for C3 and C4 should be suitable for the frequency of the crystal X1. As a guide, values (including stray capacitance) of 33pF at 1MHz falling to 18pF at 10MHz will generally prove suitable. For optimum performance, the crystal frequency tolerance should be ±10ppm or better to allow for use of the Narrow Bandwidth PLL setting (see Section 4.5.3). Tolerances as wide as ±50ppm may be used, but at the cost of slightly reduced BER performance.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

3. Values C5 and C8 should equal the following: 750,000 / symbol rate

Symbol Rate	C5 / C8
2400 symbols/second	330pF
4800 symbols/second	150pF
9600 symbols/second	82pF

4. Values C6 and C7 should equal the following: 50,000 / symbol rate

Symbol Rate	C6 / C7
2400 symbols/second	0.022µF
4800 symbols/second	0.01µF
9600 symbols/second	4700pF

5. See Section 4.5.3.

4. General Description

4.1 Description of Blocks

4.1.1 Data Bus Buffers

Eight bi-directional 3-state logic level buffers between the modem's internal registers and the host µC's data bus lines.

4.1.2 Address and R/W Decode

This block controls the transfer of data bytes between the µC and the modem's internal registers, according to the state of the Write and Read Enable inputs (WR and $\overline{RD}$), the Chip Select input ($\overline{CS}$) and the Register Address inputs A0 and A1.

The Data Bus Buffers, Address and R/W Decode blocks provide a byte-wide parallel µC interface, which can be memory-mapped, as shown in Figure 3

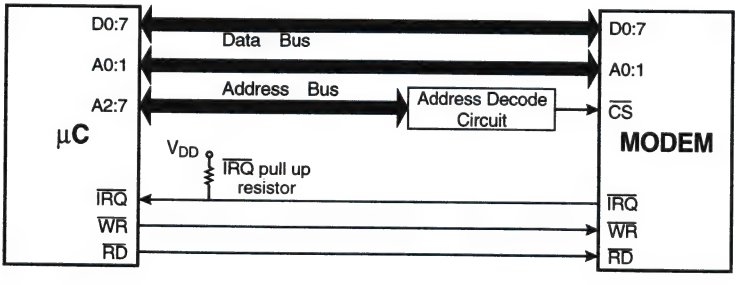


Figure 3: Typical Modem µC connections

4.1.3 Status and Data Quality Registers

Two, 8-bit registers which the µC can read, to determine the status of the modem and the received data quality.

4.1.4 Command, Mode and Control Registers

The values written by the µC to these 8-bit registers control the operation of the modem.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.1.5 Data Buffer

A 12-byte buffer used to hold receive or transmit data to or from the µC.

4.1.6 CRC Generator/Checker

A circuit which generates (in transmit mode) or checks (in receive mode) the Cyclic Redundancy Checksum bits, which may be included in the transmitted data blocks so the receive modem can detect transmission errors.

4.1.7 FEC Generator/Checker

In transmit mode, this circuit adds Forward Error Correction bits to the transmitted data, resulting in the conversion of binary data to 4-level symbols. In receive mode, this circuit translates received 4-level symbols to binary data, using the FEC information to correct a large proportion of transmission errors.

4.1.8 Interleave/De-interleave Buffer

This circuit interleaves data symbols within a block before transmission and de-interleaves the received data so that the FEC system is best able to handle short noise bursts or fades.

4.1.9 Frame Sync Detect

This circuit, which is only active in receive mode, is used to look for the 24-symbol Frame Synchronization pattern that is transmitted to mark the start of every frame.

4.1.10 Rx Input Amp

This amplifier allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components R1 and R2. The value of R1 should be calculated to give $(0.2 \times V_{DD})V_{P\text{-}P}$ at the RXAMPOUT pin for a received '...+3 +3 -3 -3 ...' sequence.

A capacitor may be placed in series with R1 if ac coupling of the received signal is desired (see Section 5.4), otherwise the dc level of the received signal should be adjusted so that the signal at the modem's RXAMPOUT pin is centered around V_{BIAS} ($V_{DD}/2$).

4.1.11 RRC Low Pass Filter

This filter, which is used in both transmit and receive modes, is a linear-phase lowpass filter with a 'Root Raised Cosine' frequency response defined by:

$$
\begin{aligned}
H(f) &= 1 && \text{for } 0 && \le f < (1-b)/(2T)\\
&= \text{square root of } \{0.5\,[1 - \sin(\pi\, T\, (f - 0.5/T)/b)]\} && \text{for } (1-b)/(2T) && \le f \le (1+b)/(2T)\\
&= 0 && \text{for } (1+b)/(2T) && < f
\end{aligned}
$$

where b = 0.2, T = 1/symbol rate

This frequency response is illustrated in Figure 5.

In transmit mode, the 4-level symbols are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

In receive mode, the filter is used to reject HF noise and to equalize the received signal to a form suitable for extracting the 4-level symbols.

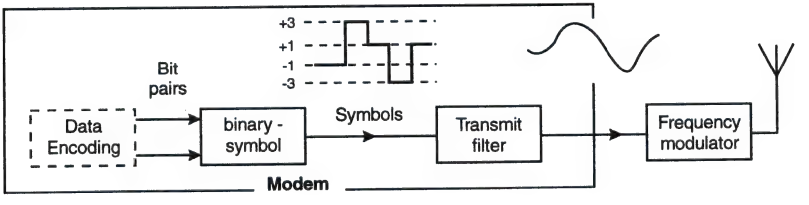


Figure 4: Translation of Binary Data to Filtered 4-Level Symbols in Tx Mode

4.1.12 Tx Output Buffer

This is a unity gain amplifier used in the transmit mode to buffer the output of the Tx low pass filter. In receive mode, the input of this buffer is connected to V_{BIAS}, unless the RXEYE bit of the Control Register is '1', when it is connected to the received signal. When changing from Rx to Tx mode the input to this buffer will be connected to V_{BIAS} for 8 symbol times while the RRC filter settles.

Note: The RC low pass filter formed by the external components R4 and C5 between the TXOUT pin and the input to the radio's frequency modulator forms an important part of the transmit signal filtering. These components may form part of any dc level-shifting and gain adjustment circuitry. The value used for C5 should take into account stray circuit capacitance, and its ground connection should be positioned to give maximum attenuation of high frequency noise into the modulator.

The signal at the TXOUT pin is centered around V_{BIAS}. It is approximately $(0.2 \times V_{DD})V_{P-P}$ for a continuous '+3 +3 -3 -3 ...' pattern.

A capacitor may be placed in series with the input to the frequency modulator if AC coupling is desired, see Section 5.4

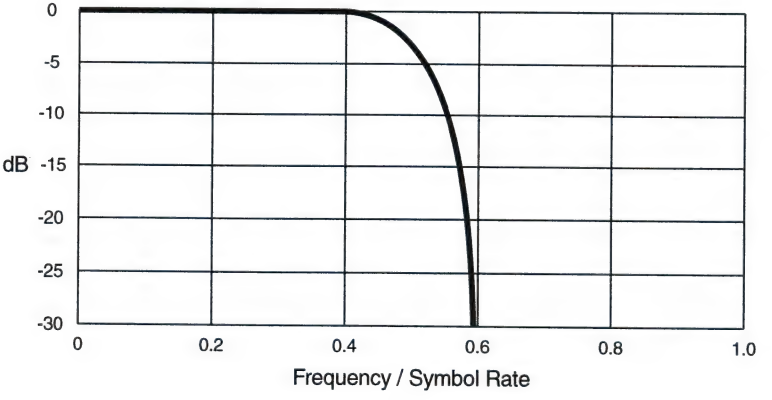


Figure 5: RRC Filter Frequency Response (including the external RC filter R4/C5)

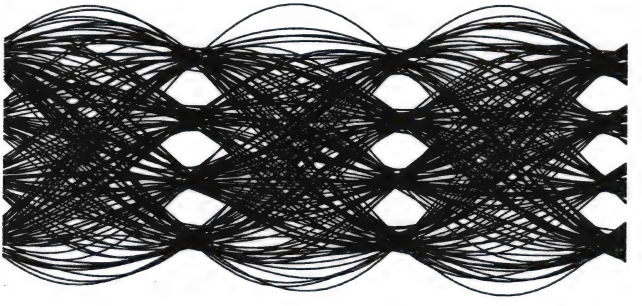


Figure 6: Transmitted Signal Eye Diagram

4.1.13 Rx Level/Clock Extraction

These circuits, which operate only in receive mode, derive a symbol rate clock from the received signal and measures the received signal amplitude and dc offset. This information is then used to extract the received 4-level symbols and also to provide an input to the received Data Quality measuring circuit. The external capacitors C6 and C7 form part of the received signal level measuring circuit.

4.1.14 Clock Oscillator and Dividers

These circuits derive the transmit symbol rate (and the nominal receive symbol rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or applied from an external source.

Note: If the on-chip Xtal oscillator is to be used, then the external components X1, C3, C4 and R3 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin, the $\overline{\text{XTAL}}$ pin should be left unconnected, and X1, C3, C4 and R3 not fitted.

4.2 Modem - µC Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Preamble' followed by one or more formatted data blocks. The Frame Preamble includes a Frame Synchronization pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (cyclic redundancy checksum) generation, Forward Error Correction coding and Interleaving. Details of the message formats handled by the modem are given in Section 4.3 and Figure 7 and Figure 8.

To reduce the processing load on the associated µC, the MX919A modem has been designed to perform as much of the computationally intensive work involved in Frame formatting and de-formatting and when in receive mode, in searching for and synchronizing onto the Frame Preamble. In normal operation the modem will only require servicing by the µC once per received or transmitted block.

Thus, to transmit a block, the controlling µC needs only to load the - unformatted - 'raw' binary data into the modem's Data Block Buffer, instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result as 4-level symbols (with Forward Error Correction coding) and interleave the symbols before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received symbols, de-interleave the symbols, translate them to binary - using the FEC coding to correct as many errors as possible - and check the resulting CRC before placing the received binary data into the Data Block Buffer for the µC to read.

The modem can also handle the transmission and reception of unformatted data - for example: to allow the transmission of Symbol and Frame Synchronization sequences or special test patterns.

4.3 Binary to Symbol Translation

Although, the over-air signal and therefore the signals at the modem TXOUT and RXIN pins, consists of 4-level symbols, the raw data passing between the modem and the µC is in binary form. Translation between binary data and the 4-level symbols is done in one of two ways, depending on the task being performed.

1. Direct: (simplest form) - converts between 2 binary bits and a single symbol.

SYMBOL	MSB	LSB
+3	1	1
+1	1	0
-1	0	0
-3	0	1

This is expanded so an 8-bit byte translates to four symbols for the T4S, T24S and R4S tasks described in Section 4.5.2.

	MSB							LSB
Bits:	7	6	5	4	3	2	1	0
Symbols:	a		b		c		d	
	sent first						sent last	

2. FEC (more complicated) - essentially translates groups of 3 binary bits to pairs of 4-level symbols using a Forward Error Correcting coding scheme for the block oriented tasks THB, TIB, TLB, RHB and RILB described in Section 4.5.2.

4.4 Frame Structure

Figure 7 shows how an over-air message frame may be constructed from Frame and Symbol Sync patterns, followed by one or more 'Header', 'Intermediate' or 'Last' blocks.

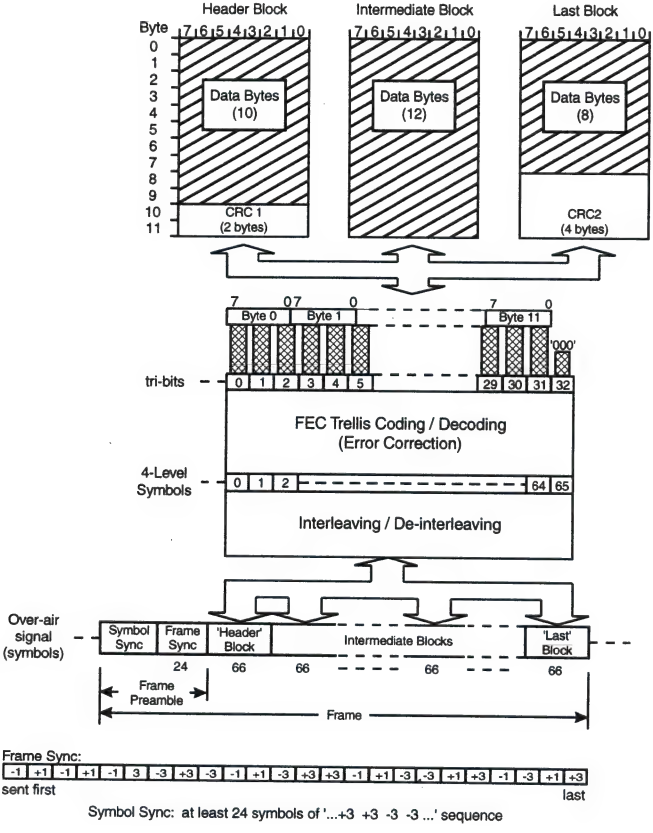


Figure 7: Over-Air Signal Format

The 'Header' block is self-contained, it includes its own checksum (CRC1), and would normally carry information such as the address of the calling and called parties, the number of following blocks in the frame (if any) and miscellaneous control information.

The 'Intermediate' block(s) contain only data, the checksum for all of the data in the 'Intermediate' and 'Last' blocks (CRC2) being contained at the end of the 'Last' block.

This arrangement, while efficient in terms of data capacity, may not be optimum for poor signal-to-noise conditions, since a reception error in any one of the 'Intermediate' or 'Last' blocks would invalidate the whole frame. In such conditions, increased throughput may be obtained by using the 'Header' block format for all blocks

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

of the frame, so blocks that are received correctly can be identified as such, and do not need to be re-transmitted. This, and some other possible frame structures, are shown in Figure 8.

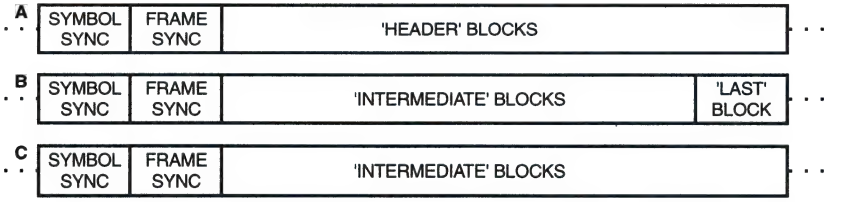


Figure 8: Alternative Frame Structure

The MX919A performs all of the block formatting and de-formatting, the binary data transferred between the modem and its µC is shown by diagonal lines in Figure 7.

4.5 The Programmer's View

To the programmer, the modem appears as 4, write only 8-bit registers, shadowed by 3 read only registers. The individual registers are selected by the A0 and A1 chip inputs:

A1	A0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	Data Quality Register
1	1	Mode Register	not used

Note: There is a minimum time allowance between accesses of the modem's registers, see Section 6.1.

4.5.1 Data Block Buffer

This is a 12-byte read/write buffer used to transfer data (as opposed to command, status, mode, data quality or control information) between the modem and the host µC.

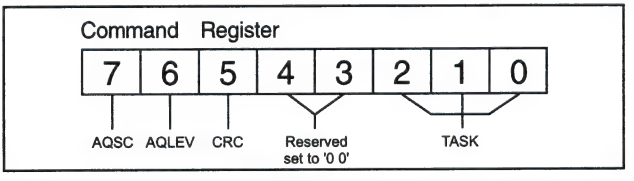
To the µC, the Data Block Buffer appears as a single 8-bit register. The modem ensures that sequential µC reads or writes to the buffer are routed to the correct locations within the buffer.

The µC should only access this buffer when the Status Register BFREE (Buffer Free) bit is '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode. Note that in receive mode the modem will function correctly even if the received data is not read from the Data Buffer by the µC.

4.5.2 Command Register

Writing to this register tells the modem to perform a specific action or actions, depending on the setting of the TASK, AQLEV and AQSC bits.



When there is no action to perform, the modem will be in an 'idle' state. If the modem is in transmit mode the input to the Tx RRC filter will be connected to V_{BIAS}. In receive mode the modem will continue to measure the received data quality and extract symbols from the received signal, supplying them to the de-interleave buffer, otherwise the received data is ignored.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.5.2.1 Command Register B7: AQSC - Acquire Symbol Clock

This bit has no effect in transmit mode.

In receive mode, when a byte with the AQSC bit set to '1' is written to the Command Register, and TASK is not set to RESET, it initiates an automatic sequence designed to achieve symbol timing synchronization with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronization is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however; the acquisition sequence will be re-started every time a byte written to the Command Register has the AQSC bit set to '1'.

The AQSC bit will normally be set at the same time as a SFS (Search for Frame Sync) or SFSH (Search for Frame Sync plus Header block) task is written to the MX919A, however it may also be used independently to re-establish clock synchronization quickly after a long fade. Alternatively, a SFS or SFSH task may be written to the Command Register with the AQSC bit at '0' if it is known that clock synchronization does not need to be re-established.

4.5.2.2 Command Register B6: AQLEV - Acquire Receive Signal Levels

This bit has no effect in transmit mode.

In receive mode, when a byte with the AQLEV bit set to '1' is written to the Command Register and TASK is not set to RESET, it initiates an automatic sequence designed to measure the amplitude and dc offset of the received signal as rapidly as possible. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time, therefore improving the measurement accuracy, until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however; the acquisition sequence will be re-started every time a byte written to the Command Register has the AQLEV bit set to '1'.

The AQLEV bit will normally be set at the same time as a SFS (Search for Frame Sync) or SFSH (Search for Frame Sync plus Header Block) task is initiated, however it may also be used independently to re-establish signal levels quickly after a long fade. Alternatively, a SFS or SFSH task may be written to the Command Register with the AQLEV bit at '0' if it is known that there is no need to re-establish the received signal levels.

4.5.2.3 Command Register B5: CRC

This bit allows the user to select between two different forms of the CRC1 and CRC2 checksums. When this bit is set to '0' the CRC generators are initialized to 'all ones' as for CCITT X25 CRC calculations. When this bit is set to '1' the CRC generators are initialized to 'all zeros'. Setting this bit to '0' provides compatibility with older 'non A' version of the MX919. Other systems may set this bit as required.

4.5.2.4 Command Register B4, B3

These bits should be set to '0'.

4.5.2.5 Command Register B2, B1, B0: TASK

Operations such as transmitting or receiving a data block are treated by the modem as 'tasks' and are initiated when the µC writes a byte to the Command Register with the TASK bits set to anything other than the 'NULL' code.

The µC should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is '0'.

Different tasks apply in receive and transmit modes.

When the modem is in transmit mode, all tasks other than NULL or RESET instruct the modem to transmit data from the Data Buffer, formatting it as required. The µC should therefore wait until the BFREE (Buffer Free) bit of the Status Register is '1', before writing the data to the Data Block Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Block Buffer, byte number 0 of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE (Buffer Free) bit of the Status Register to '0'.

Take the data from the Data Block Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

Once all of the data has been transferred from the Data Block Buffer the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the chip $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may write new data and the next task to the modem.

This lets the µC write a task and the associated data to the modem while the modem is still transmitting the data from the previous task.

© 1996 MX•COM, INC. Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

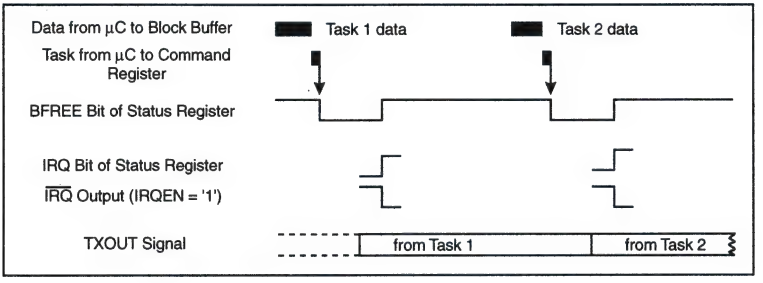

Data from µC to Block Buffer
Task 1 data
Task 2 data
Task from µC to Command Register
BFREE Bit of Status Register
IRQ Bit of Status Register
IRQ Output (IRQEN = '1')
TXOUT Signal
from Task 1
from Task 2

Figure 9: Transmit Task Overlapping

When the modem is in receive mode, the µC should wait until the BFREE bit of the Status Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to '0'.

Wait until enough received symbols are in the De-interleave Buffer.

Decode them as needed, and transfer the resulting binary data to the Data Block Buffer

Then the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may read from the Data Block Buffer and write the next task to the modem. If more than 1 byte is contained in the buffer, byte number 0 of the data will be read out first.

In this way the µC can read data and write a new task to the modem while the received symbols needed for this new task are being received and stored in the De-interleave Buffer.

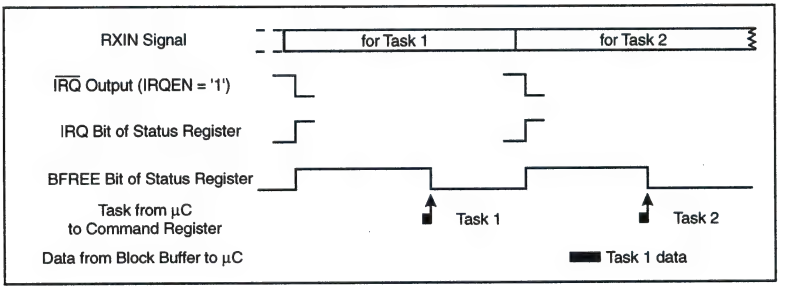


Figure 10: Receive Task Overlapping

Detailed timings for the various tasks are provide in Figure 11 and Figure 12.

© 1996 MX•COM, INC.

MX919A Modem Tasks:

B2	B1	B0	Receive Mode		Transmit Mode	
0	0	0	NULL		NULL	
0	0	1	SFSH	Search for FS + Header	T24S	Transmit 24 symbols
0	1	0	RHB	Read Header Block	THB	Transmit Header Block
0	1	1	RILB	Read Intermediate or Last Block	TIB	Transmit Intermediate Block
1	0	0	SFS	Search for Frame Sync	TLB	Transmit Last Block
1	0	1	R4S	Read 4 symbols	T4S	Transmit 4 symbols
1	1	0	NULL		NULL	
1	1	1	RESET	Cancel any current action	RESET	Cancel any current action

4.5.2.6 NULL: No effect

This 'task' is provided so an AQSC or AQLEV command can be initiated without loading a new task.

4.5.2.7 SFSH: Search for Frame Sync plus Header Block

This task causes the modem to search the received signal for a valid 24-symbol Frame Sync sequence followed by Header Block which has a correct CRC1 checksum.

The task continues until a valid Frame Sync plus Header Block has been found.

The search consists of two stages:

First of all the modem will attempt to match the incoming symbols against the 24-symbol Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Control Register.

Once a match has been found, the modem will read in the next 66 symbols as if they were a 'Header' block, decoding the symbols and checking the CRC1 checksum. If this is incorrect, the modem will resume the search, looking for a fresh Frame Sync pattern.

If the received CRC1 is correct, the 10 decoded data bytes will be placed into the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1' and the CRCERR bit cleared to '0'.

On detecting that the BFREE bit of the Status Register has gone to '1', the µC should read the 10 bytes from the Data Block Buffer and then write the next task to the modem's Command Register.

4.5.2.8 RHB: Read Header Block

This task causes the modem to read the next 66 symbols as a 'Header' Block, decoding them, placing the resulting 10 data bytes and the 2 received CRC1 bytes into the Data Block Buffer, and setting the BFREE and IRQ bits of the Status Register to '1'. When the task is complete it indicates that the µC may read the data from the Data Block Buffer and write the next task to the modem's Command Register.

The CRCERR bit of the Status Register will be set to '1' or '0' depending on the validity of the received CRC1 checksum bytes.

4.5.2.9 RILB: Read 'Intermediate' or 'Last' Block

This task causes the modem to read the next 66 symbols as an 'Intermediate' or 'Last' block (the µC should be able to tell from the 'Header' block how many blocks are in the frame and when to expect the 'Last' block).

In each case, it will decode the 66 symbols and place the resulting 12 bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete.

If an 'Intermediate' block is received then the µC should read out all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register, for a 'Last' block the µC need only read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum.

4.5.2.10 SFS: Search for Frame Sync

This task causes the modem to search the received signal for a 24-symbol sequence which matches the Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Mode Register.

When a match is found the modem will set the BFREE and IRQ bits of the Status Register to '1' to indicate to the µC that it should write the next task to the Command Register.

4.5.2.11 R4S: Read 4 Symbols

This task causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register is then set to '1' to indicate that the µC may read the data byte from the Data Block Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by SFS task.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.5.2.12 T24S: Transmit 24 Symbols

This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC or FEC.

Byte 0 of the Data Block Buffer is sent first, byte 5 last.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the data and command byte for the next task to the modem.

The tables below show what data needs to be written to the Data Block Buffer to transmit the MX919A Symbol and Frame Sync sequences:

'Symbol Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
+3	+3	-3	-3	Byte 0:	11110101	F5
+3	+3	-3	-3	Byte 1:	11110101	F5
+3	+3	-3	-3	Byte 2:	11110101	F5
+3	+3	-3	-3	Byte 3:	11110101	F5
+3	+3	-3	-3	Byte 4:	11110101	F5
+3	+3	-3	-3	Byte 5:	11110101	F5

'Frame Sync' Symbols				Values written to Data Block Buffer		
					Binary	Hex
-1	+1	-1	+1	Byte 0:	00100010	22
-1	+3	-3	+3	Byte 1:	00110111	37
-3	-1	+1	-3	Byte 2:	01001001	49
+3	+3	-1	+1	Byte 3:	11110010	F2
-3	-3	+1	+3	Byte 4:	01011011	5B
-1	-3	+1	+3	Byte 5:	00011011	1B

4.5.2.13 THB: Transmit Header Block

This task takes 10 bytes of data (Address and Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Header' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.14 TIB: Transmit Intermediate Block

This task takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Intermediate' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.15 TLB: Transmit Last Block

This task takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12 bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Last' Block.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.16 T4S: Transmit 4 Symbols

This command is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.5.2.17 RESET: Stop any current action

This 'task' takes effect immediately, and terminates any current action (task, AQSC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to '1', without setting the IRQ bit. It should be used when V_{DD} is applied, to set the modem into a known state.

Note: Due to delays in the transmit filter, it will take several symbol times for any change to appear at the TXOUT pin.

Task Timing

		Task	Time (symbol times)
t_1	Modem in idle state. Time from writing first task to application of first transmit bit to Tx RRC filter	Any	1 to 2
t_2	Time from application of first symbol of the task to the Tx RRC filter until BFREE goes to a logic '1'	T24S	5
		THB/TIB/TLB	16
		T4S	0
t_3	Time to transmit all symbols of the task	T24S	24
		THB/TIB/TLB	66
		T4S	4
t_4	Max time allowed from BFREE going to a logic '1' (high) for next task (and data) to be written to modem	T24S	18
		THB/TIB/TLB	49
		T4S	3
t_5	Time to receive all symbols of task	SFS	24 (minimum)
		SFSH	90 (minimum)
		RHB/RILB	66
		R4S	4
t_6	Maximum time between first symbol of task entering the de-interleave circuit and the task being written to modem	SFS	21
		SFSH	21
		RHB/RILB	49
		R4S	3
t_7	Maximum time from the last bit of the task entering the de interleave circuit to BFREE going to a logic '1' (high)	Any	1

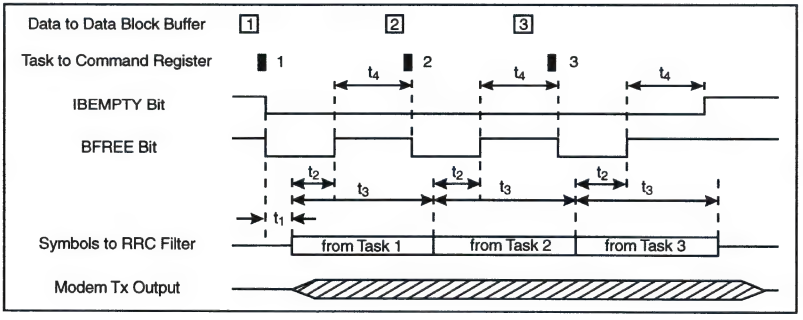


Figure 11: Transmit Task Timing Diagram

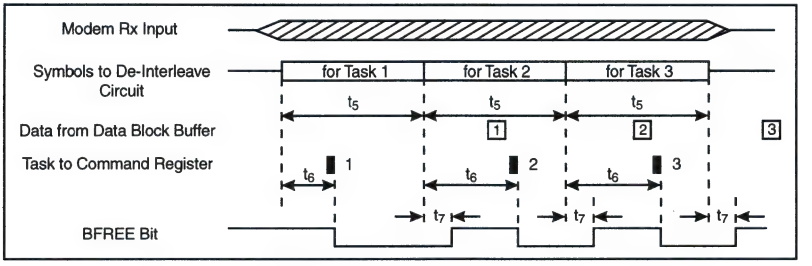


Figure 12: Receive Task Timing Diagram

4.5.2.18 RRC Filter Delay

The previous task timing figures are based on the signal at the input to the RRC filter (in transmit mode) or the input to the de-interleave buffer (in receive mode). There is an additional delay of about 8 symbol times through to the RRC filter in both transmit and receive modes, as illustrated below:

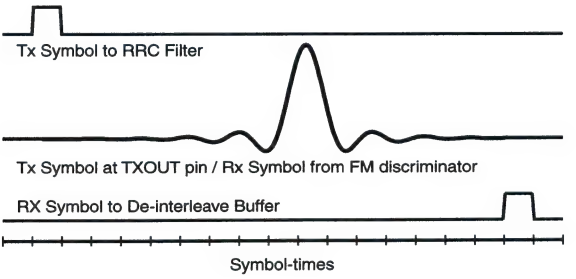
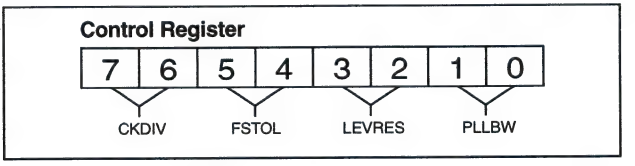

Tx Symbol to RRC Filter
Tx Symbol at TXOUT pin / Rx Symbol from FM discriminator
RX Symbol to De-interleave Buffer
Symbol-times

Figure 13: RRC Low Pass Filter Delay

4.5.3 Control Register

This 8-bit write-only register controls the modem's symbol rate, the response times of the receive clock extraction and signal level measurement circuits and the Frame Sync pattern recognition tolerance.



4.5.3.1 Control Register B7, B6: CKDIV - Clock Division Ratio

These bits control a frequency divider driven from the clock signal present at the $\overline{\text{XTAL}}$ pin, therefore determining the nominal symbol rate. The table below shows how symbol rates of 2400/4800/9600 symbols/sec may be obtained from common Xtal frequencies:

			Xtal Frequency (MHz)		
			2.4576	4.9152	9.8304
B7	B6	Division Ratio: Xtal Frequency/Symbol Rate	Symbol Rate (symbols/sec)		
0	0	512	4800	9600	
0	1	1024	2400	4800	9600
1	0	2048		2400	4800
1	1	4096			2400

Note: Device operation is not guaranteed below 2400 or above 9600 symbols/sec.

4.5.3.2 Control Register B5, B4: FSTOL - Frame Sync Tolerance

These two bits have no effect in transmit mode. In receive mode, they define the maximum number of mismatches allowed during a search for the Frame Sync pattern:

B5	B4	Mismatches allowed
0	0	0
0	1	2
1	0	4
1	1	6

Note: A single 'mismatch' is defined as the difference between two adjacent symbol levels, thus if the symbol '+1' were expected, then received symbol values of '+3' and '-1' would count as 1 mismatch, a received symbol value of '-3' would count as 2 mismatches.

4.5.3.3 Control Register B3, B2: LEVRES - Level Measurement Modes

These two bits have no effect in transmit mode. In receive mode they set the 'normal' operating mode of the Rx signal amplitude and dc offset measuring circuits. This setting will be temporarily overridden by the automatic sequencing of an AQLEV command.

B3	B2	Mode
0	0	Hold
0	1	Slow Peak Detect
1	0	Lossy Peak Detect
1	1	Clamp

For most applications these two bits should be set to 'Slow Peak Detect' mode, in which the peak positive and peak negative excursions of the received signal (after filtering) are measured to establish the amplitude and dc offset of the signal. The decay time-constant of the peak rectifier circuits used in this mode is approximately 750 symbol times.

The 'Hold' setting freezes the stored values of the current amplitude and offset measurements which may be used to improve performance during short fades or while the radio is switched from receive mode for the transmission of a short acknowledgment. It should be noted, that the measured amplitude and offset values are stored on the external capacitors C7 and C8 and will decay gradually when the 'Hold' setting is chosen, the discharge time-constant being approximately 750 symbol times.

The 'Lossy Peak Detect' setting is similar to 'Slow Peak Detect' except the decay time-constant of the peak detectors are reduced to approximately 25 symbol times to provide a faster response to signal changes at the expense of reduced BER performance. This mode is used by the automatic Level Measurement acquisition sequence but may also be useful in non-standard systems.

The 'Clamp' setting is primarily intended for use by the automatic Level Measurement Acquisition Sequence as described in Section 5.3, but may also be useful in non-standard systems. In this mode, the DOC1 and DOC2 pins are connected directly to the output of the circuit that normally drives the peak detectors.

4.5.3.4 Control Register B1, B0: PLLBW - Phase-Locked Loop Modes

These two bits have no effect in transmit mode. In receive mode, they set the 'normal' bandwidth of the Rx clock extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the automatic sequencing of an AQSC command.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

B1	B0	PLL Mode	Working Bandwidth (±ppm)
0	0	Hold	-
0	1	Narrow Bandwidth	20
1	0	Medium Bandwidth	100
1	1	Wide Bandwidth	650

Note: 'Working Bandwidths' are the maximum difference between the actual received symbol rate and the nominal rate determined by the tolerance of the modem's Xtal frequency, to provide minimal degradation of a reasonably random received signal.

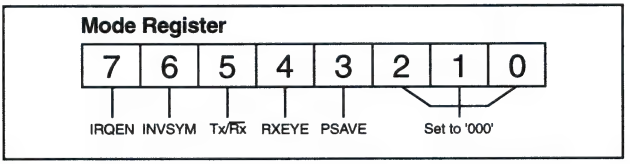
The minimum bandwidth consistent with the transmit and receive modem symbol rate tolerances should be chosen, i.e. if the Xtals used with both modems have accuracies within ± 50ppm, then the PLLBW bits should be set to '10' ('Medium Bandwidth'). However, to allow the PLL to settle quickly, it is recommended that when very close tolerance Xtals are used, then the PLLBW bits should be set to 'Medium' whenever an AQSC is triggered, and only changed to 'Narrow' about 200 symbol times later.

The 'Wide Bandwidth' setting is intended for message acquisition in systems where the µC cannot detect the start of a received message, as it allows the modem to respond rapidly to fresh messages and recover rapidly after a fade without µC intervention - although at the cost of reduced Bit Error Rate vs Signal to Noise performance.

The 'Hold' setting disables the PLL feedback loop. It may be used during signal fades.

4.5.4 Mode Register

The contents of this 8-bit write only register, control the basic operating modes of the modem:



4.5.4.1 Mode Register B7: IRQEN - $\overline{IRQ}$ Output Enable

When this bit is set to '1', the $\overline{IRQ}$ chip output pin is pulled low (V_{SS}) when the IRQ bit of the Status Register is a '1'.

4.5.4.2 Mode Register B6: INVSYM - Invert Symbols

This bit controls the polarity of the transmitted and received symbol voltages.

B6	Symbol	Signal at TXOUT	Signal at RXAMPOUT
0	'+3'	Above V_{BIAS}	Below V_{BIAS}
	'-3'	Below V_{BIAS}	Above V_{BIAS}
1	'+3'	Below V_{BIAS}	Above V_{BIAS}
	'-3'	Above V_{BIAS}	Below V_{BIAS}

4.5.4.3 Mode Register B5: TX/$\overline{RX}$ - Tx/Rx Mode

Setting this bit to '1' places the modem into the Transmit mode, clearing it to '0' puts the modem into the Receive mode.

Note: Changing between receive and transmit modes will cancel any current task.

4.5.4.4 Mode Register B4: RXEYE - Show Rx Eye

This bit should normally be set to '0'. Setting it to '1' when the modem is in receive mode configures the modem for a special test mode, in which the input of the Tx output buffer is connected to the Rx Symbol/Clock extraction circuit at a point which carries the equalized receive signal. This may be monitored with an oscilloscope (at the TXOUT pin itself), to assess the quality of the complete radio channel including the Tx and Rx modem filters, the Tx modulator and the Rx IF filters and FM demodulator.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

The resulting eye diagram (for reasonably random data) should ideally be as shown in the following Figure 14, with 4 'crisp' and equally spaced crossing points.

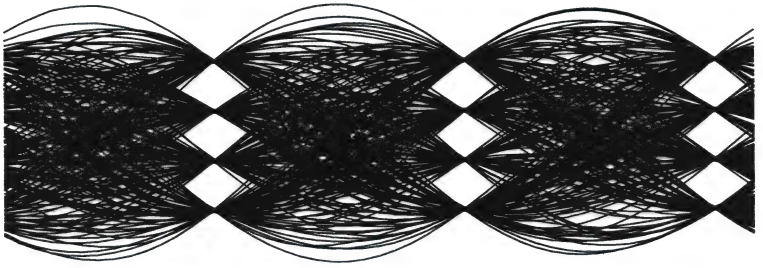


Figure 14: Ideal 'RXEYE' Signal

4.5.4.5 Mode Register B3: PSAVE - Powersave

When this bit is a '1', the modem will be in a 'powersave' mode in which the internal filters, the Rx Symbol & Clock extraction circuits and the Tx output buffer will be disabled, and the TXOUT pin will be connected to the V_{BIAS} through a high value resistance. The Xtal clock oscillator, Rx input amplifier and the µC interface logic will continue to operate.

Setting the PSAVE bit to '0' restores power to all of the chip circuitry.

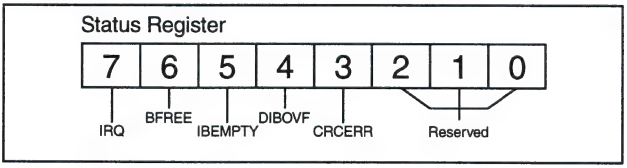
Note: The internal filters, and therefore the TXOUT pin, in transmit mode will take approximately 20 symbol-times to settle after the PSAVE bit has gone from '1' to '0'.

4.5.4.6 Mode Register B2, B1, B0

These bits should be set to '000'.

4.5.5 Status Register

This register may be read by the µC to determine the current state of the modem.



4.5.5.1 Status Register B7: IRQ - Interrupt Request

This bit is set to '1' by:

The Status Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register TX/$\overline{RX}$ bit.

The Status Register IBEMPTY bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register TX/$\overline{RX}$ bit.

The Status Register DIBOVF bit going from '0' to '1'.

The IRQ bit is cleared to '0' immediately after a read of the Status Register.

If the IRQEN bit of the Mode Register is '1', then the chip $\overline{IRQ}$ output will be pulled low (V_{SS}) when the IRQ bit is set to '1', and will go high impedance when the Status Register is read.

4.5.5.2 Status Register B6: BFREE - Data Block Buffer Free

This bit reflects the availability of the Data Block Buffer and is cleared to '0' when a task other than NULL or RESET is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status Register IRQ bit to '1') by the modem when the modem is ready for the µC to write new data to the Data Block Buffer and the next task to the Command Register.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

In receive mode, the BFREE bit is set to '1' (also setting the Status Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Block Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1' - but without setting the IRQ bit - by a RESET task or when the Mode Register TX/$\overline{RX}$ bit is changed.

4.5.5.3 Status Register B5: IBEMPTY - Interleave Buffer Empty

In transmit mode, this bit will be set to '1' - also setting the IRQ bit - when less than two symbols remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

The bit is also set to '1' by a RESET task or by a change of the Mode Register TX/$\overline{RX}$ bit, but in these cases the IRQ bit will not be set.

The bit is cleared to '0' within one symbol time after a task other than NULL or RESET is written to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid level (half-way between '+1' and '-1') signal will be sent to the RRC filter.

In receive mode this bit will be '0'.

4.5.5.4 Status Register B4: DIBOVF - De-Interleave Buffer Overflow

In receive mode this bit will be set to '1' - also setting the IRQ bit - when a RHB, RILB or R4S task is written to the Command Register too late to allow continuous reception.

The bit is cleared to '0' immediately after reading the Status Register, by writing a RESET task to the Command Register or by changing the TX/$\overline{RX}$ bit of the Mode Register.

In transmit mode this bit will be '0'.

4.5.5.5 Status Register B3: CRCERR - CRC Checksum Error

In receive mode this bit will be updated at the end of a SFSH, RHB or RILB task to reflect the result of the receive CRC check. '0' indicates that the CRC was received correctly, '1' indicates an error.

Note: This bit should be ignored when an 'Intermediate' block (which does not have an integral CRC) is received.

The bit is cleared to '0' by a RESET task, or by changing the TX/$\overline{RX}$ bit of the Mode Register. In transmit mode this bit is '0'.

4.5.5.6 Status Register B2, B1, B0

These bits are reserved for future use.

4.5.6 Data Quality Register

In receive mode, the MX919A continually measures the 'quality' of the received signal, by comparing the actual received waveform over the previous 64 symbol times against an internally generated 'ideal'.

The result is placed into bits 3-7 of the Data Quality Register for the µC to read at any time, bits 0-2 being always set to '0'. Figure 15 shows how the value (0-255) read from the Data Quality Register varies with received signal-to-noise ratio:

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

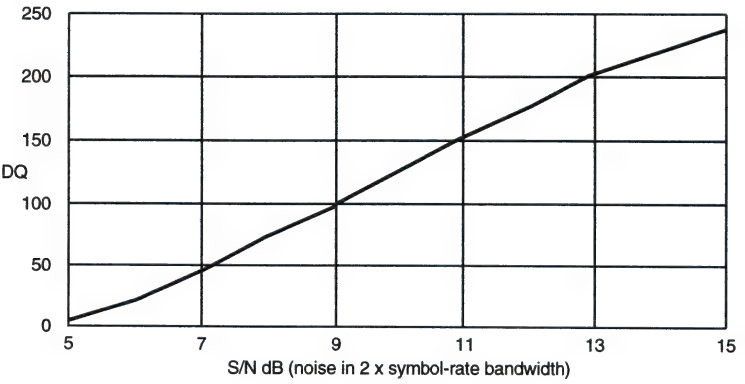


Figure 15: Typical Data Quality Reading vs S/N

In transmit mode and for 64 symbol times after enabling receive mode or after starting an AQSC or AQLEV sequence the value in the Data Quality Register will be invalid.

4.6 CRC, FEC and Interleaving

4.6.1 Cyclic Redundancy Codes

4.6.1.1 CRC1

This is a sixteen-bit CRC check code contained in bytes 10 and 11 of the Header Block. It is calculated by the modem from the first 80 bits of the block (Bytes 0 to 9 inclusive) using the generator polynomial:

$$x^{16} + x^{12} + x^5 + 1$$

4.6.1.2 CRC2

This is a thirty-two-bit CRC check code contained in bytes 8 to 11 of the 'Last' Block. It is calculated by the modem from all of the data and pad bytes in the Intermediate Blocks and in the first 8 bytes of the Last Block using the generator polynomial:

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1$$

Note: In receive mode the CRC2 checksum circuits are initialized on completion of any task other than NULL or RILB. In transmit mode the CRC2 checksum circuits are initialized on completion of any task other than NULL, TIB or TLB.

4.6.1.3 Forward Error Correction

In transmit mode, the MX919A uses a Trellis Encoder to translate the 96 bits (12 bytes) of a 'Header', 'Intermediate' or 'Last' Block into a 66-symbol sequence which includes FEC information.

In receive mode, the MX919A decodes the received 66 symbols of a block into 96 bits of binary data using a 'Soft Decision' Viterbi algorithm to perform decoding and error correction.

4.6.1.4 Interleaving

The 66 symbols of a 'Header', 'Intermediate' or 'Last' block are interleaved by the modem before transmission to provide protection against the effects of noise bursts and short fades.

In receive mode, the MX919A de-interleaves the received symbols prior to decoding.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

5. Application

5.1 Transmit Frame Example

The operations needed to transmit a single Frame consisting of Symbol and Frame Sync sequences, and one each Header, Intermediate and Last blocks are provided below:

1. Ensure that the Control Register has been loaded with a suitable CKDIV value, that the IRQEN and bits of the Mode Register are '1', the RXEYE and PSAVE bits are '0' and the INVSYM bit is set appropriately.
2. Read the Status Register to ensure that the BFREE bit is '1', then write 6 Symbol Sync bytes to the Data Block Buffer and a T24S task to the Command Register.
3. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
4. Write 6 Frame Sync bytes to the Data Block Buffer and a T24S task to the Command Register.
5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
6. Write 10 Header Block bytes to the Data Block Buffer and a THB task to the Command Register.
7. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
8. Write 12 Intermediate Block bytes to the Data Block Buffer and a TIB task to the Command Register.
9. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
10. Write 8 Last Block bytes to the Data Block Buffer and a TLB task to the Command Register.
11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
12. Wait for another interrupt from the modem, read the Status Register; the IRQ, BFREE and IBEMPTY bits should be '1'.

Note: The final symbol of the frame will start to appear approximately 2 symbol times after the Status Register IBEMPTY bit goes to '1'; a further 16 symbol times should be allowed for the symbol to pass completely through the RRC filter.

Figure 16 and Figure 17 illustrate the host µC routines needed to send a single Frame consisting of Symbol and Frame Sync patterns, a Header block, and any number of Intermediate blocks and one Last Block. It is assumed that the Tx Interrupt Service Routine Figure 17 is called when the MX919A $\overline{IRQ}$ output line goes low.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

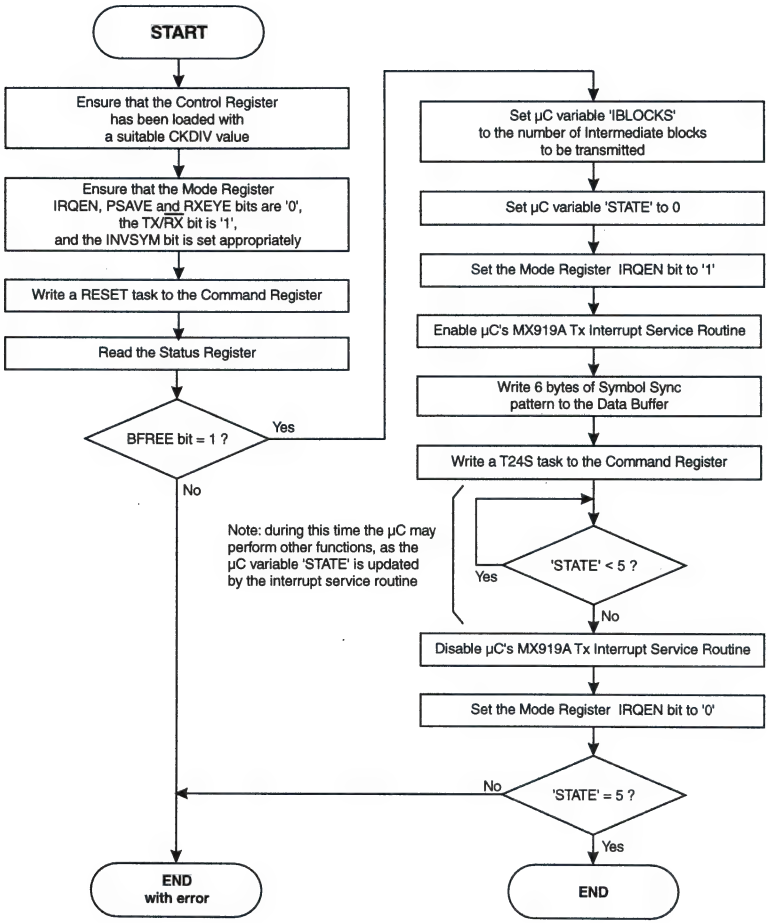

START
Ensure that the Control Register has been loaded with a suitable CKDIV value
Ensure that the Mode Register IRQEN, PSAVE and RXEYE bits are '0', the TX/RX bit is '1', and the INVSYM bit is set appropriately
Write a RESET task to the Command Register
Read the Status Register
BFREE bit = 1 ?
Yes
No
Set µC variable 'IBLOCKS' to the number of Intermediate blocks to be transmitted
Set µC variable 'STATE' to 0
Set the Mode Register IRQEN bit to '1'
Enable µC's MX919A Tx Interrupt Service Routine
Write 6 bytes of Symbol Sync pattern to the Data Buffer
Write a T24S task to the Command Register
Note: during this time the µC may perform other functions, as the µC variable 'STATE' is updated by the interrupt service routine
'STATE' < 5 ?
Yes
No
Disable µC's MX919A Tx Interrupt Service Routine
Set the Mode Register IRQEN bit to '0'
'STATE' = 5 ?
No
Yes
END with error
END

Figure 16: Transmit Frame Example Flowchart, Main Program

Note: The RESET command in Figure 16 and the practice of disabling the MX919A's $\overline{IRQ}$ output when not needed are not essential but can eliminate problems during debugging and if errors occur in operation The CRC bit should be set appropriately when a byte is written to the Command Register

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

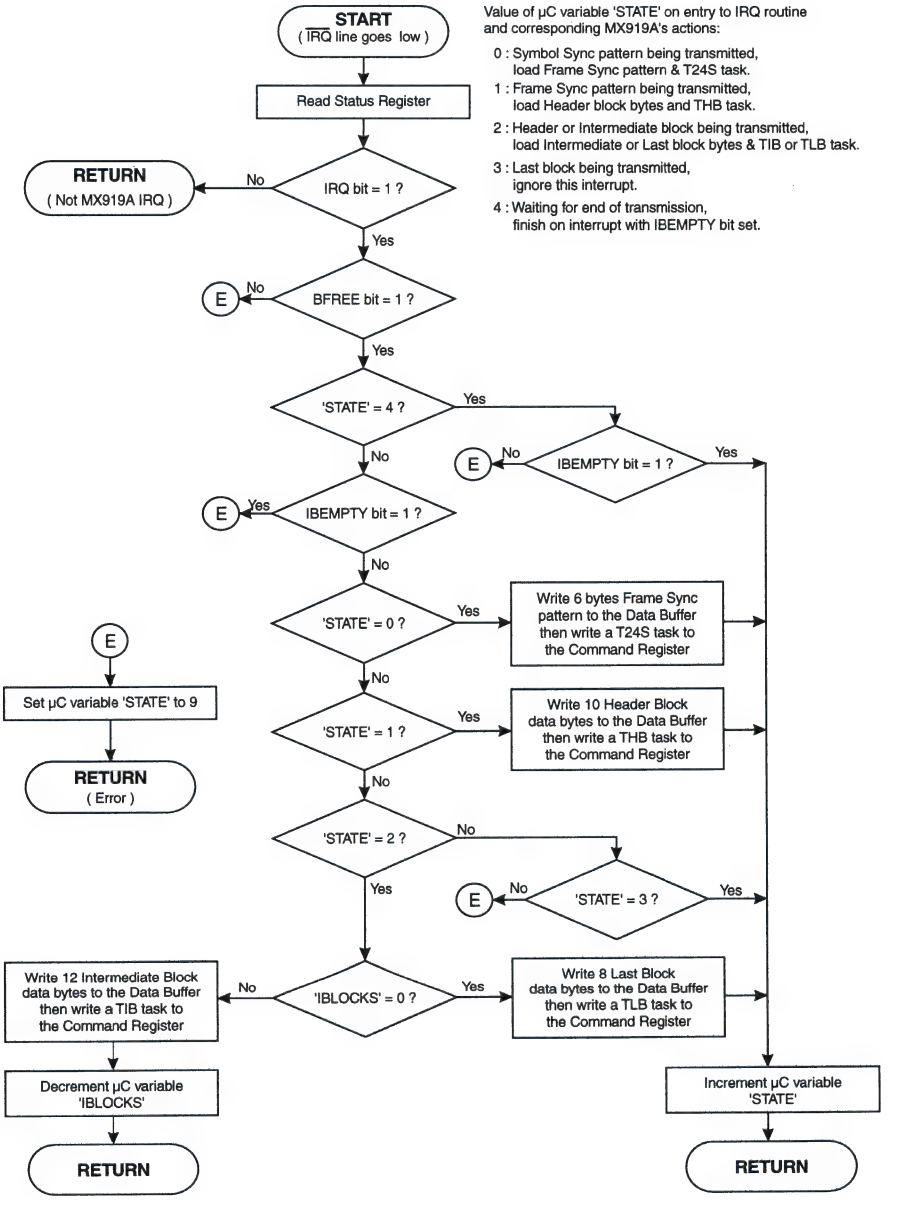

START
(IRQ line goes low)
Read Status Register
IRQ bit = 1 ?
No
RETURN
(Not MX919A IRQ)
Yes
BFREE bit = 1 ?
No
E
Yes
'STATE' = 4 ?
Yes
No
IBEMPTY bit = 1 ?
E
No
Yes
IBEMPTY bit = 1 ?
E
Yes
No
'STATE' = 0 ?
Yes
Write 6 bytes Frame Sync pattern to the Data Buffer then write a T24S task to the Command Register
No
'STATE' = 1 ?
Yes
Write 10 Header Block data bytes to the Data Buffer then write a THB task to the Command Register
No
'STATE' = 2 ?
No
Yes
'STATE' = 3 ?
E
No
Yes
'IBLOCKS' = 0 ?
No
Yes
Write 12 Intermediate Block data bytes to the Data Buffer then write a TIB task to the Command Register
Write 8 Last Block data bytes to the Data Buffer then write a TLB task to the Command Register
Decrement µC variable 'IBLOCKS'
RETURN
Increment µC variable 'STATE'
RETURN
E
Set µC variable 'STATE' to 9
RETURN
(Error)
Value of µC variable 'STATE' on entry to IRQ routine and corresponding MX919A's actions:
0 : Symbol Sync pattern being transmitted, load Frame Sync pattern & T24S task.
1 : Frame Sync pattern being transmitted, load Header block bytes and THB task.
2 : Header or Intermediate block being transmitted, load Intermediate or Last block bytes & TIB or TLB task.
3 : Last block being transmitted, ignore this interrupt.
4 : Waiting for end of transmission, finish on interrupt with IBEMPTY bit set.

Figure 17: Tx Interrupt Service Routine

5.2 Receive Frame Example

The operations needed to receive a single Frame consisting of Symbol and Frame Sync sequences and one each Header, Intermediate and Last blocks are shown below;

1. Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values, and that the IRQEN bit of the Mode Register is '1', the TX/$\overline{RX}$ PSAVE, and RXEYE bits are '0', and the INVSYM bit is set appropriately.
2. Wait until the received carrier has been present for at least 8 symbol times (see Section 5.3).
3. Read the Status Register to ensure that the BFREE bit is '1'.
4. Write a byte containing a SFSH task and with the AQSC and AQLEV bits set to '1' to the Command Register.
5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the CRCERR and DIBOVF bits should be '0'.
6. Check that the CRCERR bit of the Status Register is '0' and read 10 Header Block bytes from the Data Block Buffer.
7. Write a RILB task to the Command Register.
8. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
9. Read 12 Intermediate Block bytes from the Data Block Buffer.
10. Write a RILB task to the Command Register.
11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
12. Check that the CRCERR bit of the Status Register is '0' and read the 8 Last Block bytes from Data Buffer.

Figure 18 and Figure 19 illustrate the host µC routines needed to receive a single Frame consisting of Symbol and Frame Sync patterns, a Header Block, any number of Intermediate blocks and one Last block. It is assumed that the Rx Interrupt Service Routine Figure 19 is called when the MX919A's $\overline{IRQ}$ output goes low.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

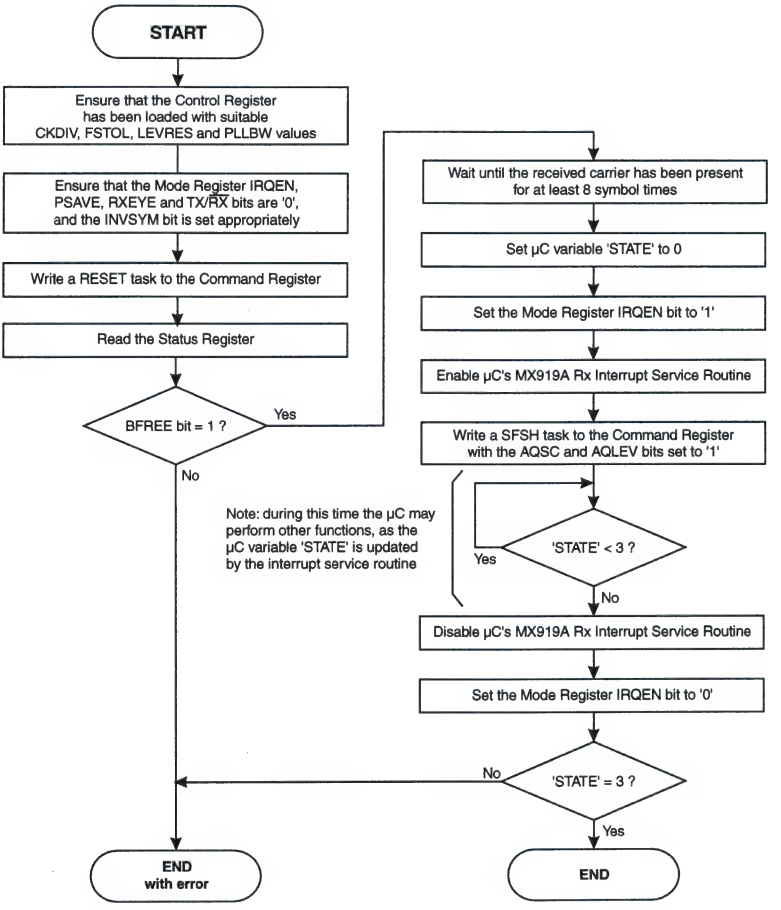

START
Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values
Ensure that the Mode Register IRQEN, PSAVE, RXEYE and TX/RX bits are '0', and the INVSYM bit is set appropriately
Write a RESET task to the Command Register
Read the Status Register
BFREE bit = 1 ?
Yes
No
Wait until the received carrier has been present for at least 8 symbol times
Set µC variable 'STATE' to 0
Set the Mode Register IRQEN bit to '1'
Enable µC's MX919A Rx Interrupt Service Routine
Write a SFSH task to the Command Register with the AQSC and AQLEV bits set to '1'
Note: during this time the µC may perform other functions, as the µC variable 'STATE' is updated by the interrupt service routine
'STATE' < 3 ?
Yes
No
Disable µC's MX919A Rx Interrupt Service Routine
Set the Mode Register IRQEN bit to '0'
'STATE' = 3 ?
No
Yes
END with error
END

Figure 18: Receive Frame Example Flowchart, Main Program

Note: The RESET command in Figure 18 and the practice of disabling the MX919A's $\overline{IRQ}$ output when not needed are not essential but can eliminate problems during debugging and if errors occur in operation. The CRC bit should be set appropriately when a byte is written to the Command Register.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

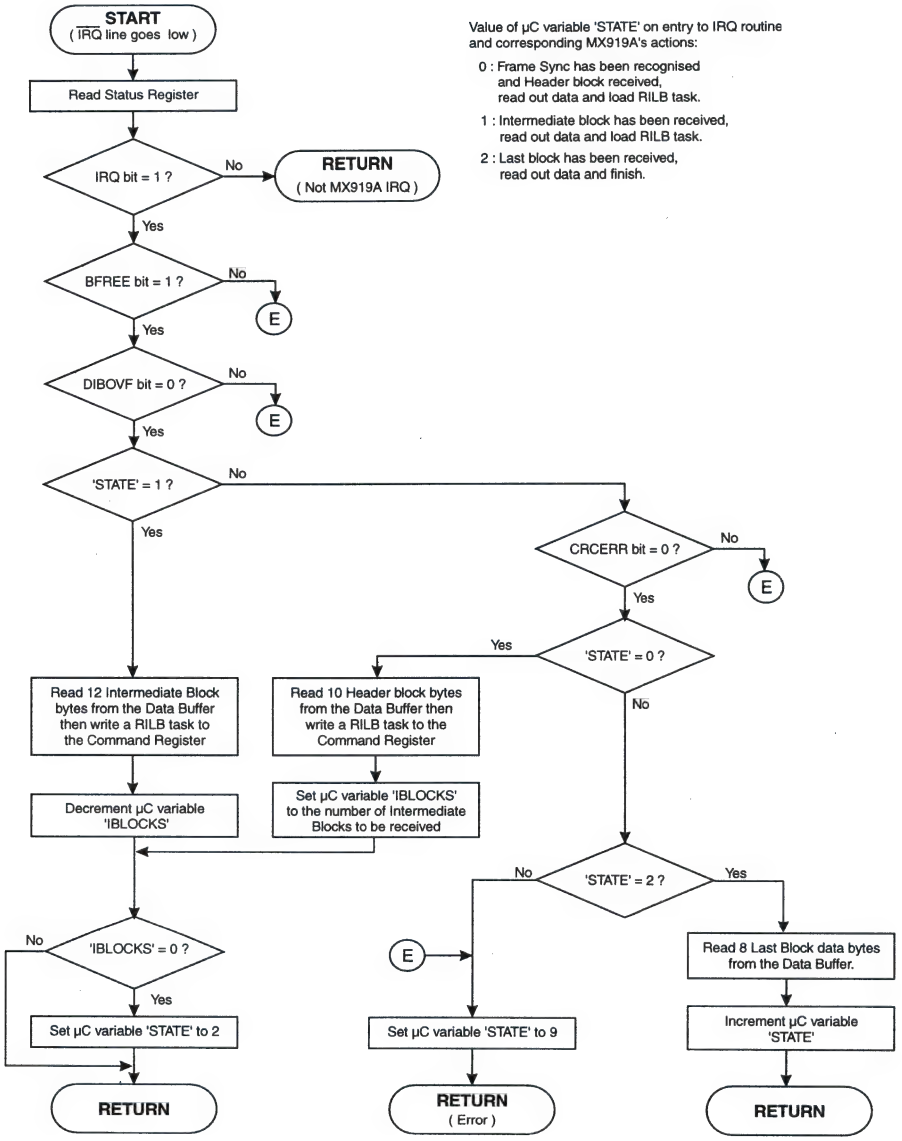

START
(IRQ line goes low)
Read Status Register
IRQ bit = 1 ?
No
RETURN
(Not MX919A IRQ)
Yes
BFREE bit = 1 ?
No
E
Yes
DIBOVF bit = 0 ?
No
E
Yes
'STATE' = 1 ?
No
Yes
CRCERR bit = 0 ?
No
E
Yes
'STATE' = 0 ?
Yes
No
Read 12 Intermediate Block bytes from the Data Buffer then write a RILB task to the Command Register
Read 10 Header block bytes from the Data Buffer then write a RILB task to the Command Register
Decrement µC variable 'IBLOCKS'
Set µC variable 'IBLOCKS' to the number of Intermediate Blocks to be received
'STATE' = 2 ?
No
Yes
'IBLOCKS' = 0 ?
No
Yes
E
Read 8 Last Block data bytes from the Data Buffer.
Set µC variable 'STATE' to 2
Set µC variable 'STATE' to 9
Increment µC variable 'STATE'
RETURN
RETURN
(Error)
RETURN
Value of µC variable 'STATE' on entry to IRQ routine and corresponding MX919A's actions:
0 : Frame Sync has been recognised and Header block received, read out data and load RILB task.
1 : Intermediate block has been received, read out data and load RILB task.
2 : Last block has been received, read out data and finish.

Figure 19: Rx Interrupt Service routine

Note: This routine assumes that the number of Intermediate blocks in the Frame is contained within the Header Block Data

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. #20480151.002

5.3 Clock Extraction and Level Measurement Systems

The MX919A is intended for use in systems where the Symbol Sync pattern is transmitted immediately on start-up of the transmitter.

When the carrier is detected by the receiver or when the receiver is switched to another channel, the controlling µC should wait approximately 8 symbol times for the received signal to propagate through the modem's RRC filter then issue a SFS or SFSH task with the AQSC and AQLEV bits set to '1'. The 8-symbol delay can usefully be included in the carrier detect circuitry.

Setting the AQSC and AQLEV bits to '1' triggers the modem's automatic Symbol Clock Extraction and Level Measurement acquisition sequences, which are designed to measure the received symbol timing, amplitude and dc offset as quickly as possible during the Symbol Sync period before switching to more accurate - but slower - measurement modes for the remainder of the received message.

Note: If the acquisition sequences are triggered after the Symbol Sync period - as can happen when the receiver is switched to another channel - they will still function correctly, but will take much longer to acquire accurate level and timing information.

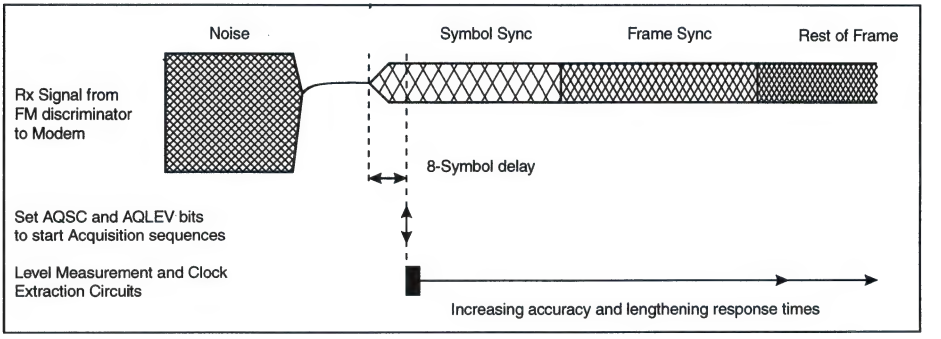

Noise
Symbol Sync
Frame Sync
Rest of Frame
Rx Signal from FM discriminator to Modem
8-Symbol delay
Set AQSC and AQLEV bits to start Acquisition sequences
Level Measurement and Clock Extraction Circuits
Increasing accuracy and lengthening response times

Figure 20: Acquisition Sequence Timing

The operation of the Level Acquisition Sequence depends on the settings of the Control Register LEVRES bits:

LEVRES setting:	B3	B2	Details of Level Acquisition Sequence
'Hold'	0	0	1 symbol time of 'Clamp' mode then 15 symbol times of 'Lossy Peak Detect' mode before reverting to 'Hold' mode.
'Slow Peak Detect'	0	1	1 symbol time of 'Clamp' mode then 15 symbol times of 'Lossy Peak Detect' mode before reverting to 'Slow Peak Detect' mode.
'Lossy Peak Detect'	1	0	1 symbol time of 'Clamp' mode before reverting to 'Lossy Peak Detect' mode
'Clamp'	1	1	Remain in 'Clamp' mode.

The 1-symbol 'Clamp' time at the start of these sequences is used to make an initial measurement of the dc offset present on the received signal, after which the 'Lossy Peak Detect' period is used to estimate the signal amplitude.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

The operation of the Symbol Clock Acquisition Sequence depends on the settings of the Control Register PLLBW bits:

PLLBW setting:	B1	B0	Details of Symbol Clock Acquisition Sequence
'Hold'	0	0	16 symbol times of 'Extra-wide BW' mode followed by 30 symbol times of 'Wide BW' mode before reverting to 'Hold' mode.
'Narrow' BW	0	1	16 symbol times of 'Extra-wide BW' mode followed by 30 symbol times of 'Wide BW' mode before reverting to 'Narrow BW' mode.
'Medium BW'	1	0	16 symbol times of 'Extra-wide BW' mode followed by 30 symbol times of 'Wide BW' before reverting to 'Medium BW' mode.
'Wide BW'	1	1	16 symbol times of 'Extra-wide BW' mode before reverting to 'Wide BW' mode.

Note: The 'Extra-wide BW' PLL mode is designed to synchronize rapidly to the '+3 +3 -3 -3 ...' Symbol Sync pattern and is available only as part of an automatic acquisition sequence.

Although it is not recommended, it is possible to use the modem in a non-standard system where there is an indeterminate delay between the transmitter start-up and the Symbol Sync pattern, or where a receive carrier detect signal is not available to the controlling µC. In these cases the Symbol Sync pattern should be extended to about 100 symbols, and the Control Register LEVRES bits should be set to 'Lossy Peak Detect' and the PLLBW bits to 'Wide BW' before initiating a 'SFS + AQSC + AQLEV' task. Once the Frame Sync pattern has been detected, the Control Register settings may be changed to 'Slow Peak Detect' and 'Medium' or 'Narrow' PLL bandwidth for the remainder of the received message.

5.4 AC Coupling

For a practical circuit, ac coupling from the modem's transmit output to the frequency modulator and between the receiver's frequency discriminator and the receive input of the modem may be desired. There are, however, two problems:

1. AC Coupling of the signal degrades the Bit Error Rate performance of the modem. The following graph illustrates the typical bit error rates at 4800 symbols/sec (without FEC) for differing degrees of ac coupling:

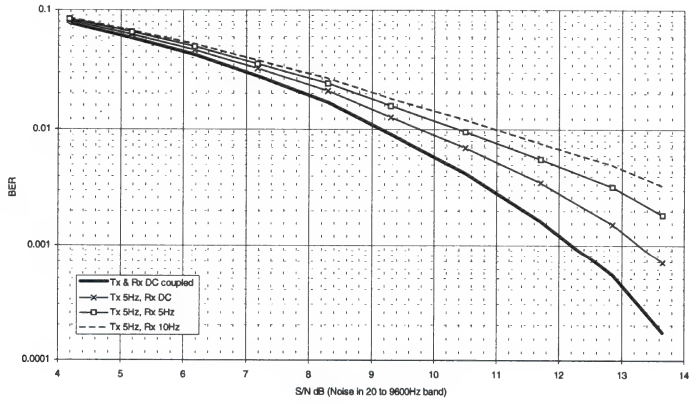


Figure 21: Effect of AC Coupling on BER

2. Any AC Coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated in Figure 22 below, the time for this step to decay to 37% of its original value is 'RC' where:

$$RC = 1/(2 \times \pi \times \text{the 3dB cut-off frequency of the RC network})$$

which is 32 msec, or 153 symbol times at 4800 symbols/sec, for a 5Hz network.

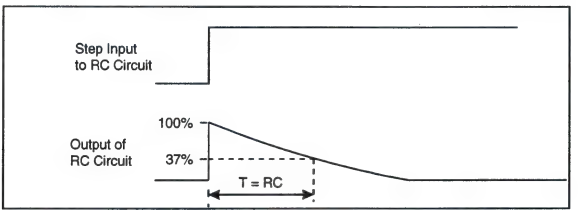


Figure 22: Decay Time - AC Coupling

In general, it is best to DC Couple the receiver discriminator to the modem, and to ensure that any AC Coupling to the transmitter's frequency modulator has a -3dB cut-off frequency of no higher than 5Hz (for 4800 symbols/sec).

5.5 Radio Performance

The maximum data rate that can be transmitted over a radio channel using these modems depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Symbol rate.
- Peak carrier deviation (modulation index).
- Tx and Rx reference oscillator accuracies.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 4800 symbols/sec can be achieved (subject to local regulatory requirements) over a system with 12.5kHz channel spacing if the transmitter frequency deviation is set to ±2.5kHz peak for a repetitive ' +3 +3 -3 -3 ... ' pattern and the maximum difference between transmitter and receiver 'carrier' frequencies is less than 2400Hz.

The modulation scheme employed by these modems is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. However; this does place constraints on the performance of the radio. Particular attention must be paid to:

- Linearity, frequency and phase response of the Tx Frequency Modulator. For a 4800 symbols/sec system, the frequency response should be within ±2dB over the range 3Hz to 5kHz, relative to 2400Hz.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a dc offset at the discriminator output.

Viewing the received signal eye - using the Mode Register RXEYE function - gives a good indication of the overall transmitter/receiver performance.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

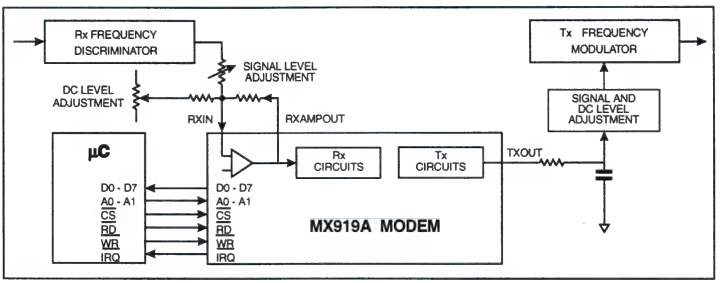


Figure 23: Typical Connections between Radio and MX919A

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW, LH, P Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above °C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
D5 Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above °C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Symbol Rate		2400	9600	Symbols/sec
Temperature		-40	85	°C
Xtal Frequency		1.0	10.0	MHz

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 4.9152MHz, Symbol Rate = 4800 symbols/sec,
Noise Bandwidth = 0 to 9600Hz, V_{DD} = 5.0V @ T_{AMB} = 25°C

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1		4.0	10.0	mA
I_{DD} (V_{DD} = 3.3V)	1		2.5	6.3	mA
I_{DD} (Powersave Mode)	1		1.5		mA
I_{DD} (Powersave Mode, V_{DD} = 3.3V)	1		0.6		mA
AC Parameters					
Tx Output					
TXOUT Impedance	2		1.0	2.5	kΩ
Signal Level	3	0.8	1.0	1.2	V_{P-P}
Output DC Offset wrt V_{DD} /2	4	-0.25		0.25	V
Rx Input					
RXIN Impedance (at 100Hz)			10.0		MΩ
RXIN Amp Voltage Gain (input = 1mV_{RMS} at 100Hz)			300		V/V
Input Signal Level	5	0.7	1.0	1.3	V_{P-P}
DC Offset wrt V_{DD} /2	5	-0.5		0.5	V
Xtal/Clock Input					
'High' Pulse Width	6	40			ns
'Low' Pulse Width	6	40			ns
Input Impedance (at 100Hz)		10.0			MΩ
Gain (input = 1 mV_{RMS} at 100Hz)		20			dB
µC Interface					
Input Logic "1" Level	7, 8	70%			V_{DD}
Input Logic "0" Level	7, 8			30%	V_{DD}
Input Leakage Current (V_{IN} = 0 to V_{DD})	7, 8	-5.0		5.0	µA
Input Capacitance	7, 8		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)	8	92%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)	8, 9			8%	V_{DD}
'Off' State Leakage Current (V_{OUT} = V_{DD})	9			10	µA

Operating Characteristics Notes:

1. Not including any current drawn from the modem pins by external circuitry other than the Xtal oscillator.
2. Small signal impedance
3. Measured after the external RC filter (R4/C5) for a "+3 +3 -3 -3...." symbol sequence, (output level is proportional to V_{DD}).
4. Measured at the TXOUT pin with the modem in the Tx idle mode.
5. For optimum performance, measured at RXAMPOUT pin, for a "...+3 +3 -3 -3..." symbol sequence optimum level is proportional to V_{DD}.
6. Timing for an external input to the CLOCK/XTAL pin.
7. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0 and A1 pins.
8. D0 - D7 pins.
9. $\overline{IRQ}$ pin.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Timing

µC Parallel Interface Timings (ref. Figure 24)		Notes	Min.	Typ.	Max.	Units
t_{ACSL}	Address valid to $\overline{CS}$ low time		0			ns
t_{AH}	Address hold time		0			ns
t_{CSH}	$\overline{CS}$ hold time		0			ns
t_{CSHI}	$\overline{CS}$ high time	1	6			clock cycles
t_{CSRWL}	$\overline{CS}$ to $\overline{WR}$ or $\overline{RD}$ low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90			ns
t_{RHCSL}	$\overline{RD}$ high to $\overline{CS}$ low time (write)		0			ns
t_{RACL}	Read access time from $\overline{CS}$ low	2			175	ns
t_{RARL}	Read access time from $\overline{RD}$ low	2			145	ns
t_{RL}	$\overline{RD}$ low time		200			ns
t_{RX}	$\overline{RD}$ high to D0-D7 3-state time				50	ns
t_{WHCSL}	$\overline{WR}$ high to $\overline{CS}$ low time (read)		0			ns
t_{WL}	$\overline{CS}$ low time		200			ns

Timing Notes:

1. Xtal/Clock cycles at the XTAL/CLOCK pin.
2. With 30pF max to V_{SS} on D0 - D7 pins.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

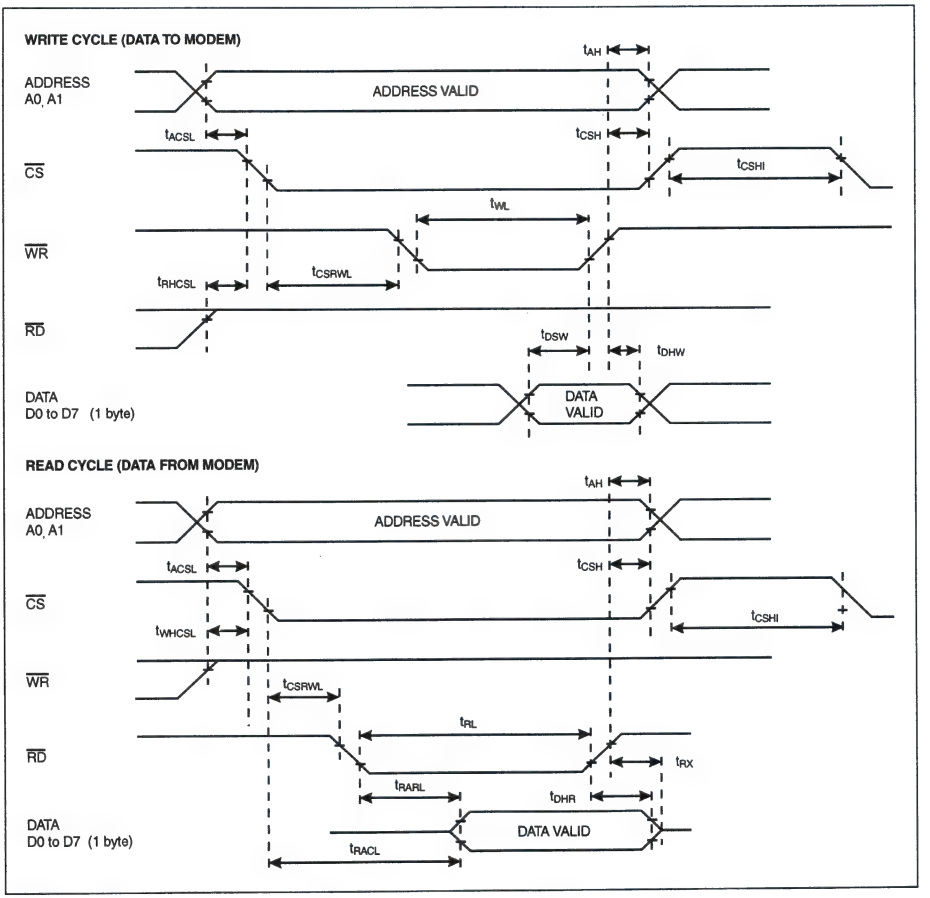


Figure 24: µC Parallel Interface Timings

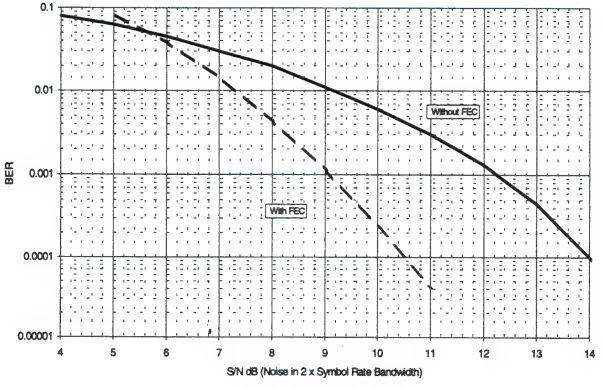
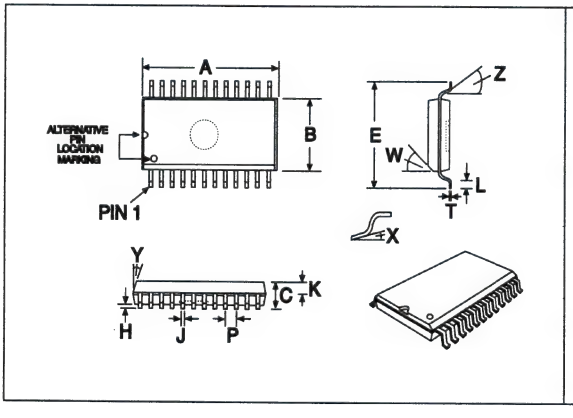


Figure 25: Typical Bit Error Rate With and Without FEC

6.2 Packaging



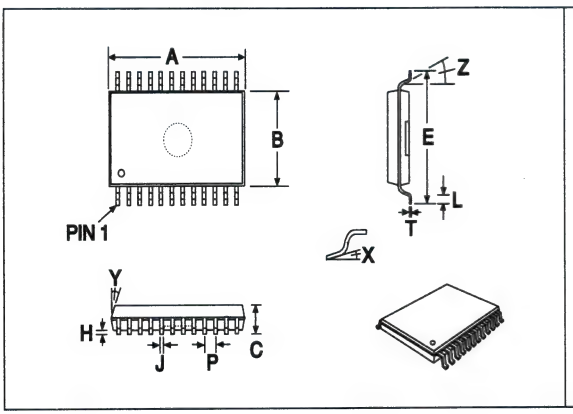
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 26: 24-pin SOIC Mechanical Outline: *order as part no. MX919ADW*

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

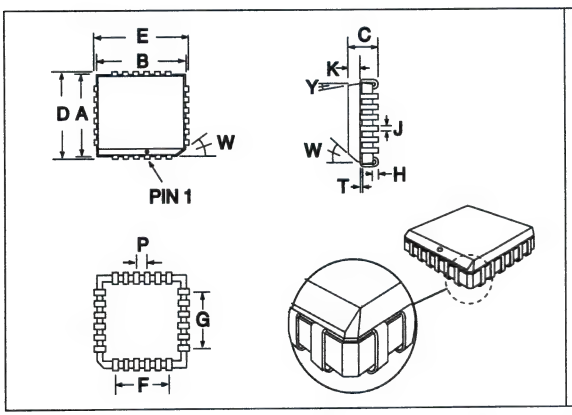


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 27: 24-pin SSOP Mechanical Outline: *Order as part no. MX919ADS*

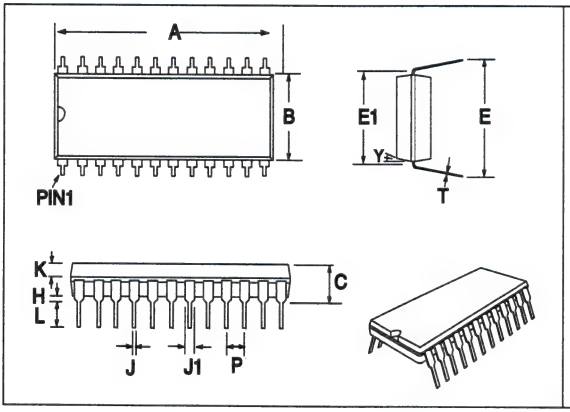


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 28: 24-pin PLCC Mechanical Outline : *Order as part no. MX919ALH*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 29: 24-pin PDIP Mechanical Outline: *Order as part no. MX919AP*

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

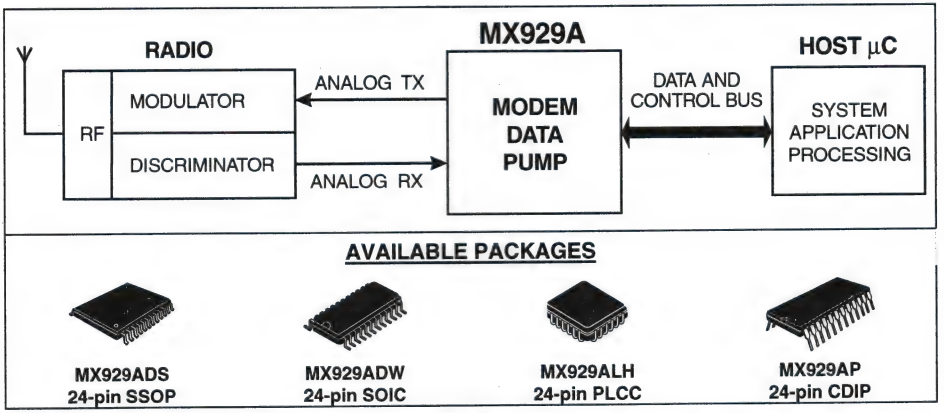
MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX929A 4-Level FSK Modem Data Pump

PRELIMINARY INFORMATION

- **4-Level FSK Modulation**
- **Half Duplex, 4800 to 19.2k bits/sec**
- **Full Data Packet Framing**
- **RD-LAP™ Compatible**
- **Flexible Operating Modes**
- **Host µC Interface**
- **Low Power 3.3V/5.0V Operation**
- **24-Pin Small Form Package Option**



The MX929A is a low voltage CMOS device containing all of the baseband signal processing and Medium Access Control (MAC) protocol functions required for a high performance 4-level FSK Wireless Packet Data Modem. It interfaces with the modem host µC and the radio modulation/demodulation circuits to deliver reliable two-way transfer of application data over a wireless link.

The MX929A assembles application data received from the host µC, adds forward error correction (FEC) and error detection (CRC) information and interleaves the result for burst-error protection. After automatically adding symbol and frame sync codewords, the data packet is converted into filtered 4-level analog signals for modulating into the radio transmitter.

In receive mode, the MX929A performs the reverse function using the analog signals from the receiver discriminator. After error correction and removal of the packet overhead, the recovered application data is supplied to the µC. CRC detected residual uncorrected data errors will be flagged. A readout of the SNR value during receipt of a packet is also provided.

The MX929A uses data block sizes and FEC/CRC algorithms compatible with the RD-LAP™ over-air standard. The format used is suitable for other private applications where the high-speed transfer of data over narrow-band wireless links is required. The device is programmable to operate at standard bit-rates from a wide choice of Xtal/Clock frequencies.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc.# 20480149.003

CONTENTS

Section ..... Page

1. Block Diagram 1-151

2. Signal List 1-152

3. External Components 1-153

4. General Description 1-154
4.1 Description of Blocks 1-154
4.2 Modem - µC Interaction 1-157
4.3 Binary to Symbol Translation 1-157
4.4 Frame Structure 1-158
4.5 The Programmer's View 1-159
4.6 CRC, FEC and Interleaving 1-171

5. Application Notes 1-172
5.1 Transmit Frame Example 1-172
5.2 Receive Frame Example 1-175
5.3 Clock Extraction and Level Measurement Systems 1-178
5.4 AC Coupling 1-179
5.5 Radio Performance 1-180

6. Performance Specification 1-181
6.1 Electrical Performance 1-181
6.2 Packaging 1-185

MX•COM, INC. Reserves the right to change specifications at any time and without notice.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

1. Block Diagram

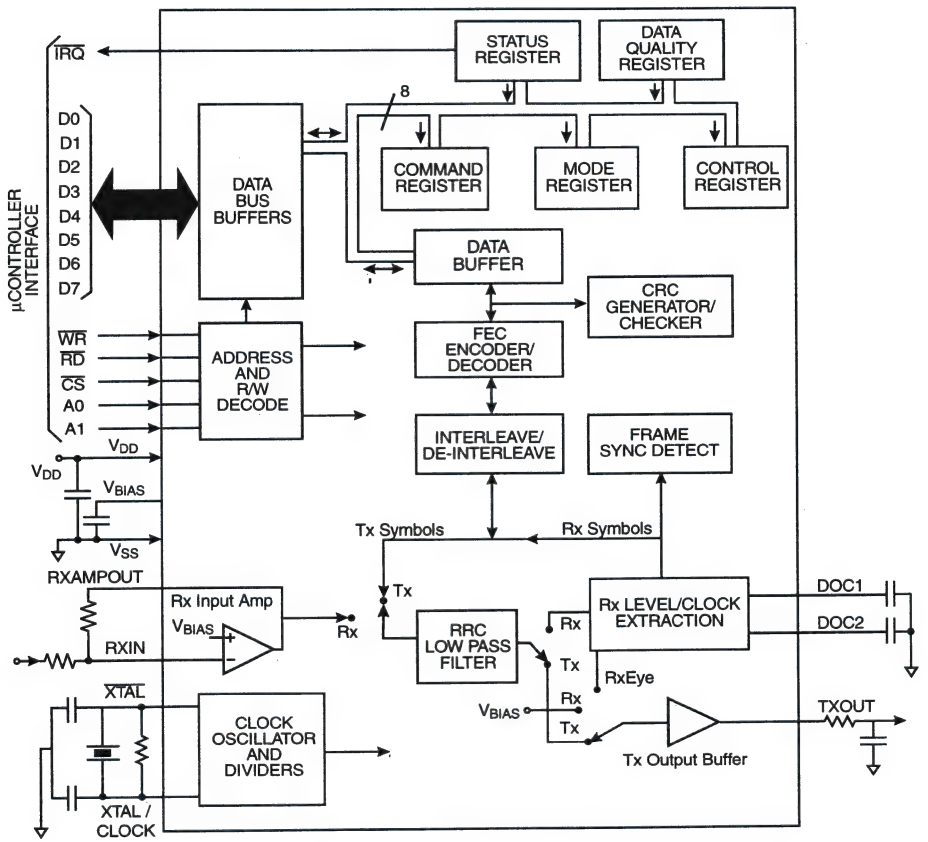


Figure 1: Block Diagram

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

2. Signal List

Pin No.	Signal	Type	Description
1	$\overline{IRQ}$	output	A 'wire-ORable' output for connection to the host µC's Interrupt Request input. When active, this output has a low impedance pull down to V_{SS}. It has a high impedance when inactive.
2	D7	BUS	Pins 2-9 (D7-D0) are 8-bit, bi-directional, 3-state µC interface data lines
3	D6	BUS	
4	D5	BUS	
5	D4	BUS	
6	D3	BUS	
7	D2	BUS	
8	D1	BUS	
9	D0	BUS	
10	$\overline{RD}$	input	Read. An active low logic level input used to control the reading of data from the modem into the host µC.
11	$\overline{WR}$	input	Write. An active low logic level input used to control the writing of data into the modem from the host µC.
12	V_{SS}	Power	Negative supply. (ground).
13	$\overline{CS}$	input	Chip Select. An active low logic level input to the modem. It is used to enable a data read or write operation.
14	A0	input	Logic level modem register select input
15	A1	input	Logic level modem register select input
16	$\overline{XTAL}$	output	The output of the on-chip oscillator.
17	XTAL/CLOCK	input	The input to the on-chip oscillator, for external Xtal circuit or clock.
18	DOC 2	output	Connection to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}
19	DOC 1	output	Connection to the Rx level measurement circuitry. Should be capacitive coupled to V_{SS}
20	TXOUT	output	Tx signal output from the modem.
21	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed to V_{SS} by a capacitor mounted close to the device pins.
22	RXIN	input	Input to the Rx input amplifier.
23	RXAMPOUT	output	Output of the Rx input amplifier
24	V_{DD}	power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

3. External Components

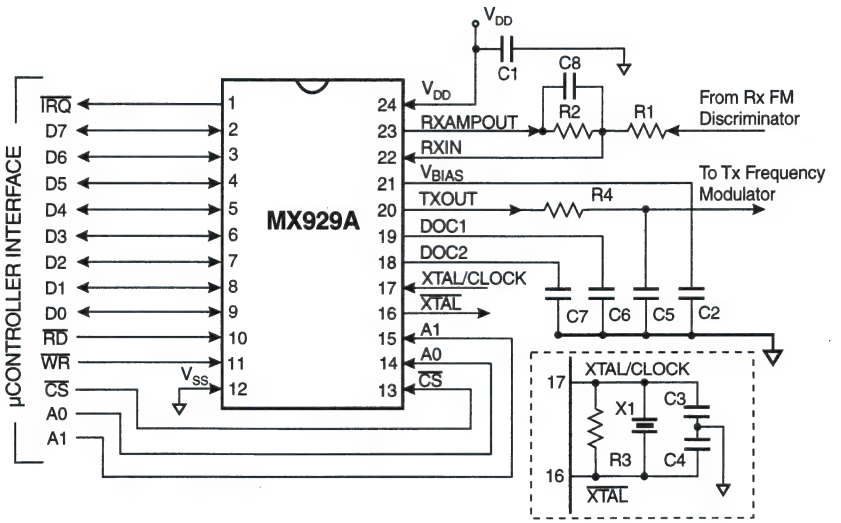


Figure 2: Recommended External Components

Component	Notes	Value	Tolerance
R1	1		
R2		100kΩ	± 5%
R3		1MΩ	± 20%
R4		100kΩ	± 5%
C1		0.1 µF	± 20%
C2		0.1 µF	± 20%
C3	2		± 20%
C4	2		± 20%
C5	3		± 5%
C6	4		± 20%
C7	4		± 20%
C8	3		± 5%
X1	2, 5		

Recommended External Components Notes

1. See section 4.1.10

2. The values used for C3 and C4 should be suitable for the frequency of the crystal X1. As a guide, values (including stray capacitance) of 33pF at 1MHz falling to 18pF at 10MHz will generally prove suitable. For optimum performance the crystal frequency should be ± 10ppm or better to allow use of the Narrow Bandwidth PLL setting

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

(see section 4.5.3). Tolerances as wide as ± 50ppm may be used, but at the cost of a slightly reduced BER performance.

3. Values C5 and C8 should be equal to 750000 ÷ symbol rate, e.g.

Symbol Rate	C5/C8
2400 symbols/second	330pF
4800 symbols/second	150pF
9600 symbols/second	82pF

4. Values C6 and C7 should be equal to 50000 ÷ symbol rate, e.g.

Symbol Rate	C6/C7
2400 symbols/second	0.022µF
4800 symbols/second	0.01µF
9600 symbols/second	4700pF

5. See section 4.5.3

4. General Description

4.1 Description of Blocks

4.1.1 Data Bus Buffers

Eight bi-directional 3-state logic level buffers between the modem's internal registers and the host µC's data bus lines.

4.1.2 Address and R/W Decode

This block controls the transfer of data bytes between the µC and the modem's internal registers, according to the state of the Write and Read Enable inputs ($\overline{WR}$ and $\overline{RD}$), the Chip Select input ($\overline{CS}$) and the Register Address inputs A0 and A1.

The Data Bus Buffers, Address and R/W Decode blocks provide a byte-wide parallel µC interface, which can be memory-mapped, as shown in Figure 3.

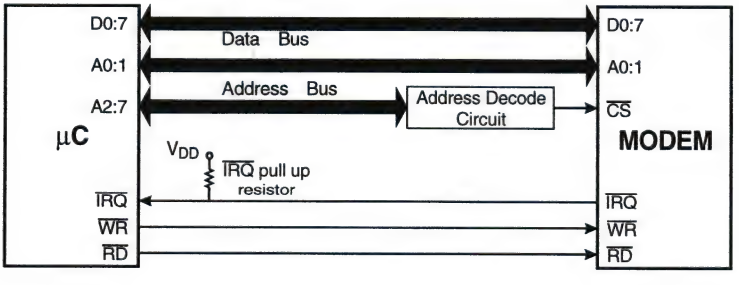


Figure 3: Typical Modem µC Connections

4.1.3 Status and Data Quality Registers

Two 8-bit registers which the µC can read to determine the status of the modem and the received data quality.

4.1.4 Command, Mode and Control Registers

The values written by the µC to these 8-bit registers control the operation of the modem.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.1.5 Data Buffer

A 12-byte buffer used to hold receive or transmit data to or from the µC.

4.1.6 CRC Generator/Checker

A circuit which generates (in transmit mode) or checks (in receive mode) the Cyclic Redundancy Checksum bits, which may be included in transmitted data blocks so the receive modem can detect transmission errors.

4.1.7 FEC Generator/Checker

In transmit mode, this circuit adds Forward Error Correction bits to the transmitted data, resulting in the conversion of binary data to 4-level symbols. In receive mode, this circuit translates received 4-level symbols to binary data, using the FEC information to correct a large proportion of transmission errors.

4.1.8 Interleave/De-interleave Buffer

This circuit interleaves data symbols within a block before transmission and de-interleaves the received data so the FEC system is best able to handle short noise bursts or fades.

4.1.9 Frame Sync Detect

This circuit, only active in receive mode, is used to look for a 24-symbol Frame Synchronization pattern that is transmitted to mark the start of every frame.

4.1.10 Rx Input Amp

This amplifier allows the received signal input to the modem to be set to the optimum level by suitable selection of the external components R1 and R2. The value of R1 should be calculated to give $(0.2 \times V_{DD})V_{P-P}$ at the RXAMPOUT pin for a received '...+3 +3 -3 -3 ...' sequence.

A capacitor may be placed in series with R1 if ac coupling of the received signal is desired (see section 5.4), otherwise the dc level of the received signal should be adjusted so the signal at the modem's RXAMPOUT is centered around V_{BIAS} ($V_{DD}/2$).

4.1.11 RRC Low Pass Filter

This filter, used in both transmit and receive modes, is a linear-phase lowpass filter with a 'Root Raised Cosine' frequency response defined by:

$$
\begin{aligned}
H(f) &= 1 && \text{for } 0 && \le f < (1-b)/(2T)\\
&= \text{square root of } \{0.5\,[1 - \sin(\pi\, T\, (f - 0.5/T)/b)]\} && \text{for } (1-b)/(2T) && \le f \le (1+b)/(2T)\\
&= 0 && \text{for } (1+b)/(2T) && < f
\end{aligned}
$$

where b = 0.2, T = 1/symbol rate

This frequency response is illustrated in Figure 5

In transmit mode, the 4-level symbols are passed through this filter to eliminate the high frequency components which would otherwise cause interference into adjacent radio channels.

In receive mode, the filter is used to reject HF noise and to equalize the received signal to a form suitable for extracting the 4-level symbols.

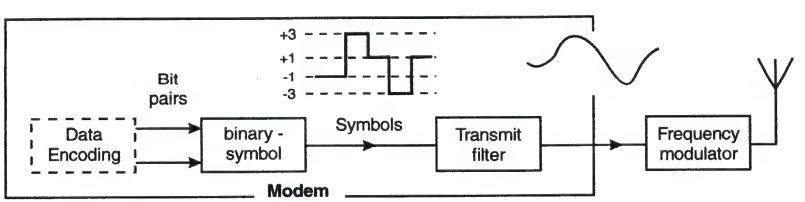


Figure 4: Translation of Binary Data to Filtered 4-Level Symbols in TX Mode

4.1.12 Tx Output Buffer

This is a unity gain amplifier used in the transmit mode to buffer the output of the Tx low pass filter. In receive mode, the input of this buffer is connected to V_{BIAS} unless the RXEYE bit of the Control Register is '1', when it is connected to the received signal. When changing from Rx to Tx mode the input to this buffer will be connected to V_{BIAS} for 8 symbol times while the RRC filter settles.

Note: The RC low pass filter formed by the external components R4 and C5 between the TXOUT pin and the input to the radio's frequency modulator forms an important part of the transmit signal filtering. These components may form part of any dc level-shifting and gain adjustment circuitry. The value used for C5 should take into account stray circuit capacitance, and its ground connection should be positioned to give maximum attenuation of high frequency noise into the modulator.

The signal at the TXOUT pin is centered around V_{BIAS} and is approx. (0.2 x V_{DD})V_{P-P} for a continuous '+3 +3 -3 -3 ...' pattern.

A capacitor may be placed in series with the input to the frequency modulator if ac coupling is desired, see section 5.4

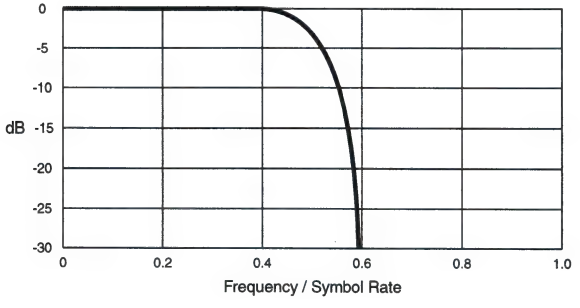


Figure 5: RRC Filter Frequency Response (including the external RC filter R4/C5)

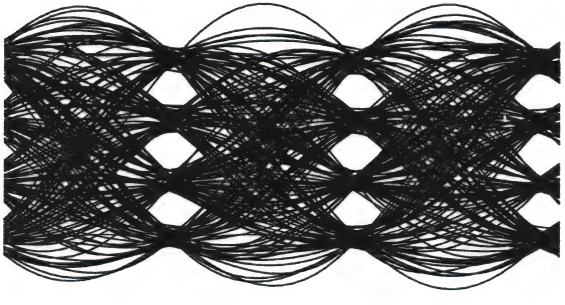


Figure 6: Transmitted Signal Eye Diagram

4.1.13 Rx Level/Clock Extraction

These circuits, which operate only in receive mode, derive a symbol rate clock from the received signal and measure the received signal amplitude and dc offset. This information is then used to extract the received 4-level symbols and also to provide an input to the received Data Quality measuring circuit. The external capacitors C6 and C7 form part of the received signal level measuring circuit.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.1.14 Clock Oscillator and Dividers

These circuits derive the transmit symbol rate (and the nominal receive symbol rate) by frequency division of a reference frequency which may be generated by the on-chip Xtal oscillator or applied from an external source.

Note: If the on-chip Xtal oscillator is to be used, then the external components X1, C3, C4 and R3 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin, the $\overline{\text{XTAL}}$ pin should be left unconnected, and X1, C3, C4 and R3 not fitted.

4.2 Modem - µC Interaction

In general, data is transmitted over-air in the form of messages, or 'Frames', consisting of a 'Frame Preamble' followed by one or more formatted data blocks. The Frame Preamble includes a Frame Synchronization pattern designed to allow the receiving modem to identify the start of a frame. The following data blocks are constructed from the 'raw' data using a combination of CRC (cyclic redundancy checksum) generation, Forward Error Correction coding and Interleaving. Details of the message formats handled by the modem are provided in section 4.3 and Figure 7 and Figure 8.

To reduce the processing load on the associated µC, the MX929A modem has been designed to perform much of the computationally intensive work involved in Frame formatting and de-formatting and - when in receive mode - in searching for and synchronizing onto the Frame Preamble. In normal operation the modem will only require servicing by the µC once per received or transmitted block.

To transmit a block, the controlling µC only needs to load the - unformatted - 'raw' binary data into the modem's Data Block Buffer, then instruct the modem to format and transmit that data. The modem will then calculate and add the CRC bits as required, encode the result as 4-level symbols (with Forward Error Correction coding), and interleave the symbols before transmission.

In receive mode, the modem can be instructed to assemble a block's worth of received symbols, de-interleave the symbols, translate them to binary - using the FEC coding to correct as many errors as possible - and check the resulting CRC before placing the received binary data into the Data Block Buffer for the µC to read.

The modem can also handle the transmission and reception of unformatted data for example: to allow for the transmission of Symbol and Frame Synchronization sequences or special test patterns.

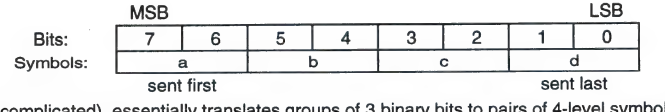
4.3 Binary to Symbol Translation

Although the over-air signal, and the signals at the modem TXOUT and RXIN pins, consists of 4-level symbols, the raw data passing between the modem and the µC is in binary form. Translation between binary data and the 4-level symbols is done in one of two ways, depending on the task being performed.

1. Direct (simplest form) - converts between 2 binary bits and a single symbol, such as the 'S' Channel Status symbol.

symbol	MSB	LSB
+3	1	1
+1	1	0
-1	0	0
-3	0	1

This is expanded so that an 8-bit byte translates to four symbols for the T4S, T24S and R4S tasks described in section 4.5.2



2. FEC (more complicated), essentially translates groups of 3 binary bits to pairs of 4-level symbols using a Forward Error Correcting coding scheme for the block oriented tasks THB, TIB, TLB, TSID, RHB, RILB and RSID described in section 4.5.2

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.4 Frame Structure

The MX929A Frame Structure (as used in a RD-LAP™ system) is illustrated in Figure 7, and consists of a Frame Preamble (comprising a 24-symbol Frame Synchronization pattern and Station ID block) followed by a 'Header Block', one or more 'Intermediate Blocks and a 'Last Block'. Channel Status (S) symbols are included at regular intervals. The first Frame of any transmission is preceded by a Symbol Synchronization pattern.

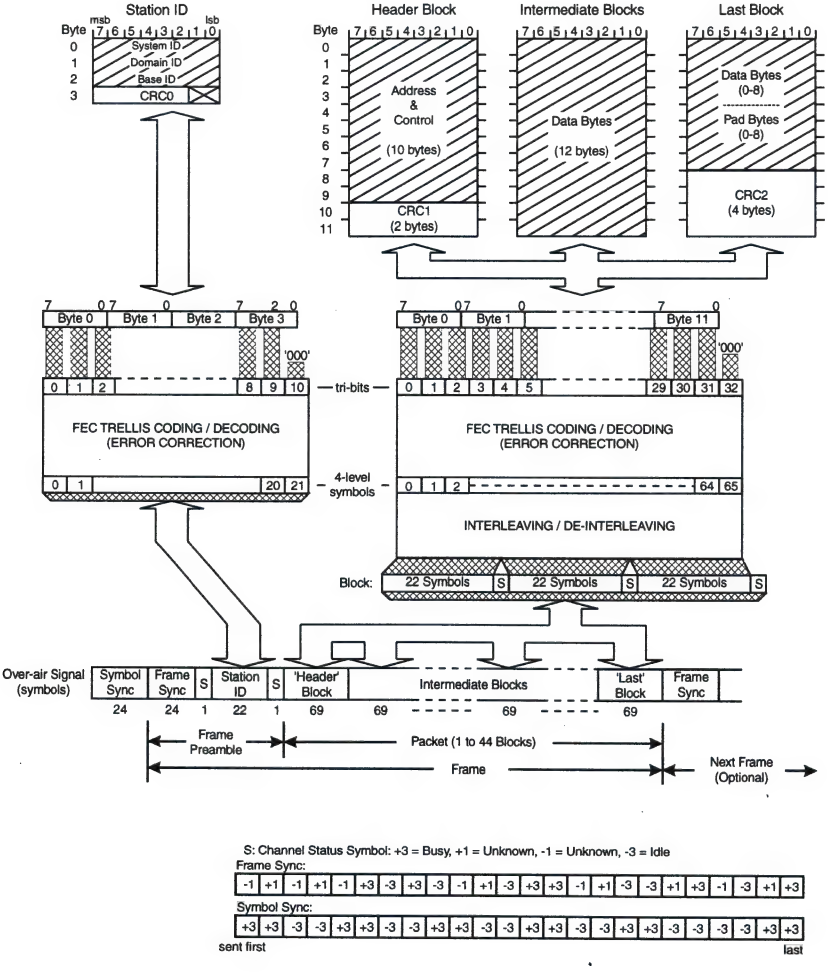


Figure 7: Over-Air-Signal Format

The 'Header' block is self-contained, includes its own checksum (CRC1), and would normally carry information such as the address of the calling and called parties, the number of following blocks in the frame (if any), and miscellaneous control information.

The 'Intermediate' block(s) contain only data. The checksum at the end of the 'Last' block (CRC2) also checks the data in any preceding 'Intermediate' blocks.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Proprietary systems which do not use the RD-LAP™ format may use the block structures provided by the MX929A to build alternative frame formats more suited to the particular application. Some examples are illustrated in Figure 8.

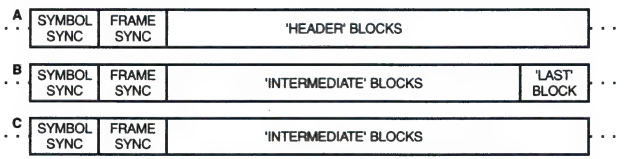


Figure 8: Some Alternative Frame Structures

The MX929A performs all of the block formatting and de-formatting, the binary data transferred between the modem and the µC is indicated by the diagonal lines in Figure 7.

4.5 The Programmer's View

To the programmer, the modem appears as 4 write only, 8-bit registers, and shadowed by 3 read only registers. The individual registers are selected by the A0 and A1 chip inputs:

A1	A0	Write to Modem	Read from Modem
0	0	Data Buffer	Data Buffer
0	1	Command Register	Status Register
1	0	Control Register	Data Quality Register
1	1	Mode Register	not used

Note: There is a minimum time allowance between accesses of the modem's registers, see section 6.1.

4.5.1 Data Block Buffer

This is a 12-byte read/write buffer which is used to transfer data (as opposed to command, status, mode, data quality or control information) between the modem and the host µC.

To the µC, the Data Block buffer appears as a single 8-bit register. The modem ensures that sequential µC reads or writes to the buffer are routed to the correct locations within the buffer.

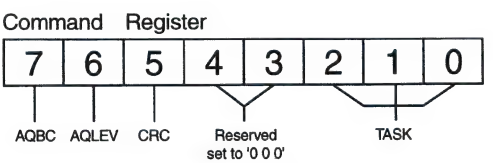
The µC should only access this buffer when the Status Register BFREE (Buffer Free) bit is '1'.

The buffer should only be written to while in Tx mode and read from while in Rx mode.

Note: In receive mode, the modem will function correctly even if the received data is not read from the Data Buffer by the µC.

4.5.2 Command Register

Writing to this register tells the modem to perform a specific action or actions, depending on the setting of the TASK, AQLEV and AQSC bits.



When there is no action to perform, the modem will be in an 'idle' state. If the modem is in transmit mode the input to the Tx RRC filter will be connected to V_{BIAS}. In receive mode the modem will continue to measure the received data quality and extract symbols from the received signal, supplying them to the de-interleave buffer, otherwise the received data is ignored.

4.5.2.1 Command Register B7: AQSC - Acquire Symbol Clock

This bit has no effect in transmit mode.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

In receive mode, when a byte with the AQSC bit set to '1' is written to the Command Register, and TASK is not set to RESET, it initiates an automatic sequence designed to achieve symbol timing synchronization with the received signal as quickly as possible. This involves setting the Phase Locked Loop of the received bit timing extraction circuits to its widest bandwidth, then gradually reducing the bandwidth as timing synchronization is achieved, until it reaches the 'normal' value set by the PLLBW bits of the Control Register.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however; the acquisition sequence will be re-started every time a byte written to the Command Register has the AQSC bit set to '1'.

The AQSC bit will normally be set at the same time as a SFS (Search for Frame Sync) or SFP (Search for Frame Preamble) task is written to the MX929A, however it may also be used independently to re-establish clock Synchronization quickly after a long fade. Alternatively, a SFS or SFP task may be written to the Command Register with the AQSC bit at '0' if it is known that clock Synchronization does not need to be re-established. More details of the clock acquisition sequence are given in section 5.3

4.5.2.2 Command Register B6: AQLEV - Acquire Receive Signal Levels

This bit has no effect in transmit mode.

In receive mode, when a byte with the AQLEV bit set to '1' is written to the Command Register and TASK is not set to RESET, it initiates an automatic sequence designed to measure the amplitude and dc offset of the received signal immediately. This sequence involves setting the measurement circuits to respond quickly at first, then gradually increasing their response time, therefore improving the measurement accuracy, until the 'normal' value set by the LEVRES bits of the Control Register is reached.

Setting this bit to '0' (or changing it from '1' to '0') has no effect, however; the acquisition sequence will be re-started every time a byte written to the Command Register has the AQLEV bit set to '1'.

The AQLEV bit will normally be set at the same time as a SFS (Search for Frame Sync) or SFP (Search for Frame Preamble) task is initiated, however it may also be used independently to re-establish signal levels quickly after a long fade. Alternatively, a SFS or SFP task may be written to the Command Register with the AQLEV bit at '0' if it is known that there is no need to re-establish the received signal levels. More details of the level measurement acquisition sequence are given in section 5.3.

4.5.2.3 Command Register B5: CRC

This bit allows the user to select between two different forms of the CRC0, CRC1, and CRC2 check sums. When this bit is set to '1' the CRC generators are initialized to 'all zeros', as required by RD-LAP systems. When this bit is set to '0' the CRC generators are initialized to 'all ones' as required by CCITT X25 based systems. It should always be set to '1' for RD-LAP compatibility, other systems may set this bit as required.

4.5.2.4 Command Register B4, B3

These two bits should always be set to '0'

4.5.2.5 Command Register B2, B1, B0: TASK

Operations such as transmitting or receiving a data block are treated by the modem as 'tasks' and are initiated when the µC writes a byte to the Command Register with the TASK bits set to anything other than the 'NULL' code.

The µC should not write a task (other than NULL or RESET) to the Command Register or write to or read from the Data Buffer when the BFREE (Buffer Free) bit of the Status Register is '0'.

Different tasks apply in receive and transmit modes.

When the modem is in transmit mode, all tasks other than NULL or RESET instruct the modem to transmit data from the Data Buffer, formatting it as required. The µC should therefore wait until the BFREE (Buffer Free) bit of the Status Register is '1', before writing the data to the Data Block Buffer, then it should write the desired task to the Command Register. If more than 1 byte needs to be written to the Data Block Buffer, byte number 0 of the block should be written first.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE (Buffer Free) bit of the Status Register to '0'.

Take the data from the Data Block Buffer as quickly as it can - transferring it to the Interleave Buffer for eventual transmission. This operation will start immediately if the modem is 'idle' (i.e. not transmitting data from a previous task), otherwise it will be delayed until there is sufficient room in the Interleave Buffer.

Once all of the data has been transferred from the Data Block Buffer the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the chip $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may write new data and the next task to the modem.

This lets the µC write a task and the associated data to the modem while the modem is still transmitting the data from the previous task.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

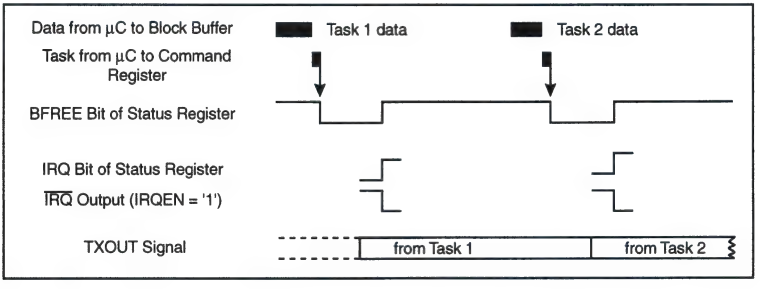

Data from µC to Block Buffer
Task 1 data
Task 2 data
Task from µC to Command Register
BFREE Bit of Status Register
IRQ Bit of Status Register
IRQ Output (IRQEN = '1')
TXOUT Signal
from Task 1
from Task 2

Figure 9: Transmit Task Overlapping

When the modem is in receive mode, the µC should wait until the BFREE bit of the Status Register is '1', then write the desired task to the Command Register.

Once the byte containing the desired task has been written to the Command Register, the modem will:

Set the BFREE bit of the Status Register to '0'.

Wait until enough received symbols are in the De-interleave Buffer.

Decode them as needed, and transfer the resulting binary data to the Data Block Buffer

Then the modem will set the BFREE and IRQ bits of the Status Register to '1', (causing the $\overline{IRQ}$ output to go low if the IRQEN bit of the Mode Register has been set to '1') to tell the µC that it may read from the Data Block Buffer and write the next task to the modem. If more than 1 byte is contained in the buffer, byte number 0 of the data will be read out first.

In this way the µC can read data and write a new task to the modem while the received symbols needed for this new task are being received and stored in the De-interleave Buffer.

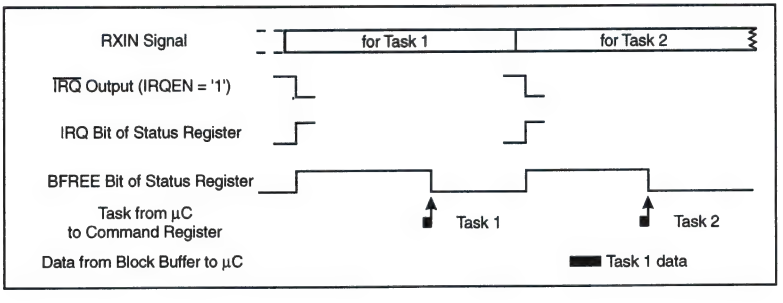


Figure 10: Receive Task Overlapping

Note: Detailed timings for the various tasks are provided in Figure 11 and Figure 12.

MX929A Modem Tasks:

B2	B1	B0	Receive Mode		Transmit Mode	
0	0	0	NULL		NULL	
0	0	1	SFP	Search for Frame Preamble	T24S	Transmit 24 symbols
0	1	0	RHB	Read Header Block	THB	Transmit Header Block
0	1	1	RILB	Read Intermediate or Last Block	TIB	Transmit Intermediate Block
1	0	0	SFS	Search for Frame Sync	TLB	Transmit Last Block
1	0	1	R4S	Read 4 symbols	T4S	Transmit 4 symbols
1	1	0	RSID	Read Station ID	TSID	Transmit Station ID
1	1	1	RESET	Cancel any current action	RESET	Cancel any current action

4.5.2.6 NULL: No effect

This task is provided so that a AQSC or AQLEV command can be initiated without loading a new task.

4.5.2.7 SFP: Search for Frame Preamble

This task causes the modem to search the received signal for a valid Frame Preamble, consisting of a 24-symbol Frame Sync sequence followed by Station ID data which has a correct CRC0 checksum.

The task continues until a valid Frame Preamble has been found.

The search consists of four stages:

First of all the modem will attempt to match the incoming symbols against the Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Control Register.

Once a match has been found, the modem will read in the following 'S' symbol, place it in the SVAL bits of the Status Register then set the SRDY bit to '1'. (The IRQ bit of the Status Register will also be set to '1' at this time if the SSIEN bit of the Mode Register is '1').

The modem will then read the next 22 symbols as station ID data. They will be decoded and the CRC0 checked. If this is incorrect, the modem will resume the search, looking for a fresh Frame Sync pattern.

If the received CRC0 is correct, the following 'S' symbol will be read into the SVAL bits of the Status Register and the SRDY, BFREE and IRQ bits set to '1', the CRCERR bit cleared to '0', and the three decoded Station ID bytes placed into the Data Block Buffer.

On detecting that the BFREE bit of the Status Register has gone to '1', the µC should read the 3 Station ID bytes from the Data Block Buffer then write the next task to the modem's Command Register.

4.5.2.8 RHB: Read Header Block

This task causes the modem to read the next 69 symbols as a 'Header' Block. It will strip out the 'S' symbols then de-interleave and decode the remaining 66 symbols, placing the resulting 10 data bytes and the 2 received CRC1 bytes into the Data Block Buffer, and setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete to indicate that the µC may read the data from the Data Block Buffer and write the next task to the modem's Command Register.

The CRCERR bit of the Status Register will be set to '1' or '0' depending on the validity of the received CRC1 checksum bytes.

As each of the 3 'S' symbols of a block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1', then the Status Register IRQ bit will also be set to '1'.) Note that when the third 'S' symbol is received, the SRDY bit will be set to '1' coincidentally with the BFREE bit also being set to '1'.

4.5.2.9 RILB: Read 'Intermediate' or 'Last' Block

This task causes the modem to read the next 69 symbols as an 'Intermediate' or 'Last' block (the µC can tell from the 'Header' block how many blocks are in the frame, and when to expect the 'Last' block).

In each case, it will strip out the 3 'S' symbols, de-interleave and decode the remaining 66 symbols and place the resulting 12 bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete.

If an 'Intermediate' block is received the µC should read out all 12 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register, for a 'Last' block the µC need only read the first 8 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received CRC2 checksum

As each of the 3 'S' symbols of the block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1', then the Status Register IRQ bit will also be set to '1'.) Note that when the third 'S' symbol is received, the SRDY bit will be set to '1' coincidentally with the BFREE bit also being set to '1'.

© 1997 MX•COM, INC. Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.5.2.10 SFS: Search for Frame Sync

This task - which is intended for special test and channel monitoring purposes - performs the first two parts only of a SFP task. It causes the modem to search the received signal for a 24-symbol sequence which matches the required Frame Synchronization pattern to within the tolerance defined by the FSTOL bits of the Mode Register.

When a match is found the modem will read in the following 'S' symbol, then set the BFREE, IRQ and SRDY bits of the Status Register to '1' and update the SVAL bits. The µC may then write the next task to the Command Register.

4.5.2.11 R4S: Read 4 Symbols

This task causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set to '1' to indicate that the µC may read the data byte from the Data Block Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by SFS task

4.5.2.12 RSID: Read Station ID

This task causes the modem to read in and decode the following 23 symbols as Station ID data followed by an 'S' symbol. It is similar to the last two parts of a SFP task except that it will not re-start if the received CRC0 is incorrect. It would normally follow a SFS task.

The 3 decoded bytes will be placed into the Data Block Buffer, and the CRCERR bit of the Status Register set to '1' if the received CRC0 was incorrect, otherwise it will be cleared to '0'. The SVAL bits of the Status Register will be updated and the BFREE, SRDY and IRQ bits set to '1' to indicate that the µC may read the 3 received bytes from the Data Block Buffer and write the next task to the modem's Command Register.

4.5.2.13 T24S: Transmit 24 Symbols

This task, which is intended to facilitate the transmission of Symbol and Frame Sync patterns as well as special test sequences, takes 6 bytes of data from the Data Block Buffer and transmits them as 24 4-level symbols without any CRC, FEC, interleaving or adding any 'S' symbols.

Byte 0 of the Data Block Buffer is sent first, byte 5 last.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1', indicating to the µC that it may write the data and command byte for the next task to the modem.

The tables below show what data has to be written to the Data Block Buffer to transmit the MX929A Symbol and Frame Sync sequences:

'Symbol Sync'				Values written to Data Block Buffer		
Symbols					Binary	Hex
+3	+3	-3	-3	Byte 0:	11110101	F5
+3	+3	-3	-3	Byte 1:	11110101	F5
+3	+3	-3	-3	Byte 2:	11110101	F5
+3	+3	-3	-3	Byte 3:	11110101	F5
+3	+3	-3	-3	Byte 4:	11110101	F5
-3	-3	+3	+3	Byte 5 :	01011111	5F

'Frame Sync'				Values written to Data Block Buffer		
Symbols					Binary	Hex
-1	+1	-1	+1	Byte 0:	00100010	22
-1	+3	-3	+3	Byte 1:	00110111	37
-3	-1	+1	-3	Byte 2:	01001001	49
+3	+3	-1	+1	Byte 3:	11110010	F2
-3	-3	+1	+3	Byte 4:	01011011	5B
-1	-3	+1	+3	Byte 5:	00011011	1B

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.5.2.14 THB: Transmit Header Block

This task takes 10 bytes of data (Address and Control) from the Data Block Buffer, calculates and appends the 2-byte CRC1 checksum, translates the result to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Header' Block , inserting 'S' symbols at 22-symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.15 TIB: Transmit Intermediate Block

This task takes 12 bytes of data from the Data Block Buffer, updates the 4-byte CRC2 checksum for inclusion in the 'Last' block, translates the 12 data bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Intermediate' Block , inserting 'S' symbols at 22-symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.16 TLB: Transmit Last Block

This task takes 8 bytes of data from the Data Block Buffer, updates and appends the 4-byte CRC2 checksum, translates the resulting 12 bytes to 4-level symbols (with FEC), interleaves the symbols and transmits the result as a formatted 'Last' Block , inserting 'S' symbols at 22-symbol intervals.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.17 T4S: Transmit 4 Symbols

This task is similar to T24S but takes only one byte from the Data Block Buffer, transmitting it as four 4-level symbols.

4.5.2.18 TSID: Transmit Station ID

This task takes 3 ID bytes from the Data Block Buffer, calculates and appends the 6-bit CRC0 checksum, translates the result to 4-level symbols (with FEC) and transmits the resulting 22 symbols preceded and followed by 'S' symbols.

Once the modem has read the data bytes from the Data Block Buffer, the BFREE and IRQ bits of the Status Register will be set to '1'.

4.5.2.19 RESET: Stop any current action

This 'task' takes effect immediately, and terminates any current action (task, AQSC or AQLEV) the modem may be performing and sets the BFREE bit of the Status Register to '1', without setting the IRQ bit. It should be used when V_{DD} is applied, to set the modem into a known state.

Note: Due to delays in the RRC filter, it will take several symbol times for any change to appear at the TXOUT pin.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Task Timings

		Task	Time (symbol times)
t_1	Modem in idle state. Time from writing first task to application of first transmit bit to Tx RRC filter	Any	1 to 2
t_2	Time from application of first symbol of the task to the Tx RRC filter until BFREE goes to a logic '1' (high).	T24S TSID THB/TIB/TLB T4S	5 6 16 0
t_3	Time to transmit all symbols of the task	T24S/TSID THB/TIB/TLB T4S	24 69 4
t_4	Max time allowed from BFREE going to a logic '1' for next task (and data) to be written to modem	T24S TSID THB/TIB/TLB T4S	18 17 52 3
t_5	Time to receive all symbols of task	SFS SFP RSID RHB/RILB R4S	25 (min) 48 (min) 23 69 4
t_6	Maximum time between first symbol of task entering the de-interleave circuit and the task being written to modem	SFS SFP RSID RHB/RILB R4S	21 21 15 51 3
t_7	Maximum time from the last bit of the task entering the de-interleave circuit to BFREE going to a logic '1'	Any	1

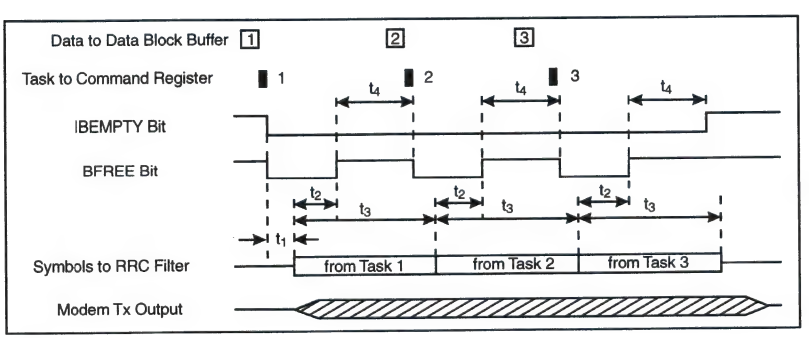


Figure 11: Transmit Task Timing Diagram

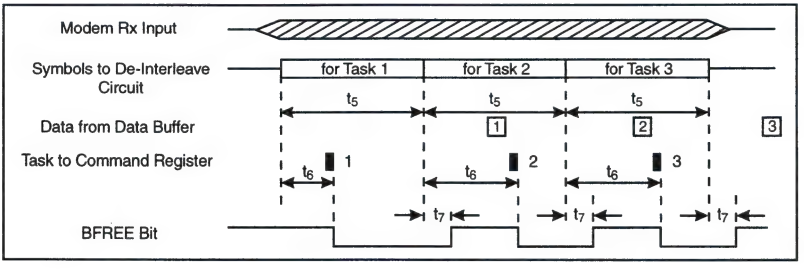


Figure 12: Receive Task Timing Diagram

RRC Filter Delay

The previous task timing figures are based on the signal at the input to the RRC filter (in transmit mode) or the input to the de-interleave buffer (in receive mode). There is an additional delay of approximately 8 symbol times through to the RRC filter in both transmit and receive modes, as shown in Figure 13:

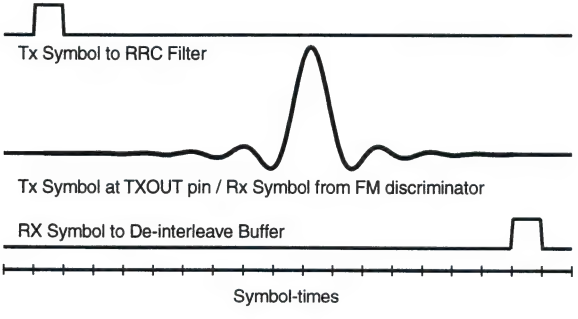
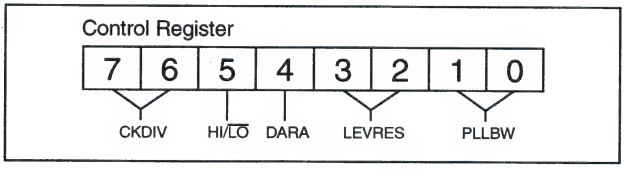

Tx Symbol to RRC Filter
Tx Symbol at TXOUT pin / Rx Symbol from FM discriminator
RX Symbol to De-interleave Buffer
Symbol-times

Figure 13: RRC Low Pass Filter Delay

4.5.3 Control Register

This 8-bit write-only register controls the modem's symbol rate, the response times of the receive clock extraction and signal level measurement circuits and the Frame Sync pattern recognition tolerance.



4.5.3.1 Control Register B7, B6: CKDIV - Clock Division Ratio

These bits control a frequency divider driven from the clock signal present at the $\overline{\text{XTAL}}$ pin, thereby determining the nominal symbol rate. The table below shows how symbol rates of 2400/4800/9600 symbols/sec may be obtained from common Xtal frequencies:

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

			Xtal Frequency (MHz)		
			2.4576	4.9152	9.8304
B7	B6	Division Ratio: Xtal Frequency/Symbol Rate	Symbol Rate (symbols/sec)		
0	0	512	4800	9600	
0	1	1024	2400	4800	9600
1	0	2048		2400	4800
1	1	4096			2400

Note: Device operation is not guaranteed below 2400 or above 9600 symbols/sec.

4.5.3.2 Control Register B5, B4: FSTOL - Frame Sync Tolerance

These two bits have no effect in transmit mode. In receive mode, they define the maximum number of mismatches which will be allowed during a search for the Frame Sync pattern:

B5	B4	Mismatches allowed
0	0	0
0	1	2
1	0	4
1	1	6

Note: A single 'mismatch' is defined as the difference between two adjacent symbol levels, thus if the symbol '+1' were expected, then received symbol values of '+3' and '-1' would count as 1 mismatch, a received symbol value of '-3' would count as 2 mismatches.

4.5.3.3 Control Register B3, B2: LEVRES - Level Measurement Modes

These two bits have no effect in transmit mode. In receive mode they set the 'normal' operating mode of the Rx signal amplitude and dc offset measuring circuits. This setting will be temporarily overridden by the automatic sequencing of an AQLEV command.

B3	B2	Mode
0	0	Hold
0	1	Slow Peak Detect
1	0	Lossy Peak Detect
1	1	Clamp

For most applications these two bits should be set to 'Slow Peak Detect' mode, in which the peak positive and peak negative excursions of the received signal (after filtering) are measured to establish the amplitude and dc offset of the signal. The decay time-constant of the peak rectifier circuits used in this mode is approximately 750 symbol times.

The 'Hold' setting freezes the stored values of the current amplitude and offset measurements and may therefore be used to improve performance during short fades or while the radio is switched from receive mode for the transmission of a short acknowledgment. It should be noted, however, that the measured amplitude and offset values are stored on the external capacitors C7 and C8 and will decay gradually when the 'Hold' setting is chosen, the discharge time-constant being approximately 750 symbol times.

The 'Lossy Peak Detect' setting is similar to 'Slow Peak Detect' except that the decay time-constant of the peak detectors are reduced to approximately 25 symbol times to give a faster response to signal changes at the expense of a reduction in BER performance. This mode is used by the automatic Level Measurement acquisition sequence but may also be useful in non-standard systems.

The 'Clamp' setting is primarily intended for use by the automatic Level Measurement acquisition sequence as described in section 5.3, but may also be useful in non-standard systems. In this mode the DOC1 and DOC2 pins are connected directly to the output of the circuit that normally drives the peak detectors.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.5.3.4 Control Register B1, B0: PLLBW - Phase-Locked Loop Modes

These two bits have no effect in transmit mode In receive mode, they set the 'normal' bandwidth of the Rx clock extraction Phase Locked Loop circuit. This setting will be temporarily overridden by the automatic sequencing of an AQSC command.

B1	B0	PLL Mode	Working Bandwidth (±ppm)
0	0	Hold	-
0	1	Narrow Bandwidth	20
1	0	Medium Bandwidth	100
1	1	Wide Bandwidth	650

The minimum bandwidth consistent with the transmit and receive modem symbol rate tolerances should be chosen, i.e. if the Xtals used with both modems have accuracy's of within ± 50ppm, then the PLLBW bits should be set to '10' ('Medium Bandwidth'). However, to allow the PLL to settle quickly it is recommended that when very close tolerance Xtals are used, then the PLLBW bits should be set to 'Medium' whenever an AQSC is triggered, and only changed to 'Narrow' about 200 symbol times later.

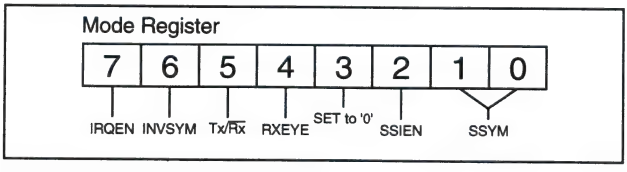
The 'Wide Bandwidth' setting is intended for message acquisition in systems where the µC cannot detect the start of a received message, as it allows the modem to respond rapidly to fresh messages and recover rapidly after a fade without µC intervention - although at the cost of reduced Bit Error Rate Vs Signal to Noise performance.

The 'Hold' setting disables the PLL feedback loop, and may be used during signal fades.

Note: 'Working Bandwidths' are the maximum difference between the actual received symbol rate and the nominal rate determined by the tolerance of the modem's Xtal frequency, to give minimal degradation of a reasonably random received signal.

4.5.4 Mode Register

The contents of this 8-bit write only register control the basic operating modes of the modem:



4.5.4.1 Mode Register B7: IRQEN - $\overline{IRQ}$ Output Enable

When this bit is set to '1', the $\overline{IRQ}$ chip output pin is pulled low (to V_{SS}) when the IRQ bit of the Status Register is a '1'.

4.5.4.2 Mode Register B6: INVSYM - Invert Symbols

This bit controls the polarity of the transmitted and received symbol voltages.

B6	Symbol	Signal at TXOUT	Signal at RXAMPOUT
0	'+3'	Above V_{BIAS}	Below V_{BIAS}
	'-3'	Below V_{BIAS}	Above V_{BIAS}
1	'+3'	Below V_{BIAS}	Above V_{BIAS}
	'-3'	Above V_{BIAS}	Below V_{BIAS}

4.5.4.3 Mode Register B5: TX/$\overline{RX}$ - Tx/Rx Mode

Setting this bit to '1' puts the modem into Transmit mode, clearing it to '0' puts the modem into Receive mode.
Note: Changing between receive and transmit modes will cancel any current task.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.5.4.4 Mode Register B4: RXEYE - Show Rx Eye

This bit should normally be set to '0'.

Setting it to '1' when the modem is in receive mode configures the modem into a special test mode, in which the input of the Tx output buffer is connected to the Rx Symbol/Clock extraction circuit at a point which carries the equalized receive signal. This may be monitored with an oscilloscope (at the TXOUT pin itself), to assess the quality of the complete radio channel including the Tx and Rx modem filters, the Tx modulator and the Rx IF filters and FM demodulator.

The resulting eye diagram (for reasonably random data) should ideally be as shown in Figure 14, with 4 'crisp' and equally spaced crossing points.

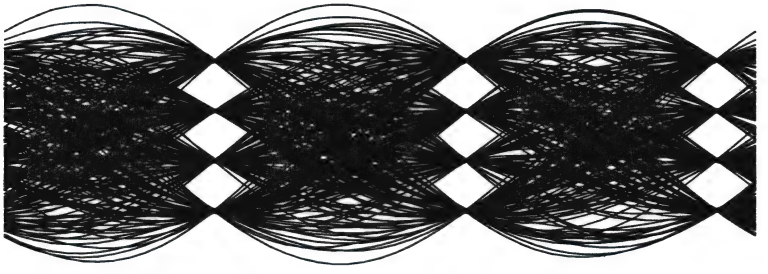


Figure 14: Ideal 'RXEYE' Signal

4.5.4.5 Mode Register B3: PSAVE - Powersave

When this bit is a '1', the modem will be in 'powersave mode' in which the internal filters, the RX Symbol and Clock extraction circuits, and the Tx output buffer will be disabled. The TXOUT pin will be connected to V_{BIAS} through a high value resistance. The XTAL/CLOCK oscillator, Rx input amplifier, and the µC interface logic will continue to operate.

4.5.4.6 Mode Register B2: SSIEN - 'S' Symbol IRQ Enable

In receive mode, setting this bit to '1' causes the IRQ bit of the status register to be set to '1' whenever a new 'S' symbol has been received. (The SRDY bit of the Status Register will also be set to '1' at the same time, and the SVAL bits updated to reflect the received 'S' symbol.)

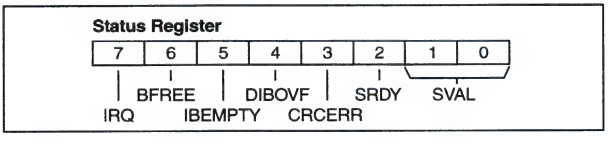
In transmit mode, setting this bit to '1' causes the IRQ bit of the Status Register to be set to '1' whenever a 'S' symbol has been transmitted. (The SRDY bit of the Status Register will also be set to '1' at the same time.)

4.5.4.7 Mode Register B1, 0: SSYM - 'S' Symbol To Be Transmitted

In transmit mode these two bits define the next 'S' symbol to be transmitted. These bits have no effect in receive mode.

4.5.5 Status Register

This register may be read by the µC to determine the current state of the modem.



4.5.5.1 Status Register B7: IRQ - Interrupt Request

This bit is set to '1' by:

Status Register BFREE bit going from '0' to '1', unless this is caused by a RESET task or by a change to the Mode Register TX/$\overline{RX}$ bit.

Status Register IBEMPTY bit going from '0' to '1', unless this is caused by a RESET task or by changing the Mode Register TX/$\overline{RX}$ bit.

Status Register DIBOVF bit going from '0' to '1'.

Status Register SRDY bit being set to '1' (due to a 'S' symbol being received or transmitted) if the Mode Register SSIEN bit is '1'.

The IRQ bit is cleared to '0' immediately after a read of the Status Register.

If the IRQEN bit of the Mode Register is '1', then the chip $\overline{IRQ}$ output will be pulled low (to V_{SS}) whenever the IRQ bit is set to '1', and will go high impedance when the Status Register is read.

4.5.5.2 Status Register B6: BFREE - Data Block Buffer Free

This bit reflects the availability of the Data Block Buffer and is cleared to '0' whenever a task other than NULL or RESET is written to the Command Register.

In transmit mode, the BFREE bit will be set to '1' (also setting the Status Register IRQ bit to '1') by the modem when the modem is ready for the µC to write new data to the Data Block Buffer and the next task to the Command Register.

In receive mode, the BFREE bit is set to '1' (also setting the Status Register IRQ bit to '1') by the modem when it has completed a task and any data associated with that task has been placed into the Data Block Buffer. The µC may then read that data and write the next task to the Command Register.

The BFREE bit is also set to '1' - but without setting the IRQ bit - by a RESET task or when the Mode Register TX/$\overline{RX}$ bit is changed.

4.5.5.3 Status Register B5: IBEMPTY - Interleave Buffer Empty

In transmit mode, this bit will be set to '1' - also setting the IRQ bit - when less than two symbols remain in the Interleave Buffer. Any transmit task written to the modem after this bit goes to '1' will be too late to avoid a gap in the transmit output signal.

The bit is also set to '1' by a RESET task or by a change of the Mode Register TX/$\overline{RX}$ bit, but in these cases the IRQ bit will not be set.

The bit is cleared to '0' within one symbol time after a task other than NULL or RESET is written to the Command Register.

Note: When the modem is in transmit mode and the Interleave Buffer is empty, a mid level (half-way between '+1' and '-1') signal will be sent to the RRC filter.

In receive mode this bit will be '0'.

4.5.5.4 Status Register B4: DIBOVF - De-Interleave Buffer Overflow

In receive mode this bit will be set to '1' - also setting the IRQ bit - when a RHB, RILB, RSID or R4S task is written to the Command Register too late to allow continuous reception.

The bit is cleared to '0' immediately after reading the Status Register, by writing a RESET task to the Command Register or by changing the TX/$\overline{RX}$ bit of the Mode Register.

In transmit mode this bit is '0'.

4.5.5.5 Status Register B3: CRCERR - CRC Checksum Error

In receive mode this bit will be updated at the end of a SFP, RHB, RILB or RSID task to reflect the result of the receive CRC check. '0' indicates that the CRC was received correctly, '1' indicates an error. In transmit mode this bit will be '0'.

Note: This bit should be ignored when an 'Intermediate' block (which does not have an integral CRC) is received.

The bit is cleared to '0' by a RESET task, or by changing the TX/$\overline{RX}$ bit of the Mode Register.

4.5.5.6 Status Register B2: SRDY - 'S' Symbol Ready

In receive mode, this bit is set to '1' whenever an 'S' symbol has been received. The µC may then read the value of the symbol from the SVAL field of the Status Register. In transmit mode, this bit is set to '1' whenever an 'S' symbol has been transmitted.

The bit is cleared to '0' immediately after a read of the Status Register, by a RESET task or by changing the TX/$\overline{RX}$ bit of the Mode Register.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.5.5.7 Status Register B1, B0: SVAL - Received 'S' Symbol Value

In receive mode, these two bits reflect the value of the latest received 'S' symbol. In transmit mode, these two bits will be '0'.

4.5.6 Data Quality Register

In transmit mode and for 64 symbol times after enabling receive mode or after starting an AQSC or AQLEV sequence the value in the Data Quality Register will be invalid.

In receive mode, the MX929A continually measures the 'quality' of the received signal, by comparing the actual received waveform over the previous 64 symbol times against an internally generated 'ideal'.

The result is placed into bits 3-7 of the Data Quality Register for the µC to read at any time, bits 0-2 being always set to '0'. Figure 15 shows how the value (0-255) read from the Data Quality Register varies with received signal-to-noise ratio:

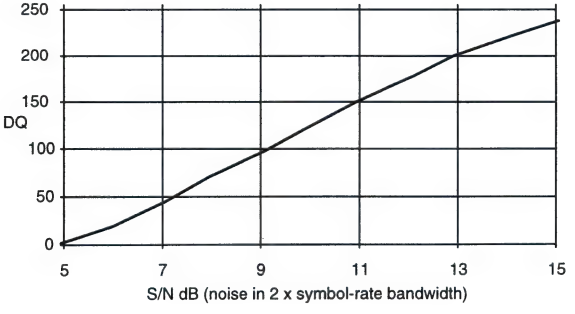


Figure 15: Typical Data Quality Reading vs S/N

4.6 CRC, FEC and Interleaving

4.6.1 Cyclic Redundancy Codes

4.6.1.1 CRC0

This is a six-bit CRC check code used in the Station ID Block. It is calculated by the modem from the first 24 bits of the block (Bytes 0,1 & 2) as follows:

The 24 bits are considered as the coefficients of a polynomial M(x) of degree 23, such that the msb bit (7) of byte 0 is the coefficient of x^{23}, and bit 0 of byte 2 is the coefficient of x^0.

The polynomial F(x) of degree 5 is calculated as being the remainder of the modulo-2 division

$$x^6 M(x) / (x^6 + x^4 + x^3 + 1)$$

The polynomial $x^5 + x^4 + x^3 + x^2 + x^1 + x^0$ is added (modulo-2) to F(x)

The coefficients of F(x) are placed in the 6-bit CRC0 field, such that the coefficient of x^5 corresponds to the msb of CRC0.

4.6.1.2 CRC1

This is a sixteen-bit CRC check code contained in bytes 10 and 11 of the Header Block. It is calculated by the modem from the first 80 bits of the block (Bytes 0 to 9 inclusive) using the generator polynomial:

$$x^{16} + x^{12} + x^5 + 1$$

4.6.1.3 CRC2

This is a thirty-two-bit CRC check code contained in bytes 8 to 11 of the 'Last' Block. It is calculated by the modem from all of the data and pad bytes in the Intermediate Blocks and in the first 8 bytes of the Last Block using the generator polynomial:

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1$$

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Note: In receive mode the CRC2 checksum circuits are initialized on completion of any task other than NULL or RILB. In transmit mode the CRC2 checksum circuits are initialized on completion of any task other than NULL, TIB or TLB.

4.6.2 Forward Error Correction

In transmit mode, the MX929A uses a Trellis Encoder to translate the 96 bits (12 bytes) of a 'Header', 'Intermediate' or 'Last' Block or the 30 bits of a Station ID Block into a 66 or 22-symbol sequence which includes FEC information.

In receive mode, the MX929A decodes the received 22 or 66 symbols of a block into 30 or 96 bits of binary data using a 'Soft Decision' Viterbi algorithm to perform decoding and error correction.

4.6.3 Interleaving

The 66 symbols of a 'Header', 'Intermediate' or 'Last' block are interleaved by the modem before transmission (and before the 'S' symbols are added) to give protection against the effects of noise bursts and short fades. The 22 symbols of a 'Station ID' Block are not interleaved.

In receive mode, the MX929A de-interleaves the received symbols after stripping out the 'S' symbols and prior to decoding.

5. Application Notes

5.1 Transmit Frame Example

The operations needed to transmit a single Frame consisting of Symbol and Frame Sync sequences, Station ID block, and one each Header, Intermediate and Last blocks are shown below:

1. Ensure that the Control Register has been loaded with a suitable CKDIV value, that the IRQEN and TX/$\overline{RX}$ bits of the Mode Register are '1', the RXEYE, PSAVE and SSIEN bits are '0' and the INVSYM bit is set appropriately.
2. Read the Status Register to ensure that the BFREE bit is '1', then write 6 Symbol Sync bytes to the Data Block Buffer and a T24S task to the Command Register.
3. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
4. Write 6 Frame Sync bytes to the Data Block Buffer and a T24S task to the Command Register.
5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
6. Write 3 Station ID bytes to the Data Block Buffer and a TSID task to the Command Register.
7. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
8. Write 10 Header Block bytes to the Data Block Buffer and a THB task to the Command Register.
9. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
10. Write 12 Intermediate Block bytes to the Data Block Buffer and a TIB task to the Command Register.
11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
12. Write 8 Last Block bytes to the Data Block Buffer and a TLB task to the Command Register.
13. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the IBEMPTY bit should be '0'.
14. Wait for another interrupt from the modem, read the Status Register; the IRQ, BFREE and IBEMPTY bits should be '1'.

Note: The final symbol of the frame will start to appear approximately 2 symbol times after the Status Register IBEMPTY bit goes to '1'; a further 16 symbol times should be allowed for the symbol to pass completely through the RRC filter.

The SSYM bits of the Mode Register may be altered at any time to change the transmitted 'S' symbols. If a timing reference is required, setting the Mode Register SSIEN bit to '1' will cause a µC interrupt after every 'S' symbol transmitted - in which case the µC will have to distinguish between interrupts caused by the BFREE bit going to '1', and those caused by the SRDY bit being set to '1'.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Figure 16 and Figure 17 illustrate the host µC routines needed to send a single Frame consisting of Symbol and Frame Sync patterns, a Station ID Block, a Header Block, any number of Intermediate Blocks and one Last Block. It is assumed that the Tx Interrupt Service routine (Figure 17) is called when the MX929A's $\overline{IRQ}$ outline goes low.

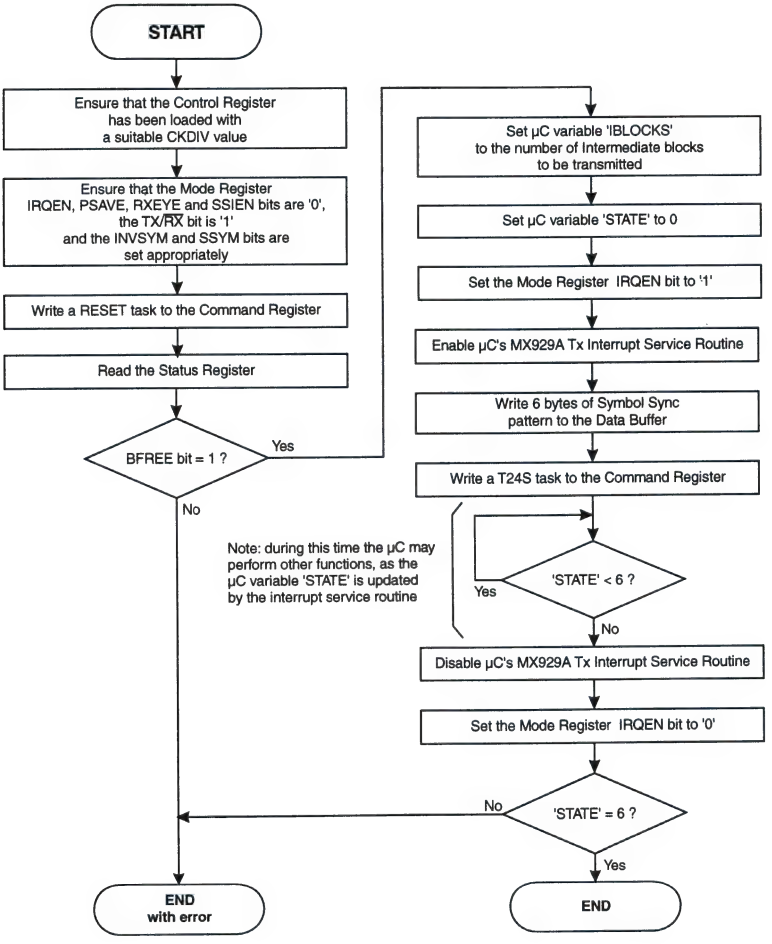

START
Ensure that the Control Register has been loaded with a suitable CKDIV value
Ensure that the Mode Register IRQEN, PSAVE, RXEYE and SSIEN bits are '0', the TX/RX bit is '1' and the INVSYM and SSYM bits are set appropriately
Write a RESET task to the Command Register
Read the Status Register
BFREE bit = 1 ?
Yes
No
Set µC variable 'IBLOCKS' to the number of Intermediate blocks to be transmitted
Set µC variable 'STATE' to 0
Set the Mode Register IRQEN bit to '1'
Enable µC's MX929A Tx Interrupt Service Routine
Write 6 bytes of Symbol Sync pattern to the Data Buffer
Write a T24S task to the Command Register
Note: during this time the µC may perform other functions, as the µC variable 'STATE' is updated by the interrupt service routine
'STATE' < 6 ?
Yes
No
Disable µC's MX929A Tx Interrupt Service Routine
Set the Mode Register IRQEN bit to '0'
'STATE' = 6 ?
No
Yes
END with error
END

Figure 16: Transmit Frame Example Flowchart , Main Program

Note: The RESET command in Figure 16 and the practice of disabling the MX929A's $\overline{IRQ}$ output when not needed are essential, but can eliminate problems during debugging and if errors occur in operation. The CRC bit should be set appropriately when a byte is written to the Command Register.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

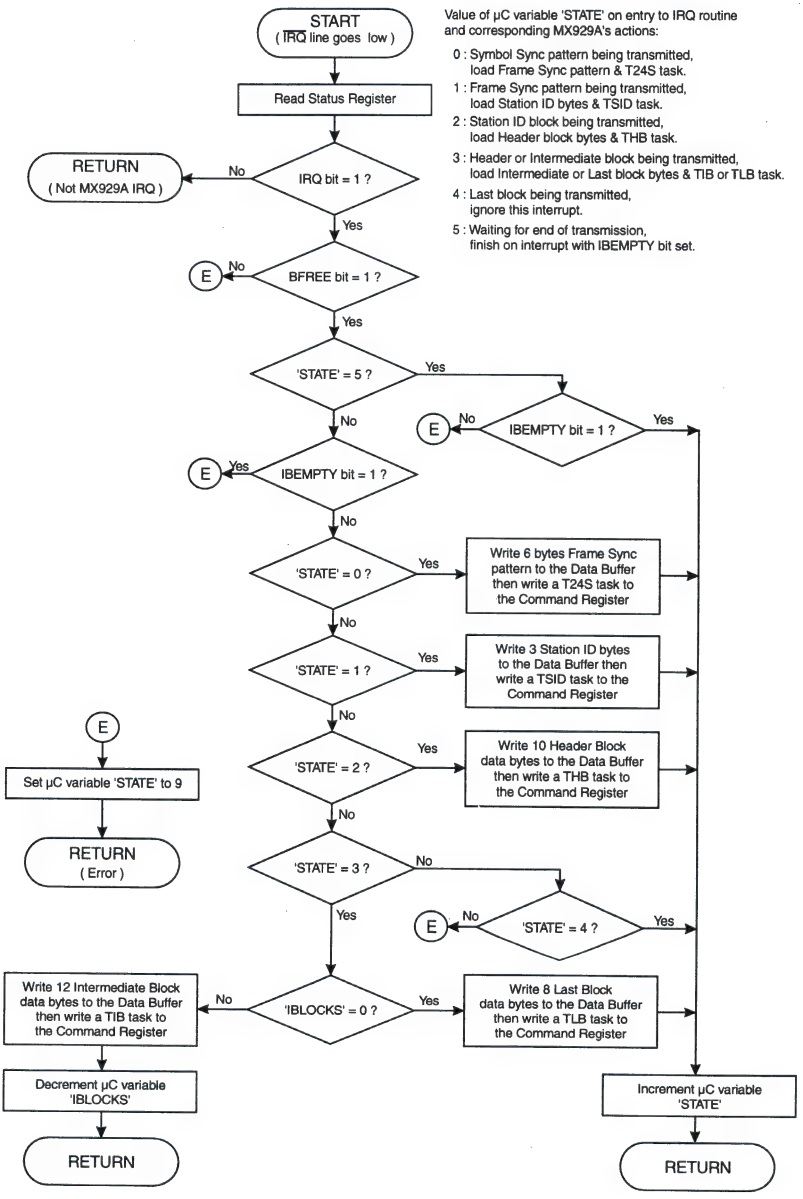

START
(IRQ line goes low)
Read Status Register
IRQ bit = 1 ?
No
RETURN
(Not MX929A IRQ)
Yes
BFREE bit = 1 ?
No
E
Yes
'STATE' = 5 ?
Yes
No
IBEMPTY bit = 1 ?
No
E
Yes
IBEMPTY bit = 1 ?
Yes
E
No
'STATE' = 0 ?
Yes
Write 6 bytes Frame Sync pattern to the Data Buffer then write a T24S task to the Command Register
No
'STATE' = 1 ?
Yes
Write 3 Station ID bytes to the Data Buffer then write a TSID task to the Command Register
No
'STATE' = 2 ?
Yes
Write 10 Header Block data bytes to the Data Buffer then write a THB task to the Command Register
No
'STATE' = 3 ?
No
Yes
E
No
'STATE' = 4 ?
Yes
E
Set µC variable 'STATE' to 9
RETURN
(Error)
Write 12 Intermediate Block data bytes to the Data Buffer then write a TIB task to the Command Register
No
'IBLOCKS' = 0 ?
Yes
Write 8 Last Block data bytes to the Data Buffer then write a TLB task to the Command Register
Decrement µC variable 'IBLOCKS'
RETURN
Increment µC variable 'STATE'
RETURN
Value of µC variable 'STATE' on entry to IRQ routine and corresponding MX929A's actions:
0 : Symbol Sync pattern being transmitted, load Frame Sync pattern & T24S task.
1 : Frame Sync pattern being transmitted, load Station ID bytes & TSID task.
2 : Station ID block being transmitted, load Header block bytes & THB task.
3 : Header or Intermediate block being transmitted, load Intermediate or Last block bytes & TIB or TLB task.
4 : Last block being transmitted, ignore this interrupt.
5 : Waiting for end of transmission, finish on interrupt with IBEMPTY bit set.

Figure 17: Transmit Interrupt Service Routine

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

5.2 Receive Frame Example

The operations needed to receive a single Frame consisting of Symbol and Frame Sync sequences, Station ID block and one each Header, Intermediate and Last blocks are shown below;

1. Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values, and that the IRQEN bit of the Mode Register is '1', the TX/$\overline{RX}$, RXEYE PSAVE, and SSIEN bits are '0', and the INVSYM bit is set appropriately.
2. Wait until the received carrier has been present for at least 8 symbol times (see section 5.3).
3. Read the Status Register to ensure that the BFREE bit is '1'.
4. Write a byte containing a SFP task with the AQSC and AQLEV bits set to '1' to the Command Register.
5. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the CRCERR and DIBOVF bits should be '0'.
6. Read 3 Station ID bytes from the Data Block Buffer.
7. Write a RHB task to the Command Register.
8. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
9. Check that the CRCERR bit of the Status Register is '0' and read 10 Header Block bytes from the Data Block Buffer.
10. Write a RILB task to the Command Register.
11. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
12. Read 12 Intermediate Block bytes from the Data Block Buffer.
13. Write a RILB task to the Command Register.
14. Wait for an interrupt from the modem, read the Status Register; the IRQ and BFREE bits should be '1' and the DIBOVF bit '0'.
15. Check that the CRCERR bit of the Status Register is '0' and read the 8 Last Block bytes from Data Buffer.

Note: The value of the latest 'S' symbol received will be contained in the SVAL bits each time that the Status Register is read. If desired, the Mode Register SSIEN bit may be set to '1', which will cause a µC interrupt after every 'S' symbol is received - in which case the µC will have to distinguish between interrupts caused by the BFREE bit going to '1', and those caused by the SRDY bit being set to '1'.

Figure 18 and Figure 19 illustrate the host µC routines needed to receive a single Frame consisting of Symbol and Frame Sync patterns, a Station ID Block, a Header Block, any number of Intermediate Blocks and one Last Block. It is assumed that the Rx Interrupt service routine (Figure 19) is called when the MX929A's $\overline{IRQ}$ output line goes low.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

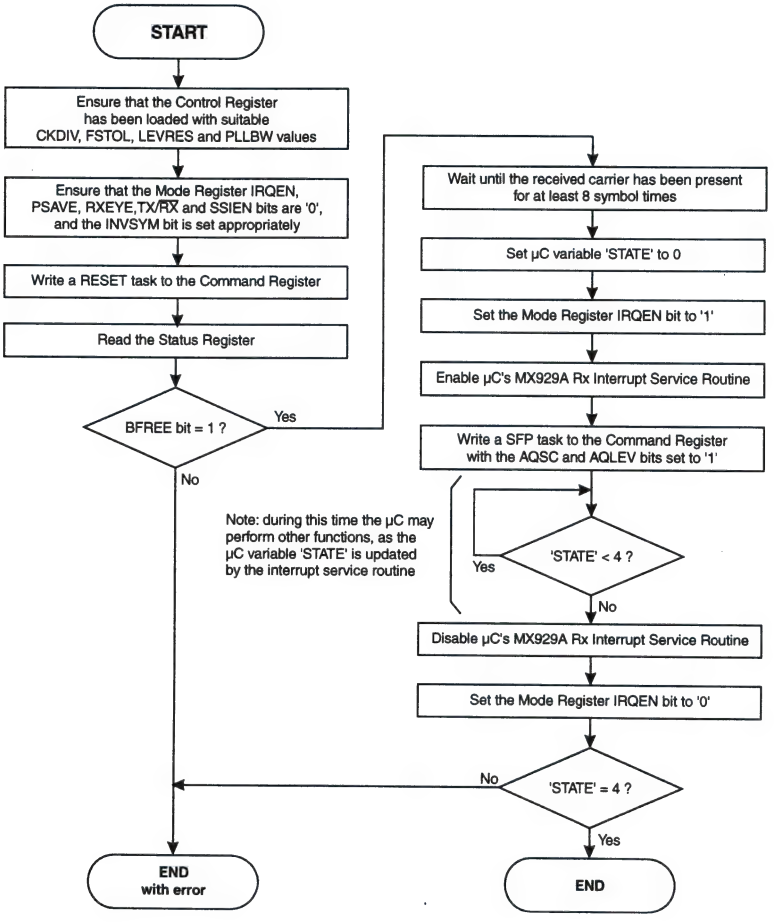

START
Ensure that the Control Register has been loaded with suitable CKDIV, FSTOL, LEVRES and PLLBW values
Ensure that the Mode Register IRQEN, PSAVE, RXEYE,TX/RX and SSIEN bits are '0', and the INVSYM bit is set appropriately
Write a RESET task to the Command Register
Read the Status Register
BFREE bit = 1 ?
Yes
No
Wait until the received carrier has been present for at least 8 symbol times
Set µC variable 'STATE' to 0
Set the Mode Register IRQEN bit to '1'
Enable µC's MX929A Rx Interrupt Service Routine
Write a SFP task to the Command Register with the AQSC and AQLEV bits set to '1'
Note: during this time the µC may perform other functions, as the µC variable 'STATE' is updated by the interrupt service routine
'STATE' < 4 ?
Yes
No
Disable µC's MX929A Rx Interrupt Service Routine
Set the Mode Register IRQEN bit to '0'
'STATE' = 4 ?
No
Yes
END with error
END

Figure 18: Receive Frame Example Flowchart, Main Program

Note: The RESET command in Figure 18 and the practice of disabling the MX929A's $\overline{IRQ}$ output when not needed are not essential, but can eliminate problems during debugging and if errors occur in operation. The CRC bit should be set appropriately when a byte is written to the Command Register.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

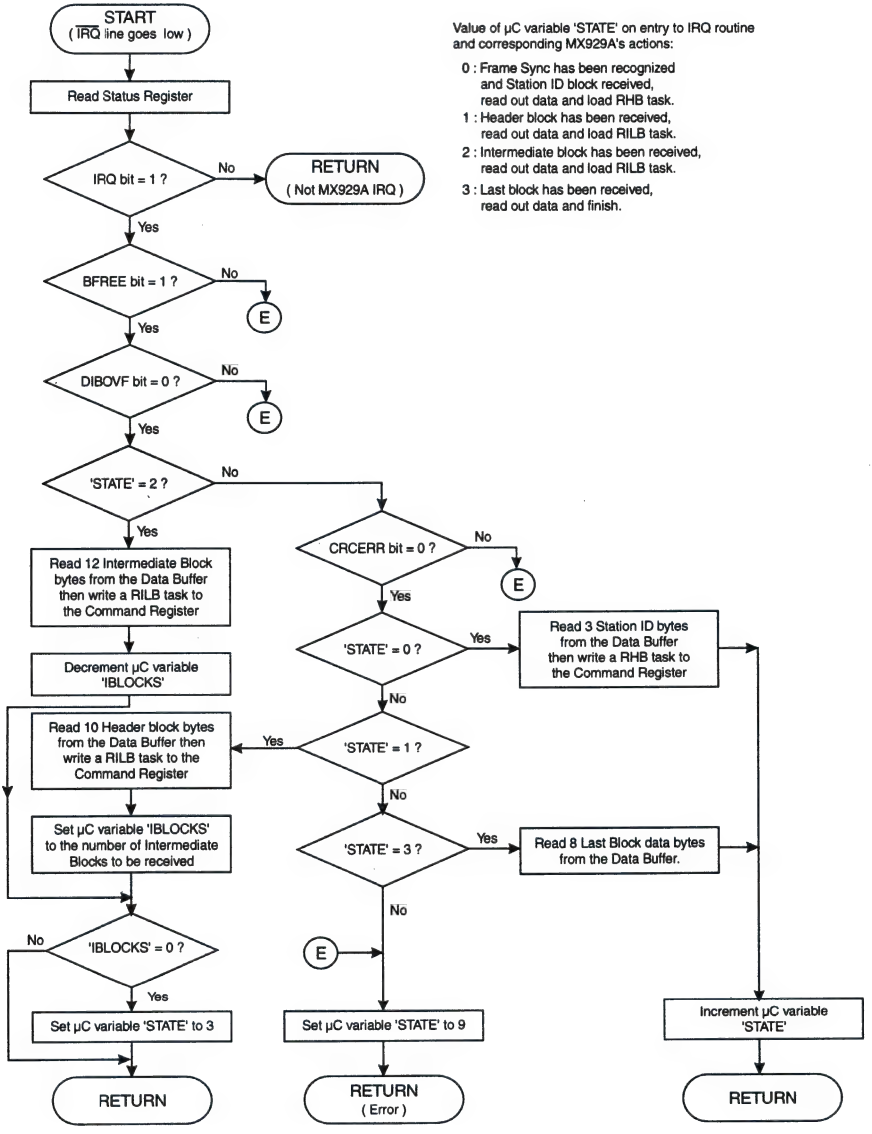

START
(IRQ line goes low)
Read Status Register
IRQ bit = 1 ?
No
RETURN
(Not MX929A IRQ)
Yes
BFREE bit = 1 ?
No
E
Yes
DIBOVF bit = 0 ?
No
E
Yes
'STATE' = 2 ?
No
Yes
Read 12 Intermediate Block bytes from the Data Buffer then write a RILB task to the Command Register
Decrement µC variable 'IBLOCKS'
Read 10 Header block bytes from the Data Buffer then write a RILB task to the Command Register
Set µC variable 'IBLOCKS' to the number of Intermediate Blocks to be received
No
'IBLOCKS' = 0 ?
Yes
Set µC variable 'STATE' to 3
RETURN
CRCERR bit = 0 ?
No
E
Yes
'STATE' = 0 ?
Yes
Read 3 Station ID bytes from the Data Buffer then write a RHB task to the Command Register
No
'STATE' = 1 ?
Yes
No
'STATE' = 3 ?
Yes
Read 8 Last Block data bytes from the Data Buffer.
No
E
Set µC variable 'STATE' to 9
RETURN
(Error)
Increment µC variable 'STATE'
RETURN
Value of µC variable 'STATE' on entry to IRQ routine and corresponding MX929A's actions:
0 : Frame Sync has been recognized and Station ID block received, read out data and load RHB task.
1 : Header block has been received, read out data and load RILB task.
2 : Intermediate block has been received, read out data and load RILB task.
3 : Last block has been received, read out data and finish.

Figure 19: Receive Interrupt Service Routine

Note: This routine assumes that the number of Intermediate Blocks in the Frame are contained within the header Block

5.3 Clock Extraction and Level Measurement Systems

The MX929A is intended for use in systems where the Symbol Sync pattern is transmitted immediately on start-up of the transmitter.

When the carrier is detected by the receiver or when the receiver is switched to another channel, the controlling µC should wait approximately 8 symbol times for the received signal to propagate through the modem's RRC filter then issue a SFS or SFP task with the AQSC and AQLEV bits set to '1'. The 8-symbol delay can usefully be included in the carrier detect circuitry.

Setting the AQSC and AQLEV bits to '1' triggers the modem's automatic Symbol Clock Extraction and Level Measurement acquisition sequences, which are designed to measure the received symbol timing, amplitude and dc offset as quickly as possible during the Symbol Sync period before switching to more accurate - but slower - measurement modes for the remainder of the received message.

Note: If the acquisition sequences are triggered after the Symbol Sync period - as can happen when the receiver is switched to another channel - they will still function correctly, but will take much longer to acquire accurate level and timing information.

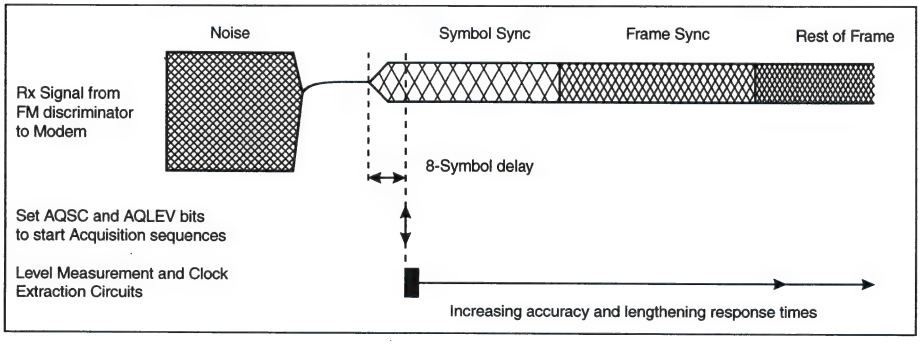

Noise
Symbol Sync
Frame Sync
Rest of Frame
Rx Signal from FM discriminator to Modem
8-Symbol delay
Set AQSC and AQLEV bits to start Acquisition sequences
Level Measurement and Clock Extraction Circuits
Increasing accuracy and lengthening response times

Figure 20: Acquisition sequence Timing

The operation of the Level Acquisition Sequence depends on the settings of the Control Register LEVRES bits:

LEVRES setting:	B3	B2	Details of Level Acquisition Sequence
'Hold'	0	0	1 symbol time of 'Clamp' mode then 15 symbol times of 'Lossy Peak Detect' mode before reverting to 'Hold' mode.
'Slow Peak Detect'	0	1	1 symbol time of 'Clamp' mode then 15 symbol times of 'Lossy Peak Detect' mode before reverting to 'Slow Peak Detect' mode.
'Lossy Peak Detect'	1	0	1 symbol time of 'Clamp' mode before reverting to 'Lossy Peak Detect' mode
'Clamp'	1	1	Remain in 'Clamp' mode.

The 1-symbol 'Clamp' time at the start of these sequences is used to make an initial measurement of the dc offset present on the received signal, after which the 'Lossy Peak Detect' period is used to estimate the signal amplitude.

© 1997 MX•COM, INC.

The operation of the Symbol Clock Acquisition Sequence depends on the settings of the Control Register PLLBW bits:

PLLBW setting:	B1	B0	Details of Symbol Clock Acquisition Sequence
'Hold'	0	0	16 symbol times of 'Extra-wide BW' mode followed by 30 symbol times of 'Wide BW' mode before reverting to 'Hold' mode.
'Narrow' BW	0	1	16 symbol times of 'Extra-wide BW' mode followed by 30 symbol times of 'Wide BW' mode before reverting to 'Narrow BW' mode.
'Medium BW'	1	0	16 symbol times of 'Extra-wide BW' mode followed by 30 symbol times of 'Wide BW' before reverting to 'Medium BW' mode.
'Wide BW'	1	1	16 symbol times of 'Extra-wide BW' mode before reverting to 'Wide BW' mode.

Note: The 'Extra-wide BW' PLL mode is designed to synchronize rapidly to the '+3 +3 -3 -3 ...' Symbol Sync pattern and is available only as part of an automatic acquisition sequence.

Although not recommended, it is possible to use the modem in a non-standard system where there is an indeterminate delay between the transmitter start-up and the Symbol Sync pattern, or where a receive carrier detect signal is not available to the controlling µC. In these cases the Symbol Sync pattern should be extended to about 100 symbols, and the Control Register LEVRES bits should be set to 'Lossy Peak Detect' and the PLLBW bits to 'Wide BW' before initiating a 'SFS + AQSC + AQLEV' task. Once the Frame Sync pattern has been detected, the Control Register settings may be changed to 'Slow Peak Detect' and 'Medium' or 'Narrow' PLL bandwidth for the remainder of the received message.

5.4 AC Coupling

For a practical circuit, ac coupling from the modem's transmit output to the frequency modulator and between the receiver's frequency discriminator and the receive input of the modem, may be desired. However; there are two problems:

1. AC Coupling of the signal degrades the Bit Error Rate performance of the modem. The following graph illustrates the typical bit error rates at 4800 symbols/sec (without FEC) for differing degrees of ac coupling:

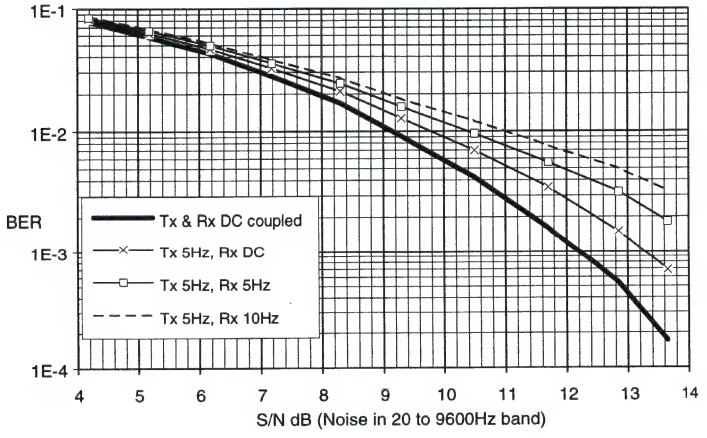


Figure 21: Effect of AC Coupling on BER

2. AC Coupling at the receive input will transform any step in the voltage at the discriminator output to a slowly decaying pulse which can confuse the modem's level measuring circuits. As illustrated in Figure 22, the time for this step to decay to 37% of its original value is 'RC' where:

   RC = 1/(2 x π x the 3dB cut-off frequency of the RC network)

   which is 32 msec, or 153 symbol times at 4800 symbols/sec, for a 5Hz network.

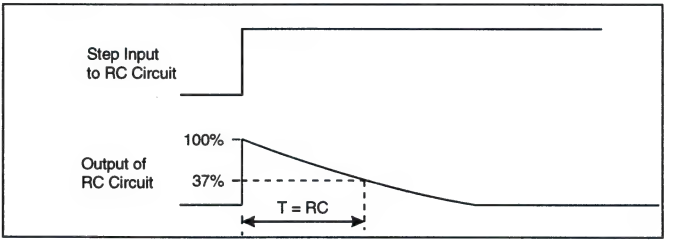


Figure 22: Decay Time - AC Coupling

In general, it is best to dc couple the receiver discriminator to the modem, and to ensure that any AC Coupling to the transmitter's frequency modulator has a -3dB cut-off frequency of no higher than 5Hz (for 4800 symbols/sec).

5.5 Radio Performance

The maximum data rate that can be transmitted over a radio channel using these modems depends on:

- RF channel spacing.
- Allowable adjacent channel interference.
- Symbol rate.
- Peak carrier deviation (modulation index).
- Tx and Rx reference oscillator accuracies.
- Modulator and demodulator linearity.
- Receiver IF filter frequency and phase characteristics.
- Use of error correction techniques.
- Acceptable error rate.

As a guide, 4800 symbols/sec can be achieved, subject to local regulatory requirements, over a system with 12.5kHz channel spacing, if the transmitter frequency deviation is set to ±2.5kHz peak for a repetitive '+3 +3 -3 -3 ....' pattern and the maximum difference between transmitter and receiver 'carrier' frequencies is less than 2400Hz.

The modulation scheme employed by these modems is designed to achieve high data throughput by exploiting as much as possible of the RF channel bandwidth. This does, however, place constraints on the performance of the radio. Particular attention must be paid to:

- Linearity, frequency and phase response of the Tx Frequency Modulator. For a 4800 symbols/sec system, the frequency response should be within ±2dB over the range 3Hz to 5kHz, relative to 2400Hz.
- The bandwidth and phase response of the receiver's IF filters.
- Accuracy of the Tx and Rx reference oscillators, as any difference will shift the received signal towards the skirts of the IF filter response and cause a dc offset at the discriminator output.

Viewing the received signal eye - using the Mode Register RXEYE function - gives a good indication of the overall transmitter/receiver performance.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

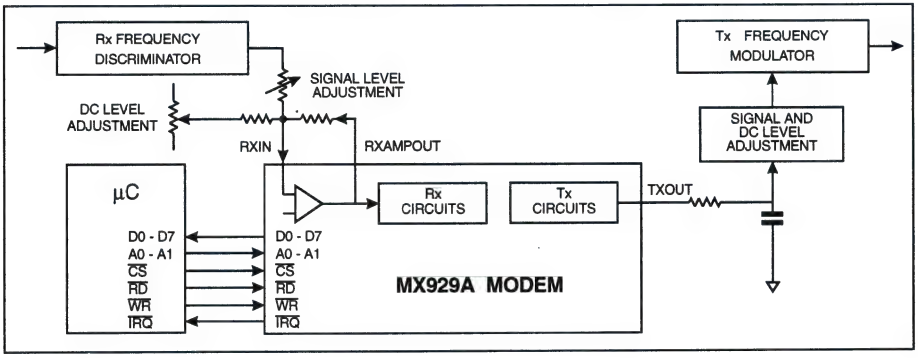


Figure 23: Typical connections Between Radio and MX929A

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW, LH, P Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Temperature		-40	85	°C
Symbol Rate		2400	9600	Symbols/sec
Xtal Frequency		1.0	10.0	MHz

Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 4.9152mhz, Symbol Rate = 4800 symbols/sec,
Noise Bandwidth = 0 to 9600Hz, V_{DD} = 5.0V @ T_{AMB} =25°C

	Notes	Min.	Typ.	Max.	Units
DC PARAMETERS					
I_{DD}	1		4.0	10.0	mA
I_{DD} (V_{DD} = 3.3V)	1		2.5	6.3	mA
I_{DD} (Powersave Mode)	1		1.5		mA
I_{DD} (Powersave Mode, V_{DD} = 3.3V)	1		0.6		mA
AC PARAMETERS					
Tx Output					
TXOUT Impedance	2		1.0	2.5	kΩ
Signal Level	3	0.8	1.0	1.2	V_{P-P}
Output DC Offset wrt V_{DD}/2	4	-0.25		0.25	V
Rx Input					
RXIN Impedance (at 100Hz)			10.0		MΩ
RXIN Amp Voltage Gain (input = 1mV_{RMS} at 100Hz)			300		V/V
Input Signal Level	5	0.7	1.0	1.3	V_{P-P}
DC Offset wrt V_{DD}/2	5	-0.5		0.5	V
Xtal/Clock Input					
'High' Pulse Width	6	40			ns
'Low' Pulse Width	6	40			ns
Input Impedance (at 100Hz)		10.0			MΩ
Gain (input = 1 mV_{RMS} at 100Hz)		20			dB
µC Interface					
Input Logic "1" Level	7, 8	70%			V_{DD}
Input Logic "0" Level	7, 8			30%	V_{DD}
Input Leakage Current (V_{IN} = 0 to V_{DD})	7, 8	-5.0		5.0	µA
Input Capacitance	7, 8		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)	8	92%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)	8, 9			8%	V_{DD}
'Off' State Leakage Current (V_{OUT} = V_{DD})	9			10	µA

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Operating Characteristics Notes:

1. Not including any current drawn from the modem pins by external circuitry other than the Xtal oscillator.
2. Small signal impedance
3. Measured after the external RC filter (R4/C5) for a "+3 +3 -3 -3...." symbol sequence, (output level is proportional to V_{DD}).
4. Measured at the TXOUT pin with the modem in the Tx idle mode.
5. For optimum performance, measured at RXAMPOUT pin, for a "...+3 +3 -3 -3..." symbol sequence optimum level is proportional to V_{DD}.
6. Timing for an external input to the CLOCK/XTAL pin.
7. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0 and A1 pins.
8. D0 - D7 pins.
9. $\overline{IRQ}$ pin.

Timing

µC Parallel Interface Timings (ref. Figure 24)		Notes	Min.	Typ.	Max.	Units
t_{ACSL}	Address valid to $\overline{CS}$ low time		0			ns
t_{AH}	Address hold time		0			ns
t_{CSH}	$\overline{CS}$ hold time		0			ns
t_{CSHI}	$\overline{CS}$ high time	1	6			clock cycles
t_{CSRWL}	$\overline{CS}$ to $\overline{WR}$ or $\overline{RD}$ low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90			ns
t_{RHCSL}	$\overline{RD}$ high to $\overline{CS}$ low time (write)		0			ns
t_{RACL}	Read access time from $\overline{CS}$ low	2			175	ns
t_{RARL}	Read access time from $\overline{RD}$ low	2			145	ns
t_{RL}	$\overline{RD}$ low time		200			ns
t_{RX}	$\overline{RD}$ high to D0-D7 3-state time				50	ns
t_{WHCSL}	$\overline{WR}$ high to $\overline{CS}$ low time (read)		0			ns
t_{WL}	$\overline{WR}$ low time		200			ns

Timing Notes:

1. Xtal/Clock cycles at the XTAL/CLOCK pin.
2. With 30pF max to V_{SS} on D0 - D7 pins.

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc #20480149.003

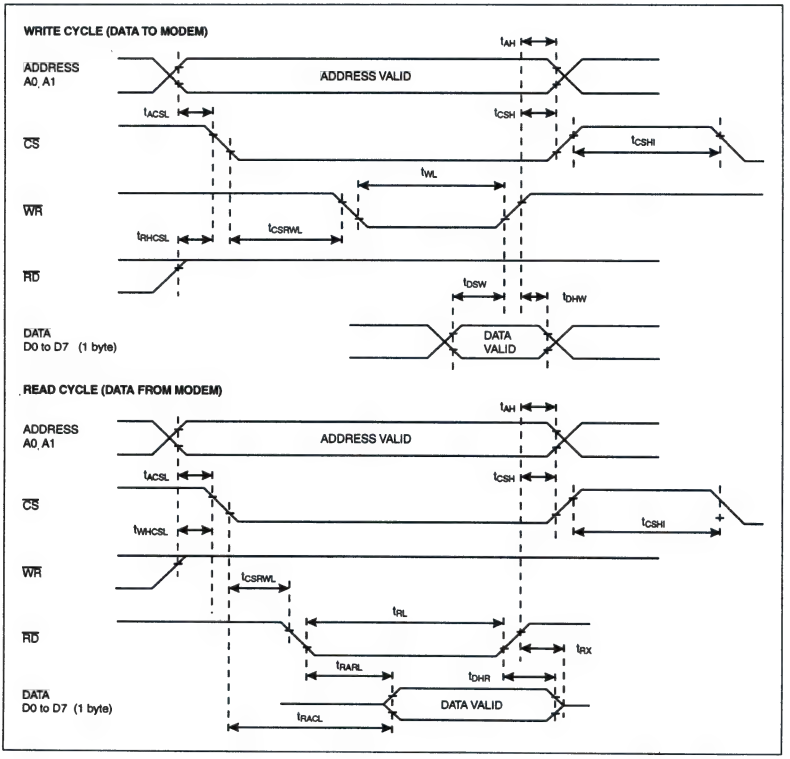


Figure 24: µC Parallel Interface Timings

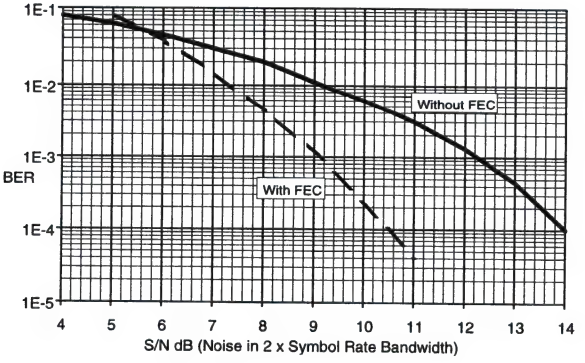
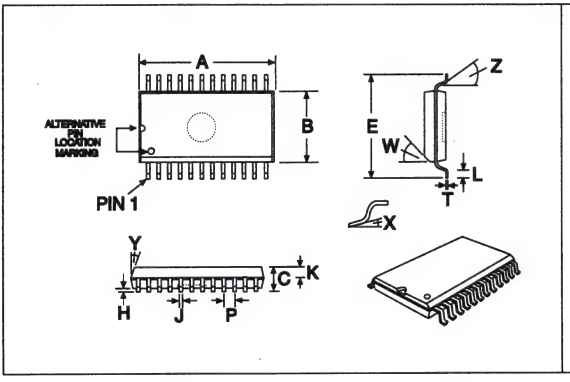


Figure 25: Typical Bit Error Rate With and Without FEC

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

6.2 Packaging

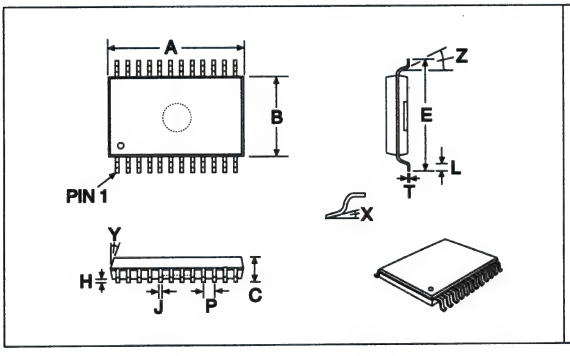


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 26: 24-pin SOIC Mechanical Outline : *Order as part no. MX929ADW*

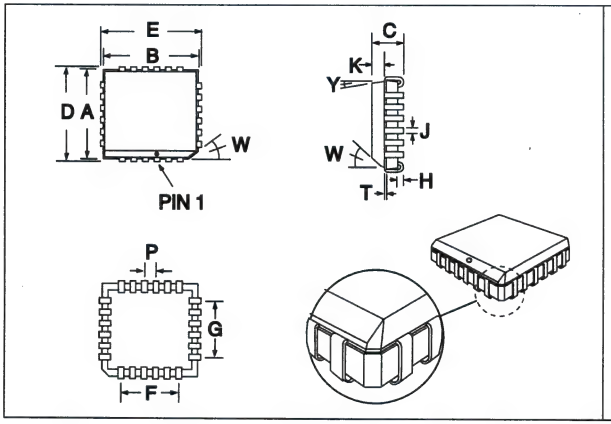


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 27: 24-pin SSOP Mechanical Outline : *Order as part no. MX929ADS*

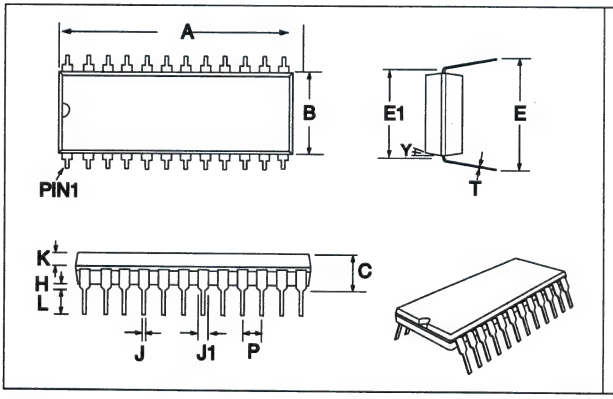


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 28: 24-pin PLCC Mechanical Outline : *Order as part no. MX929ALH*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 29: 24-pin PDIP Mechanical Outline : *Order as part no. MX929AP*

© 1997 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX949 CDPD Wireless Modem Data Pump

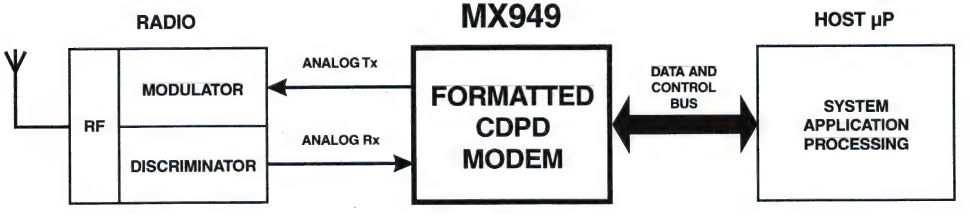
PRELIMINARY INFORMATION

Features

- **19.2 kbps GMSK Modulation**
- **MES (Mobile End Station) Full Duplex Operation**
- **Forward Channel Decoding**
- **Reverse Channel Encoding**
- **Error Detection and Syndrome Output**
- **Low Power Operation for Portable Applications**
- **PCMCIA Compatibility**
- **Sleep Timer Included**
- **3.3V and 5V Applications**
- **Host µP Interface**

Applications

- **CDPD (Cellular Digital Packet Data) Wireless Modem Applications**



The MX949 is a low power CMOS integrated circuit which performs the real-time signal and data format-management functions required for full-duplex operation of a CDPD (Cellular Digital Packet Data) MES.

Interfacing directly with the analog modulation and demodulation circuits of the radio and the host radio/application processor bus, the MX949 accepts application data from the processor, constructs a correct Reverse Channel packet and converts the packet to GMSK analog signals for transmission. In receive, Forward Channel GMSK signals from the discriminator are demodulated, the packet is disassembled, error checked, and the recovered application data passed to the processor.

The MX949 is a cost, size, and power efficient alternative to DSP design solutions in high performance OEM products for the (CDPD) wireless services. The MX949 operates from a 3.0V to 5.5V supply and is available in the following package styles: 40-pin PDIP (MX949P), 44-pin PLCC (MX949LH), and 48-pinTQFP (MX949TG).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Doc. # 20480126.004

CONTENTS

Section	Page
1. Block Diagram	**1-189**
2. Signal List	**1-190**
3. External Components	**1-192**
4. General Description	**1-196**
4.1 Software Description	1-196
4.2 Read Only Registers	1-196
4.3 Write Only Registers	1-198
5. Application	**1-200**
5.1 General	1-200
5.2 Transmitter (Reverse Channel)	1-200
5.3 Receiver (Forward Channel)	1-201
5.4 Timer	1-201
6. Performance Specification	**1-203**
6.1 Electrical Performance	1-203
6.2 Timing	1-205
6.3 Packaging	1-207

MX•COM, Inc. reserves the right to change specifications at any time and without notice

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1. Block Diagram

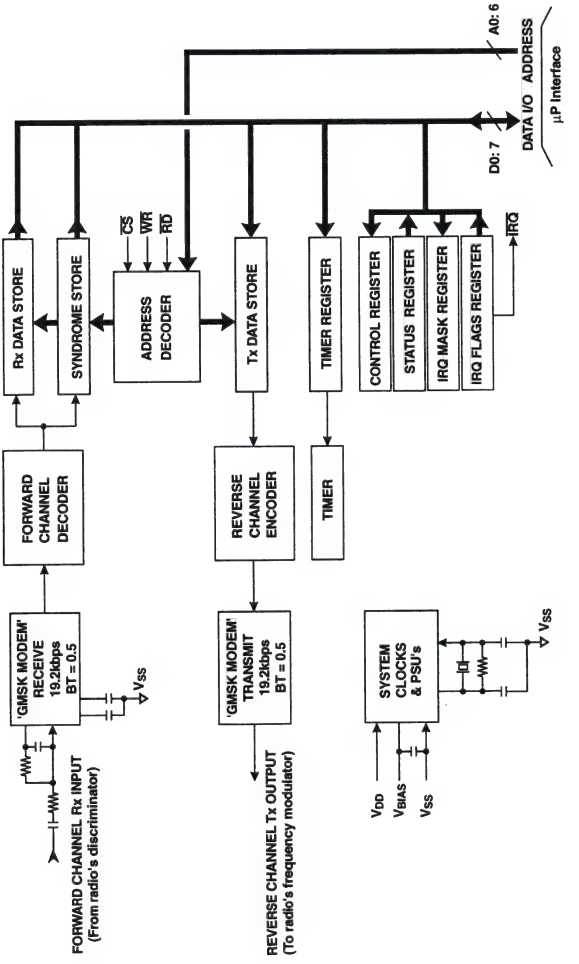


Figure 1: Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. Signal List

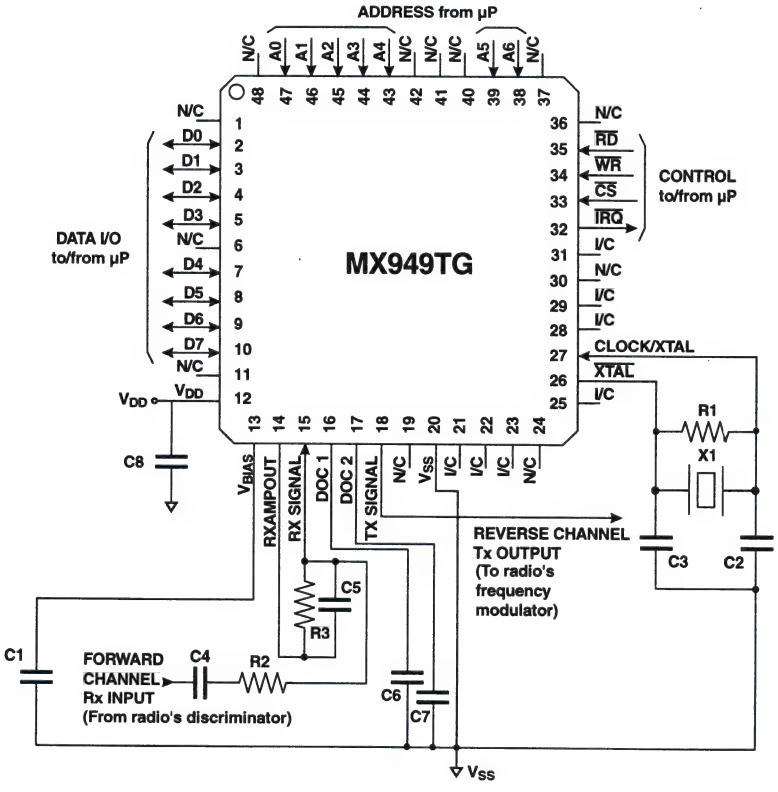
TG	LH	PDIP	Signal		Description
Pin No.	Pin No.	Pin No.	Name	Type	
2	8	37	D0	BUS	8-bit, bi-directional, tristate µP interface data lines
3	9	38	D1	BUS	
4	10	39	D2	BUS	
5	11	40	D3	BUS	
7	12	1	D4	BUS	
8	13	2	D5	BUS	
9	14	3	D6	BUS	
10	15	4	D7	BUS	
12	17	5	V_{DD}	power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pin.
13	18	6	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed by a capacitor mounted close to the device pins (see Figure 2, Figure 3, and Figure 4).
14	19	7	RXAMPOUT	output	Output of the Rx input amplifier.
15	20	8	RX SIGNAL	input	Inverting input to the Rx input amplifier.
16	21	9	DOC 1	output	Connections to the Rx level measurement circuitry. Should be capacitive coupled from pin to V_{SS}.
17	22	10	DOC 2	output	Connections to the Rx level measurement circuitry. Should be capacitive coupled from pin to V_{SS}.
18	23	11	TX SIGNAL	output	Inverted Tx signal output from the modem.
20	24	12	V_{SS}	power	Negative supply (ground).
26	31	17	$\overline{XTAL}$	output	Inverted output of the on-chip oscillator.
27	32	18	CLOCK/XTAL	input	Input to the on-chip oscillator, for external Xtal circuit or clock.
32	36	22	$\overline{IRQ}$	output	A 'wire-ORable' output for connection to the controlling µP Interrupt Request input. When active, this output has a low impedance pull down to V_{SS} and has a high impedance when inactive.
33	37	23	$\overline{CS}$	input	Chip Select. An active low logic level input to the modem, used to enable a data read or write operation.
34	38	24	$\overline{WR}$	input	Write. An active low logic level input used to control the writing of data into the modem from the controlling µP.
35	39	25	$\overline{RD}$	input	Read. An active low logic level input used to control the reading of data from the modem into the controlling µP.
38	41	27	A6	input	7 logic level modem register address select inputs.
39	42	29	A5	input	
43	1	30	A4	input	
44	2	31	A3	input	
45	3	32	A2	input	
46	4	34	A1	input	
47	5	35	A0	input	

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1, 6, 11, 19, 24, 30, 36, 37, 40, 41, 42, 48	6, 7, 16, 28, 30, 40, 43, 44	26, 28, 33, 36	N/C		No internal connection
21, 22, 23, 25, 28, 29, 31	25,26, 27, 29, 33, 34, 35	13, 14, 15, 16, 19, 20, 21	I/C		Internally connected: leave open circuit.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components



R1	1MΩ	±5%
R2	Note 1	±10%
R3	100kΩ	±10%
C1	1µF	±20%
C2	18pF	±20%
C3	18pF	±20%

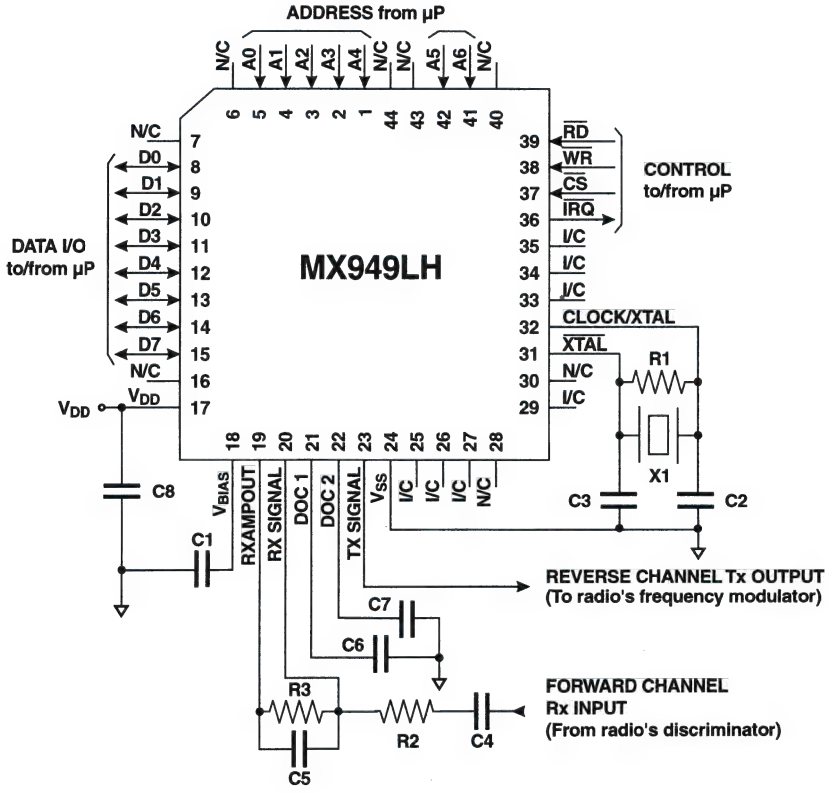
C4	Note 1	±20%
C5	100pF	±20%
C6	6800pF	±20%
C7	6800pF	±20%
C8	0.1µF	±20%
X1	4.9152MHz	see Sec. 6.1

External Component Notes:

1. R2, R3, C4, and C5 form the gain components for the Rx INPUT. R2 and C4 should be chosen as required by the signal input level, using the following formula: Gain = -R3 / R2
2. Connections labeled 'N/C': No internal connection, do not use
3. Connections labeled 'I/C': Internally connected, leave open circuit

Figure 2: Recommended External Components for MX949TG

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



R1	1MΩ	±5%
R2	Note 1	±10%
R3	100kΩ	±10%
C1	1µF	±20%
C2	18pF	±20%
C3	18pF	±20%

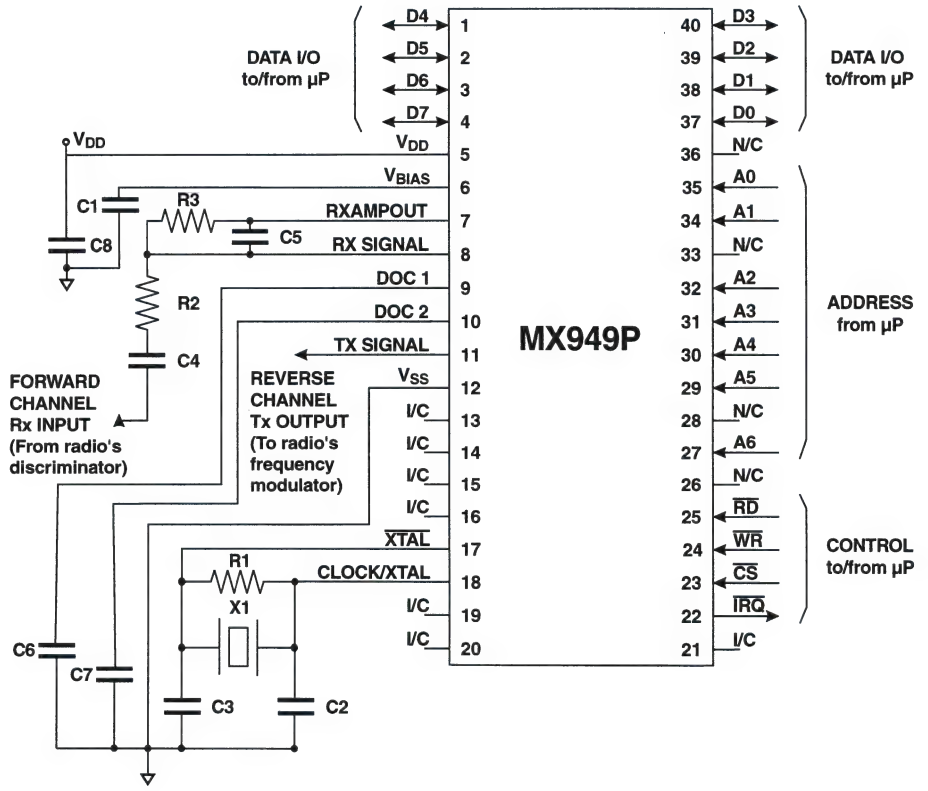
C4	Note 1	±20%
C5	100pF	±20%
C6	6800pF	±20%
C7	6800pF	±20%
C8	0.1µF	±20%
X1	4.9152MHz	see Sec. 6.1

External Component Notes:

1. R2, R3, C4, and C5 form the gain components for the Rx INPUT. R2 and C4 should be chosen as required by the signal input level, using the following formula: Gain = -R3 / R2
2. Connections labeled 'N/C': No internal connection, do not use
3. Connections labeled 'I/C': Internally connected, leave open circuit

Figure 3: Recommended External Components MX949LH

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



R1	1MΩ	±5%
R2	Note 1	±10%
R3	100kΩ	±10%
C1	1µF	±20%
C2	18pF	±20%
C3	18pF	±20%

C4	Note 1	±20%
C5	100pF	±20%
C6	6800pF	±20%
C7	6800pF	±20%
C8	0.1µF	±20%
X1	4.9152MHz	see Sec. 6.1

External Component Notes:

1. R2, R3, C4, and C5 form the gain components for the Rx INPUT. R2 and C4 should be chosen as required by the signal input level, using the following formula: Gain = -R3 / R2
2. Connections labeled 'N/C': No internal connection, do not use
3. Connections labeled 'I/C': Internally connected, leave open circuit

Figure 4: Recommended External Components for MX949P

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

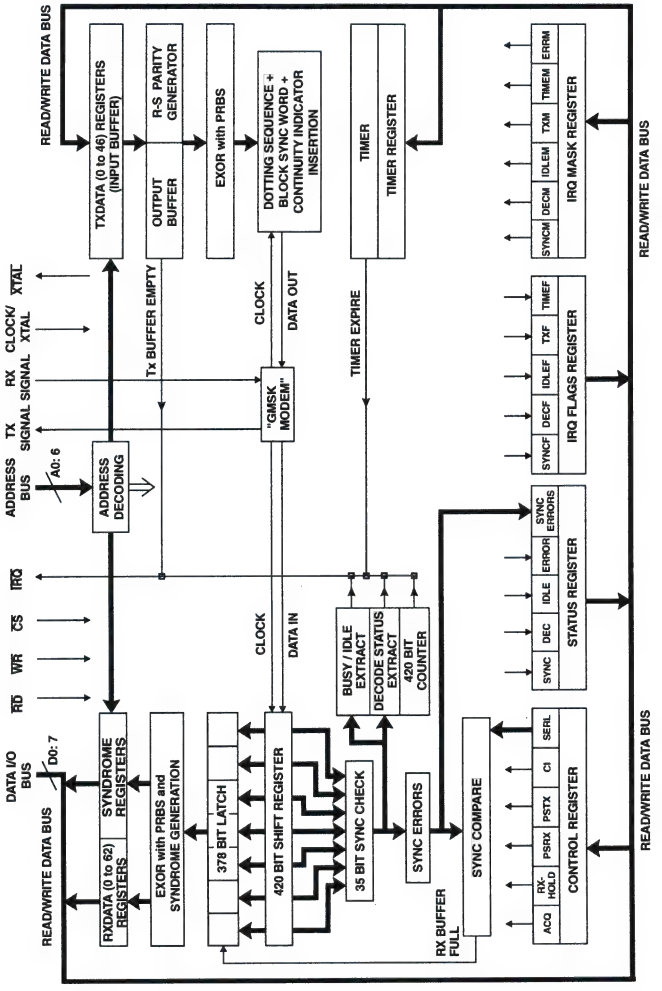


Figure 5: Internal Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4. General Description

This device performs most of the Medium Access Control (MAC) layer functions of the CDPD specification as well as generation of the baseband signals in the physical layer, all of which are specifically for the Mobile End Station (M-ES). For details of the system requirements and telegram formats, the user is referred to "Cellular Digital Packet Data System Specification", Volumes 1 to 5, currently available from:

CDPD Forum Inc.
PO Box 809320
Chicago, IL 60686
United States of America

4.1 Software Description

From the programmer's viewpoint, the MX949 interface consists of a number of registers, addressable from a 7-bit bus with data supplied on a standard 8-bit µP bus, as shown in Figure 5.

4.2 Read Only Registers

A0 - A6 HEX ADDRESS	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$00	0	1	0	RX DATA 0	0	0	DATA SYMBOL 0					
$01	0	1	0	RX DATA 1	0	0	DATA SYMBOL 1					
$02	0	1	0	RX DATA 2	0	0	DATA SYMBOL 2					
I				I			I					
I				I			I					
$3C	0	1	0	RX DATA 60	0	0	DATA SYMBOL 60					
$3D	0	1	0	RX DATA 61	0	0	DATA SYMBOL 61					
$3E	0	1	0	RX DATA 62	0	0	DATA SYMBOL 62					
$3F	0	1	0	RX SYN 1	0	0	SYNDROME SYMBOL 1 = $[r(x)/(x+\alpha^{1})]$					
$40	0	1	0	RX SYN 2	0	0	SYNDROME SYMBOL 2 = $[r(x)/(x+\alpha^{2})]$					
$41	0	1	0	RX SYN 3	0	0	SYNDROME SYMBOL 3 = $[r(x)/(x+\alpha^{3})]$					
$42	0	1	0	RX SYN 4	0	0	SYNDROME SYMBOL 4 = $[r(x)/(x+\alpha^{4})]$					
$43	0	1	0	RX SYN 5	0	0	SYNDROME SYMBOL 5 = $[r(x)/(x+\alpha^{5})]$					
$44	0	1	0	RX SYN 6	0	0	SYNDROME SYMBOL 6 = $[r(x)/(x+\alpha^{6})]$					
$45	0	1	0	RX SYN 7	0	0	SYNDROME SYMBOL 7 = $[r(x)/(x+\alpha^{7})]$					
$46	0	1	0	RX SYN 8	0	0	SYNDROME SYMBOL 8 = $[r(x)/(x+\alpha^{8})]$					
$47	0	1	0	RX SYN 9	0	0	SYNDROME SYMBOL 9 = $[r(x)/(x+\alpha^{9})]$					
$48	0	1	0	RX SYN 10	0	0	SYNDROME SYMBOL 10 = $[r(x)/(x+\alpha^{10})]$					
$49	0	1	0	RX SYN 11	0	0	SYNDROME SYMBOL 11 = $[r(x)/(x+\alpha^{11})]$					
$4A	0	1	0	RX SYN 12	0	0	SYNDROME SYMBOL 12 = $[r(x)/(x+\alpha^{12})]$					
$4B	0	1	0	RX SYN 13	0	0	SYNDROME SYMBOL 13 = $[r(x)/(x+\alpha^{13})]$					
$4C	0	1	0	RX SYN 14	0	0	SYNDROME SYMBOL 14 = $[r(x)/(x+\alpha^{14})]$					
$4D	0	1	0	RX SYN 15	0	0	SYNDROME SYMBOL 15 = $[r(x)/(x+\alpha^{15})]$					
$4E	0	1	0	RX SYN 16	0	0	SYNDROME SYMBOL 16 = $[r(x)/(x+\alpha^{16})]$					
$4F	0	1	0	STATUS	SYNC	DEC	IDLE	ERROR	0	SYNC ERRORS		
$50	0	1	0	IRQ FLAGS	SYNCF	DECF	IDLEF	TXF	TIMEF	0	0	0

4.2.1 Read Only Register Description

4.2.1.1 RXDATA0 to RXDATA62 Registers (Hex address $00 to $3E)

These are read only registers and all 63 registers are each updated with 6-bit symbols every time a valid SYNC occurs. This is indicated by an interrupt (see SYNC, SYNC ERRORS, and SYNC ERROR LIMIT).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.2.1.2 SYNDROME SYMBOL 1 to 16 (Hex address $3F to $4E)

These 16, 6-bit symbols contain the syndrome calculated from the received data (RXDATA 0 to 62). The syndrome is recalculated every time a valid SYNC occurs. An all zero pattern in the 16 syndrome symbols indicates zero errors in the data.

4.2.1.3 STATUS Register (Hex address $4F)

This is a read only register that contains the status of the various functions on the device as described below:

SYNC (Bit 7)	This bit is set to "1" when a forward channel synchronization word has been received successfully. (See SYNC ERRORS and SYNC ERROR LIMIT). This bit is reset to "0" when the sync word has not been detected for more than 420 bits (i.e. sync lost).
DEC (Bit 6)	This bit indicates the decode status of the Mobile Data Base Station (MDBS) on the forward channel. This bit is set to "1" when the station fails to decode data successfully, and is reset to "0" when the station is successful in decoding data. This bit will only change and be valid if SYNC (Bit 7) is set to "1".
IDLE (Bit 5)	This bit indicates the active status of the Mobile Data Base Station (MDBS) on the forward channel. This bit is set to "0" when the station is in an IDLE state, and reset to "1" when the station is in a BUSY state. This bit will only change and be valid if SYNC (Bit 7) is set to "1". The IDLE bit is derived from a majority decision on the five consecutive busy/idle bits, as in the CDPD specification. The first block of data received in the forward channel will not output any data until the sync word has been found. Once this has been found, the most recent (last) idle bit will be output in the STATUS register, and the IDLEF bit will be set to "1" in the IRQ FLAGS register. The next seven idle bits are output as they come in and, so long as the sync word remains correct, successive idle bits are output as they come in.
ERROR (Bit 4)	This bit indicates if there are errors in RXDATA. This bit is set to "0" if all syndrome symbols (1 - 16) are "0", i.e. no errors in the data. This bit is set to "1" if any syndrome symbol is not "0", i.e. errors are present in the data. This bit is updated every time a valid SYNC occurs.
SYNC ERRORS (Bits 2, 1 and 0)	This 3-bit number indicates the number of errors received in the synchronization word. It is updated whenever the synchronization word is in error, less than or equal to the number specified by the SYNC ERROR LIMIT bits of the CONTROL register. It also implies the synchronization word has been received successfully and sets the SYNC bit to "1" (See SYNC above).

4.2.1.4 IRQ FLAGS Register (Hex address $50)

This is a read only register that contains flags to indicate the source of an interrupt, as described below:

SYNCF (Bit 7)	This bit is set to "1" when the device has decoded the sync word on the forward channel. It also is set to "1" if, after detecting sync, it fails to detect it 420 bits later, indicating sync has been lost. The state of sync can be read from the STATUS register. This bit is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated, depending on the state of the IRQ MASK register.
DECF (Bit 6)	This bit is set to "1" when the decode status of the Mobile Data Base Station (MDBS) in the forward channel changes state. The decode state can be read from the STATUS register. This bit is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.
IDLEF (Bit 5)	This bit is set to "1" when the idle status of the Mobile Data Base Station (MDBS) in the forward channel changes state. The idle state can be read from the STATUS register. This bit is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.
TXF (Bit 4)	This bit is used in transmission of data from the 47 symbol "write only" buffer on the reverse channel. This bit is set to "1" when the buffer is empty and new data can be loaded in. It is reset to "0" after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.
TIMEF (Bit 3)	This bit is set to "1" when the timer expires and it is reset after a "read" of the IRQ FLAGS register. When this bit is set to "1" an interrupt may be generated depending on the state of the IRQ MASK register.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.3 Write Only Registers

A0 - A6 HEX ADDRESS	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$00	1	0	0	TX DATA 0	X	X	DATA SYMBOL 0					
$01	1	0	0	TX DATA 1	X	X	DATA SYMBOL 1					
$02	1	0	0	TX DATA 2	X	X	DATA SYMBOL 2					
I				I			I					
I				I			I					
$2C	1	0	0	TX DATA 44	X	X	DATA SYMBOL 44					
$2D	1	0	0	TX DATA 45	X	X	DATA SYMBOL 45					
$2E	1	0	0	TX DATA 46	X	X	DATA SYMBOL 46					
$2F	1	0	0	TIMER	0 TO 255 SECONDS							
$30	1	0	0	CONTROL	ACQ	RX-HOLD	PSRX	PSTX	CI	SYNC ERROR LIMIT (SERL)		
$31	1	0	0	IRQ MASK	SYNCM	DECM	IDLEM	TXM	TIMEM	ERRM	0	0

4.3.1 Write Only Register Description

4.3.1.1 TXDATA0 to TXDATA46 Registers (Hex address $00 to $2E)

These 47 registers can be loaded with 6-bit symbols when the TXF bit in the IRQ FLAGS register is "1". On loading the 47th symbol, the device will generate the 16 symbol parity code and begin the transmit sequence. These registers are buffered, therefore after the TXF bit has gone to "1" there are 47 x 6 bit periods minus the time to generate the 16 parity symbols in which to load all registers, i.e. approximately 14 msec. The controlling µP has to re-load the buffer with new data within this time otherwise the old data will be sent again.

4.3.1.2 TIMER Register (Hex address $2F)

This register sets a timer to expire from 1 to 255 seconds ("0" disables and powersaves it). The time starts from when the register is first set and expires when the programmed time has passed. On expiration, the TIMEF bit is set in the IRQ FLAGS register and an interrupt may occur. The timer is 1-shot and does not restart until it is programmed again. After power up the TIMEF bit should be reset to "0" in order to initialize the timer.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.3.1.3 CONTROL Register (Hex address $30)

This register is used to control the functions of the device as described below:

ACQ (Bit 7)	This bit controls the way in which the receiver locks onto the phase and amplitude of the incoming signal. When a carrier has been detected, this bit should be set high for at least 16 signal-bit periods, during which time the receiver measures the signal level (Fast Peak Detect) and sets its phase locked loop (PLL) bandwidth wide enough to lock to the received signal in less than 8 zero crossings. When the ACQ bit is returned low, level measurement enters the slower but more accurate Averaging Peak Detect mode; the PLL enters its medium bandwidth for about 30 signal-bit periods, after which time it will continue in its narrow bandwidth mode.
RXHOLD (Bit 6)	When this bit is set to "1" the receiver "bit synchronization" PLL will lock. It can be used during times when the signal fades, so that when the signal returns the receiver is still very close to good "bit synchronization". When this bit is set to "0", the device uses its normal PLL acquisition sequence for "bit synchronization". When ACQ is high, the RXHOLD bit has no effect.
PSRX (Bit 5)	When this bit is "1" the receiver is powersaved. When this bit is "0" the receiver is enabled. After power up, this bit should be programmed to "1" in order to initialize the receiver.
PSTX (Bit 4)	When this bit is "1" the transmitter is powersaved. When this bit is "0" the transmitter is enabled. Transmission starts as soon as the PSTX bit goes to "0". Before that time, the CI bit and the TXDATA symbols should be set up for the first transmission. Transmission is terminated as soon as the PSTX bit goes to "1". After power up, this bit should be programmed to "1" in order to initialize the transmitter.
CI (Bit 3)	This bit sets the continuity indicator for transmission. It should be set to "1" when there are more blocks to follow and set to "0" when the last block begins. The first 47 symbol block transmitted after this bit has gone from "0" to "1" is preceded by the "dotting sequence" and the reverse synchronization.
SYNC ERROR LIMIT (SERL) (Bits 2, 1 and 0)	This 3-bit number specifies the maximum number of bits that can be in error in the synchronization word. When the synchronization word is recognized with less than or equal to this number of errors the SYNCF bit is set to "1" and the actual number of errors is loaded into SYNC ERRORS. The RXDATA is then loaded into the registers for "Data Symbols 0 to 62", the Rx syndrome is updated, and an interrupt may be generated, depending on the state of the IRQ MASK register. If 5, 6 or 7 errors are programmed to be accepted in the SYNC ERROR LIMIT, falsing of the forward channel sync word may occur.

4.3.1.4 IRQ MASK Register (Hex address $31)

These bits prevent interrupts from occurring as detailed below:

SYNCM (Bit 7)	When this bit is set to "1" the SYNC interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is set to "0" the SYNC interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
DECM (Bit 6)	When this bit is set to "1" the DEC interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is set to "0" the DEC interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
IDLEM (Bit 5)	When this bit is set to "1" the IDLE interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is set to "0" the IDLE interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
TXM (Bit 4)	When this bit is set to "1" the Tx interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is set to "0" the Tx interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
TIMERM (Bit 3)	When this bit is set to "1" the TIMER interrupt will be gated out to the $\overline{IRQ}$ pin. After this bit is set to "0" the TIMER interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
ERRM (Bit 2)	For systems that are required to work error free and where Reed-Solomon error correction is not implemented, this bit provides the means not to interrupt the controlling µP if errors are detected. When this bit is set to "1" all the interrupts will work as specified. When this bit is set to "0", the SYNC, DEC and IDLE interrupts will be inhibited. The inhibiting of SYNC, DEC, and IDLE interrupts prevents the unnecessary servicing of interrupts by the controlling µP if the on chip Reed-Solomon error detector indicates errors in the data.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. Application

Further information on Reed-Solomon codes may be found in "Error Control Coding" by S. Lin and D.J. Costello, published by Prentice Hall in 1983. The ISBN number is 0-13-283796-X.

The operation of the MX949 can be divided into 3 sections: the Transmitter (reverse channel), the Receiver (forward channel) and the Timer. The operational sequence of each is described below, with reference to the internal block diagram, shown in Figure 5. Data and framing transmission structures are shown in Figure 6 for the reverse channel and in Figure 7 for the forward channel.

5.1 General

1. After power up, enable or disable the interrupts by using the IRQ MASK register, depending on whether the $\overline{IRQ}$ signal or direct polling of the IRQ FLAGS register is being used.
2. After power up, program PSRX (Bit 5 of the CONTROL register) to "1" to initialize the Rx circuitry, i.e:

   reset the interrupts

   reset SYNCF, DECF, IDLEF in the IRQ FLAGS register

   reset SYNC, DEC, IDLE, ERROR, SYNC ERRORS in the STATUS register

   All other Rx registers are not affected and will be in a random state after power up.
3. After power up, program PSTX (Bit 4 of the CONTROL register) to "1" to initialize the Tx circuitry, i.e:

   set TXF in the IRQ register to "1" to indicate that the Tx buffer is empty

   set the interrupt $\overline{IRQ}$, if enabled, to request Tx data from the controlling µP

5.2 Transmitter (Reverse Channel)

1. After power up, a Tx interrupt is generated, if enabled, and TXF (Bit 4 of the IRQ FLAGS register) is set, indicating the output buffer is empty.
2. The transmitter can now be enabled.
3. CI (Bit 3 of the CONTROL register) should be set to "1" when there are more Tx blocks to follow and set to "0" for the last block. If there is only one block to be sent, i.e. the first block is the last block, then the CI bit should be pulsed from "0" to "1" to "0" to ensure that the dotting pattern and block sync are sent and that CI is set to "0" to indicate the presence of the last block, except just after powersave when the dotting sequence and block sync are added automatically.
4. All 47 symbols (0 to 46) are loaded into the TXDATA registers from the controlling µP, finishing the load with the 47th symbol. This set of TXDATA registers is double buffered, therefore any previous data can be sent again by re-loading only symbol 46, i.e. loading symbol 46 indicates that data is ready to be sent.
5. The loading of symbol 46 (as above [4]) triggers the generation of a Reed-Solomon 16 symbol parity code, based on symbols 0 to 46 in the input buffer.
6. The transmitter will wait for the output buffer to become empty (if it is the first transmission it may already be empty). When this condition is met, data is transferred to the output buffer. At this point the data and CI bit (Bit 3 of the CONTROL register) for that block have been defined and will not change while setting up for the next block to be sent.
7. The data is EXORed with the pseudorandom sequence (PRBS) as it is transmitted. Once this is done, the output buffer will be empty and the TXF flag with interrupt will be generated, looping the control sequence back to the first step.
8. The input buffer can be re-loaded while the transmitter is transmitting.
9. The CI (continuity indicator) bit is automatically inserted every 9 symbols, during transmission.
10. The 38 bit "dotting sequence" and 22 bit block synchronization word are added if it is the first transmission after Tx powersave or if the CI bit has just previously gone from "0" to "1" indicating the start of a new transmission block.
11. The signal generated has a data rate of 19.2 kbps and is filtered by a Gaussian filter with a BT of 0.5 in the transmit section of the GMSK modem.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.3 Receiver (Forward Channel)

1. The SYNC ERROR LIMIT (SERL) (Bits 2, 1 and 0 of the CONTROL register) is set from "0" to "7" as required by the application.
2. The receiver is enabled using PSRX (Bit 5 of the CONTROL register).
3. The receiver is now able to receive 19.2 kbps data via the receive section of the GMSK modem, comprising input filter, slicer and bit synchronizer.
4. A continuous stream of data is fed into the receiver input shift register.
5. When the controlling µP receives a carrier detect, it can pulse ACQ (Bit 7 of the CONTROL register) in order to quickly acquire bit synchronization. If carrier detect is not available or, due to powersave requirements, the controlling device remains unpowered, then slower bit synchronization will be acquired in approximately 32 bits.
6. The receiver input shift register is continually monitored for the 35-bit synchronization word interleaved with the data. It correlates the number of errors in the synchronization word with the maximum number allowed (previously programmed into the SYNC ERROR LIMIT bits of the CONTROL register). When it achieves this limit or less, valid data is assumed to be present.
7. The data is EXORed with the pseudorandom sequence (PRBS) and a 16-symbol syndrome is generated. The data and syndrome are then loaded into the Rx output registers, ready for reading by the controlling µP.
8. DEC (Bit 6) and IDLE (Bit 5) of the STATUS register are set according to the data received.
9. SYNCF (Bit 7 of the IRQ FLAGS register) is set and an IRQ is generated. SYNC (Bit 7 of the STATUS register) is set to "1". This indicates that a new block of data has successfully been received and is available for reading by the controlling µP.
10. With the first block sync received, the device now checks the DEC and IDLE positions in the next block of data and outputs them with interrupts as they are counted in.
11. On-chip circuitry predicts when the next block sync will arrive. If it arrives before that time, the circuit is reset and the sequence loops back to step (6). If the time expires, the SYNCF and IRQ signals will be generated and SYNC (Bit 7 of the STATUS register) will be set to "0", indicating that block sync has been lost and DEC, IDLE and RXDATA are no longer valid.

5.4 Timer

1. The IRQ FLAGS register is read, to reset TIMEF (Bit 3).
2. The TIMER register is programmed with the time required, from 1 to 255 seconds, starting the time-out.
3. IRQ and TIMEF are set when time expires.
4. This timer can be used to implement the "sleep mode", as described in the CDPD specification.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

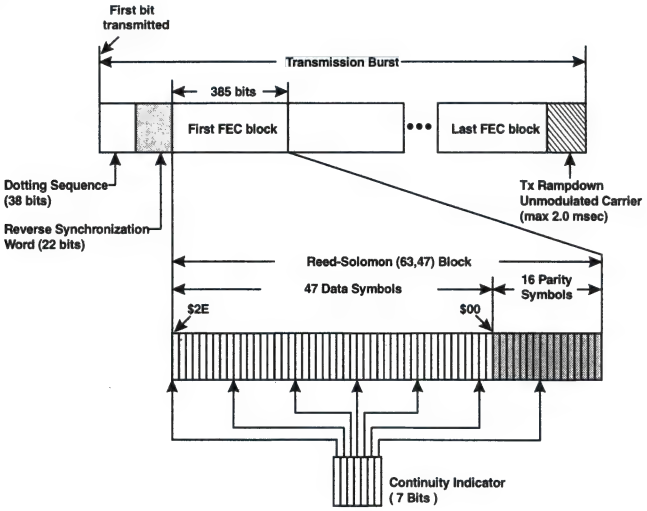


Figure 6: Reverse Channel Transmission Structure

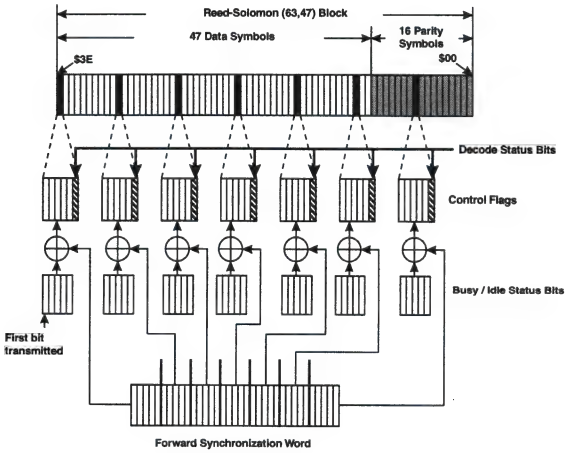


Figure 7: Forward Channel Transmission Structure

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin (wrt V_{SS})	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
TG Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-40	85	°C
Operating Temperature	-40	85	°C
LH / P Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-40	85	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Xtal Frequency		4.9149	4.9155	MHz
Temperature		-40	85	°C

Note: For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of VDD, peak to peak. Tuning fork crystals cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer. Operation of this device without a Xtal or Clock input may cause device damage.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 4.9152MHz, Bit Rate = 19.2 kbps,
V_{DD} = 5.0V @ T_{AMB} = 25°C

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (all enabled)	1		5.0	7.0	mA
I_{DD} (all enabled) (V_{DD} = 3.0V)	1		2.0	3.0	mA
I_{DD} (powersaved)	1		1.3	2.0	mA
I_{DD} (powersaved) (V_{DD} = 3.0V)	1		0.5	1.0	mA
AC Parameters					
Tx Output					
Tx Output Impedance (Tx enabled)	2		1.0	2.5	kΩ
Tx Output Impedance (powersaved)	2	300	500		kΩ
Output Signal Level	3	0.9	1.0	1.1	V_{P-P}
Power up to Tx Output Stable	4		3	5	bits
Rx Input					
Rx Input Impedance (at 100Hz)		10			MΩ
Rx Input Amp Voltage Gain (Input = 1 mV_{RMS} at 100Hz)		500			V/V
Input Signal Level	5	0.7	1.0	1.3	V_{P-P}
Xtal/Clock Input					
'High' Pulse Width	6	40			ns
'Low' Pulse Width	6	40			ns
Input Impedance (at 100Hz)		10			MΩ
Gain (Input = 1mV_{RMS} at 100Hz)		20			dB
µP Interface					
Input Logic "1" Level	7, 8	70%			V_{DD}
Input Logic "0" Level	7, 8			30%	V_{DD}
Input Leakage Current (V_{IN} = 0 to V_{DD})	7, 8	-5.0		5.0	µA
Input Capacitance	7, 8		10.0		pF
Output Logic "1" Level (I_{OH} = 120µA)	8	90%			V_{DD}
Output Logic "0" Level (I_{OL} = 360µA)	8, 9			10%	V_{DD}
'Off' State Leakage Current (V_{OUT} = V_{DD})	9			10	µA

Operating Characteristics Notes:

1. Not including any current drawn from the modem pins by external circuitry.
2. Small signal impedance
3. For 1111000011110000.. bit sequence, (output level is proportional to V_{DD}).
4. Measured between setting PSTX to "'0" and TXSIGNAL becoming stable.
5. For optimum performance, measured at RXAMPOUT pin,for a '...11110000...' bit sequence
6. Timing for an external input to the Clock/XTAL pin.
7. $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, A0 - A6 pins.
8. D0 - D7 pins.
9. $\overline{IRQ}$ pin.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.2 Timing

6.2.1 Interface Timing

For the following conditions unless otherwise specified:

Xtal Frequency = 4.9152MHz, V_{DD} = 5.0V @ T_{AMB} = 25°C

µP Interface Timings (ref. Figure 8)		Notes	Min.	Typ.	Max.	Units
t_{ACSL}	Address valid to $\overline{CS}$ low time		0			ns
t_{AH}	Address hold time		10			ns
t_{CSH}	$\overline{CS}$ hold time		0			ns
t_{CSHI}	$\overline{CS}$ high time		6			clock cycles
t_{CSRWL}	$\overline{CS}$ to $\overline{WR}$ or $\overline{RD}$ low time		0			ns
t_{DHR}	Read data hold time		0			ns
t_{DHW}	Write data hold time		0			ns
t_{DSW}	Write data setup time		90			ns
t_{RHCSL}	$\overline{RD}$ high to $\overline{CS}$ low time (write)		0			ns
t_{RACL}	Read access time from $\overline{CS}$ low	1			175	ns
t_{RARL}	Read access time from $\overline{RD}$ low	1			145	ns
t_{RL}	$\overline{RD}$ low time		200			ns
t_{RX}	$\overline{RD}$ high to D0: 7 tristate time				50	ns
t_{WHCSL}	$\overline{WR}$ high to $\overline{CS}$ low time (read)		0			ns
t_{WL}	$\overline{WR}$ low time		200			ns

Timing Notes:

1. With 30pF max. to V_{SS} on D0: 7 pins.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.2.2 Timing Diagrams

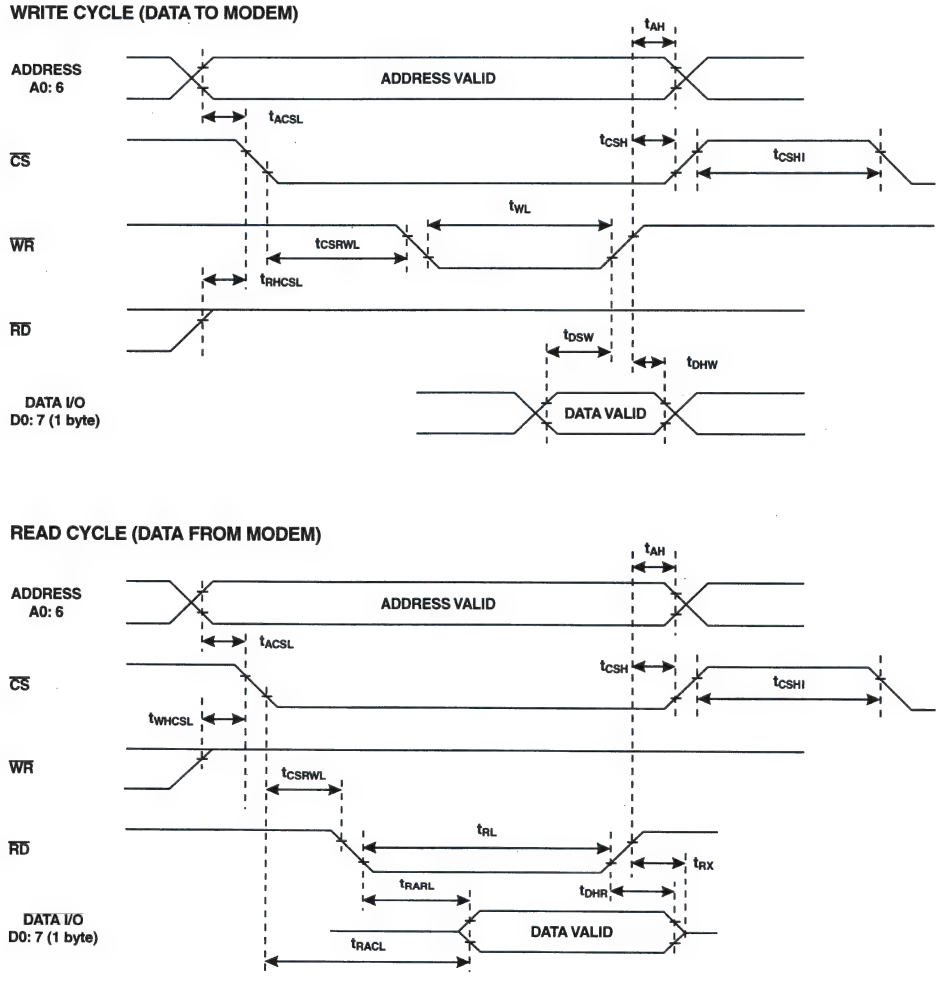
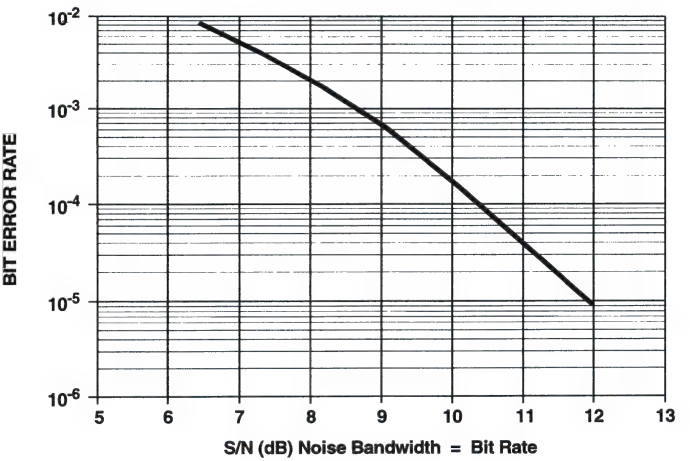


Figure 8: µP Interface Timings

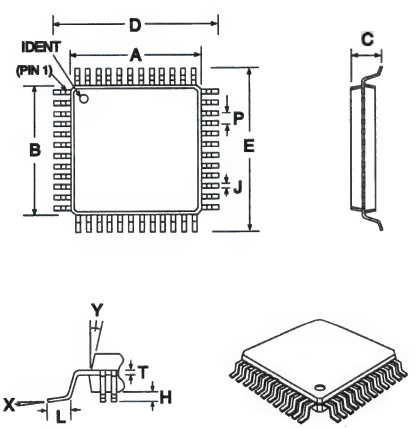
© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



Note: This graph does not include the improvement in error rate that is achievable if error correction is included in the user's application software.

Figure 9: Typical Raw Bit Error Rate for Xtal frequency = 4.9152MHz, V_{DD} = 5.0V, T_{AMB} = 25°C

6.3 Packaging



DIM.	MIN.	TYP.	MAX.
A	0.272 (6.90)		0.280 (7.10)
B	0.272 (6.90)		0.280 (7.10)
C			0.063 (1.60)
D	0.344 (8.75)		0.364 (9.25)
E	0.344 (8.75)		0.364 (9.25)
H	0.002 (0.05)		0.006 (0.15)
J	0.004 (0.11)		0.011 (0.27)
L	0.014 (0.35)		0.026 (0.66)
P		0.020 (0.50)	
T		0.005 (0.13)	
X	0°		7°
Y	11°		13°

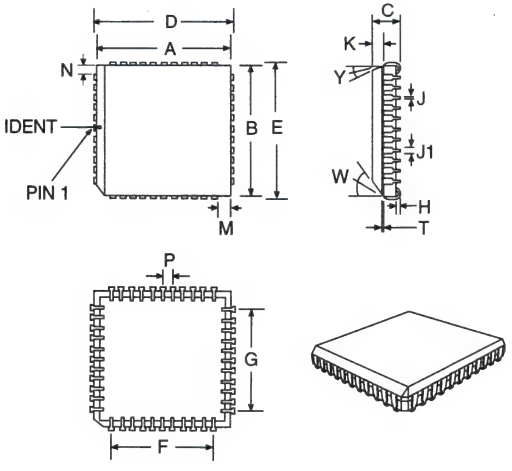
NOTE : All dimensions in inches (mm.)

Angles in degrees

Lead coplanarity to be 0 to 0.003 (0.08) Max

Figure 10: 48-pin TQFP Mechanical Outline: *Order as part no. MX949TG*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

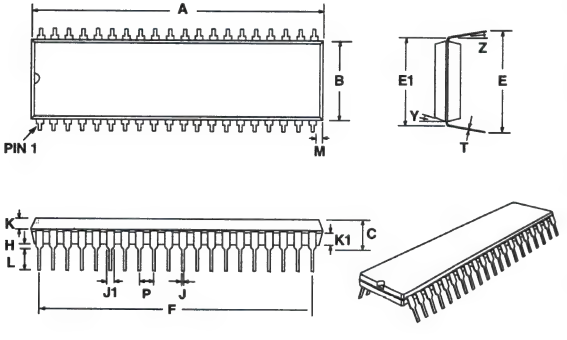


DIM.	MIN.	TYP.	MAX.
A	0.650 (16.51)		0.656 (16.66)
B	0.650 (16.51)		0.656 (16.66)
C			0.180 (4.57)
D	0.685 (17.40)		0.695 (17.65)
E	0.685 (17.40)		0.695 (17.65)
F		0.500 (12.7)	
G		0.500 (12.7)	
H	0.020 (0.51)		
J	0.013 (0.33)		0.021 (0.53)
J1		0.029 (0.74)	
K		0.070 (1.78)	
M		0.062 (1.57)	
N		0.062 (1.57)	
P		0.050 (1.27)	
T		0.010 (0.25)	
W		0.30 (7.62) x 45°	
Y		7°	

NOTE : All dimensions in inches (mm.)

Angles in degrees

Figure 11: 44-pin PLCC Mechanical Outline: *Order as part no. MX949LH*



DIM.	MIN.	TYP.	MAX.
A	2.040 (51.82)		2.060 (52.32)
B	0.532 (13.51)		0.552 (14.02)
C	0.151 (3.84)		0.195 (4.95)
E	0.600 (15.24)		0.670 (17.02)
E1	0.595 (15.11)		0.625 (15.88)
F		1.90 (48.26)	
H	0.015 (0.38)		0.045 (1.14)
J		0.018 (0.46)	
J1		0.060 (1.52)	
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.150 (3.81)
M		0.070 (1.79)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		3°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 12: 40-pin Plastic DIP Mechanical Outline: *Order as part no. MX949P*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480126.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Technical Specifications

Section 2: Telephony IC's

Device	Description	Page
MX602	Calling Line Identifier/Calling Line Identifier on Call Waiting	3
MX604	v.23 Compatible Modem	29
MX613	Global Call Progress Tone Detector	47
MX614	Bell 202 Compatible Modem	57
MX623	Line-Powered Call Progress Tone Detector	75
MX631	Low Voltage Subscriber Pulse Metering (SPM) Detector	81
MX633	Call Progress Tone Detector	89
MX641	Dual Subscriber Pulse Metering (SPM) Detector	101
MX643	Call Progress Tone Detector with Special Information Tones	117
MX651	Telephone Subscriber Pulse Metering (SPM) Detector and Anti-Fraud Processor	129
MX663	Call Progress Decoder	143

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX602

Calling Line Identifier /
Calling Line Identifier on Call Waiting

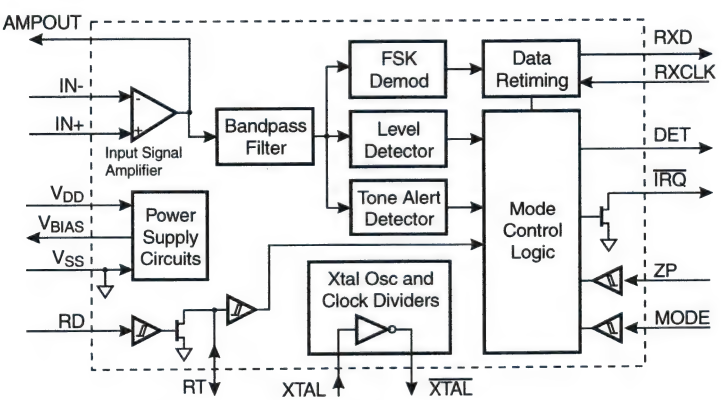
PRELIMINARY INFORMATION

Features

- **'Zero-Power' Ring or Line Polarity Reversal Detector**
- **V23/Bell202 FSK Demodulator with Data Retiming facility**
- **Dual-Tone Alert Detector**
- **µC Interrupt / Wake-up output to minimize system operating power**
- **Low Power Operation 0.5mA/1.0mA at 3.3V/5.5V$_{DD}$**
- **1µA max. 'Zero-Power' current**

Applications

- **Caller ID**
- **Caller ID on Call Waiting (Telephones and Adjunct Boxes)**



The MX602 is a low power CMOS device used for the reception of physical layer signals in Bellcore's Calling Identity Delivery (CID) and Calling Identity on Call Waiting (CIDCW) systems, British Telecom Calling Line Identification Service (CLIP), the Cable Communications Association's Caller Display Services (CDS), and similar evolving services.

The device includes a 'zero-power' ring or line polarity reversal detector, a dual-tone (2130Hz plus 2750Hz) Tone Alert Signal detector and a 1200-baud FSK V23/Bell202 compatible asynchronous data demodulator with a data retiming circuit which removes the need for a UART in the associated µC.

It is suitable for 'on-hook' use in systems using Bellcore specifications TR-NWT-000030 and SR-TSV-002476, British Telecom specifications SIN227 and SIN242, CCA TW/P&E/312, ETSI ETS 300 659-1 and ETS 300 659-2 and Mercury Communications MNR 19. It is also suitable for 'off-hook' use in some of those systems.

The MX602 may be used with a 3.0V to 5.0V supply and is available in the following packages: 16-pin SOIC (MX602DW) and a 16-pin PDIP (MX602P).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

CONTENTS

Section **Page**

1. Block Diagram **2-5**

2. Signal List **2-6**

3. External Components **2-7**

4. General Description **2-8**

4.1 Mode Control Logic 2-8
4.2 Input Signal Amplifier 2-8
4.3 Bandpass Filter 2-9
4.4 Level Detector 2-9
4.5 FSK Demodulator 2-10
4.6 FSK Data Retiming 2-10
4.7 Tone Alert Detector 2-11
4.8 Ring or Line Polarity Reversal Detector 2-12
4.9 Xtal Osc and Clock Dividers 2-13

5. Application Notes **2-14**

5.1 Typical Caller Identity Delivery (Caller ID) System Signals 2-14
5.2 MX602 CIDCW (Calling Line Identity on Call Waiting) Operation 2-15
5.2.1 Introduction 2-15
5.2.2 Overview 2-16
5.2.3 Detailed Procedure for CIDCW Transaction Initiation Detection 2-18
5.2.4 Block Diagrams of Adjunct Box and Telephone Set Interface 2-19
5.2.5 Timing Diagrams 2-20

6. Performance Specification **2-24**

6.1 Electrical Performance 2-24
6.2 Packaging 2-28

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1. Block Diagram

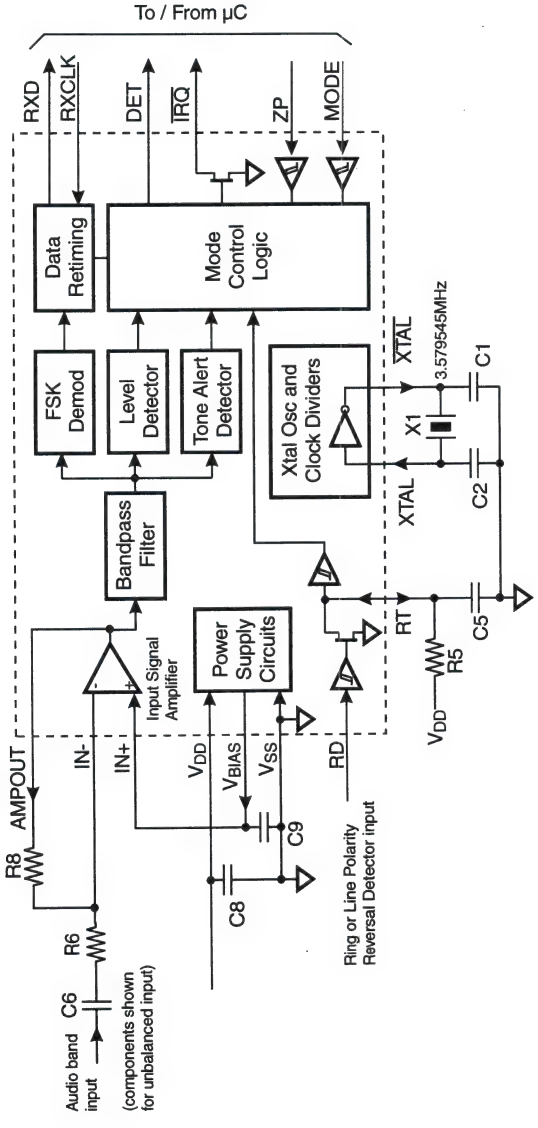


Figure 1: Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

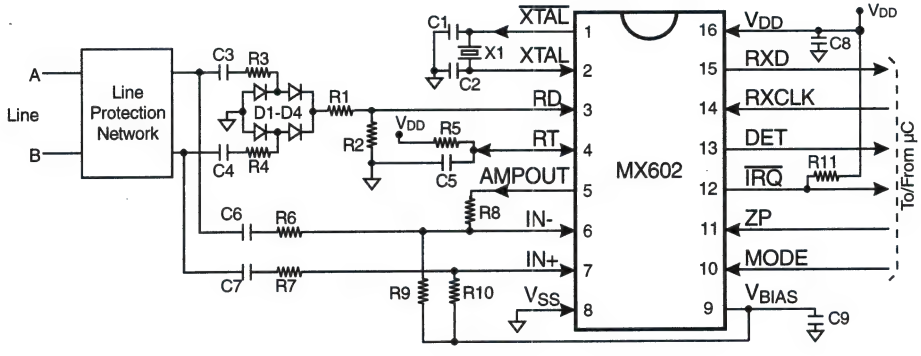
2. Signal List

Pin No.	Signal	Type	Description
1	$\overline{XTAL}$	output	Output of the on-chip Xtal oscillator inverter
2	XTAL	input	Input to the on-chip Xtal oscillator inverter
3	RD	input (S)	Input to the Ring or Line Polarity Reversal Detector
4	RT	input / output	Open-drain output and Schmitt trigger input forming part of the Ring or Line Polarity Reversal detector. An external resistor to V_{DD} and a capacitor to V_{SS} should be connected to RT to filter and extend the RD input signal
5	AMPOUT	output	Output of the on-chip Input Signal Amplifier
6	IN -	input	Inverting input to the on-chip Input Signal Amplifier
7	IN +	input	Non-inverting input to the on-chip Input Signal Amplifier
8	V_{SS}	power	Negative supply
9	V_{BIAS}	output	Internally generated bias voltage, held at $V_{DD}/2$ when the device is not in 'Zero-Power' mode. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
10	MODE	input (S)	Input used to select the operating mode.
11	ZP	input (S)	High level on this input selects 'Zero-Power' mode.
12	$\overline{IRQ}$	output	Open-drain output (active low) that may be used as an Interrupt Request / Wake-up input to the associated µC. An external pull-up resistor should be connected between this output and V_{DD}.
13	DET	output	Logic level output driven by the Ring or Line Polarity Reversal Detector, the Tone Alert Detector or the FSK Level detect circuits, depending on the operating mode.
14	RXCLK	input	Logic level input which may be used to clock received data bits out of the FSK Data Retiming block
15	RXD	output	Logic level output carrying either the raw output of the FSK Demodulator or re-timed 8-bit characters depending on the state of the RXCLK input
16	V_{DD}	power	Positive supply. Levels and thresholds within the device are proportional to this voltage. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

Notes: input (S) = Schmitt trigger input

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components



R1		470kΩ	±1%
R2	Note 1		±1%
R3, R4 R5, R6 R7		470kΩ	±1%
R8	Note 2, 3	470kΩ @ 3.3V 680kΩ @ 5.0V	±1%
R9	Note 2	240kΩ@ 3.3V 200kΩ@ 5.0V	±1%
R10		160kΩ	±1%

R11		100kΩ	±20%
C1, C2		18pF	±20%
C3, C4		0.1µF	±20%
C5		0.33µF	±20%
C6, C7		680pF	±20%
C8,C9		0.1µF	±20%
X1	Note 4	3.579545MHz	±0.1%
D1 - D4		1N4004	

Figure 2 : Recommended External Components for Dual Bellcore and British Telecom Application

Recommended External Component Notes:

1. See section 4.8
2. See section 4.2
3. The recommended values of R8 were selected for applications in both Bellcore and British Telecom Systems. Optimum Bellcore-only operation may be achieved by reducing the value of R8 e.g. to 656kΩ @ 5.0V.
4. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4. General Description

4.1 Mode Control Logic

The MX602's operating mode and the source of the DET and $\overline{IRQ}$ outputs are determined by the logic levels applied to the MODE and ZP input pins;

ZP	MODE	Mode	DET output from	$\overline{IRQ}$ output from
0	0	Tone Alert Detect	Tone Alert Signal Detection	End of Tone Alert Signal Ring or Line Polarity Reversal Detector
0	1	FSK Receive	FSK Level Detector	FSK Data Retiming (if enabled) and Ring or Line Polarity Reversal Detector
1	0	Zero-Power	Ring or Line Polarity Reversal Detector	Ring or Line Polarity Reversal Detector
1	1	Zero-Power	Ring or Line Polarity Reversal Detector	None

In the 'Zero-Power' modes, power is removed from all of the internal circuitry except for the Ring or Line Polarity Reversal Detector and the DET and $\overline{IRQ}$ outputs.

4.2 Input Signal Amplifier

This amplifier is used to convert the balanced FSK and Tone Alert signals received over the telephone line to an unbalanced signal of the correct amplitude for the FSK receiver and Tone Alert Detector circuits.

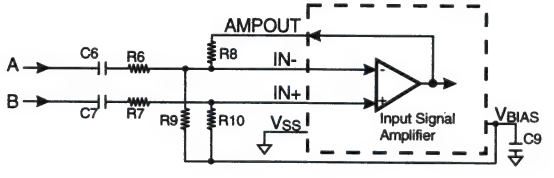


Figure 3: Input Signal Amplifier, balanced input configuration

The design equations for this circuit are:

$$\text{Differential Voltage Gain } \frac{V_{AMPOUT}}{V_{(B-A)}} = \frac{R8}{R6} \qquad R9 = \frac{R8 \times R10}{(R8 - R10)}$$

$$R6 = R7 = 470k\Omega \qquad R10 = 160k\Omega$$

The target differential voltage gain depends on the expected signal levels between the A and B wires and the MX602's internal overload and threshold levels, which are proportional to the supply voltage.

The MX602 has been designed to meet the related specifications when R8 = 470kΩ at V_{DD} = 3.3V nominal, rising to 680kΩ at V_{DD} = 5.0V (see note) and R9 = 240kΩ at V_{DD} = 3.3V dropping to 200kΩ at V_{DD} = 5.0V as shown in section 4.2 Figure 5

Notes:

1. The recommended values of R8 were selected for applications in both Bellcore and British Telecom Systems. Optimum Bellcore-only operation may be achieved by reducing the value of R8 e.g. to 656kΩ @ 5.0V.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

The Input Signal Amplifier may also be used, with different external components, to allow the MX602 to operate from an unbalanced signal source as shown in Figure 4. In this unbalanced signal configuration, the values of R6 and R8 are the same as used for the balanced input configuration @ 3.3V nominal.

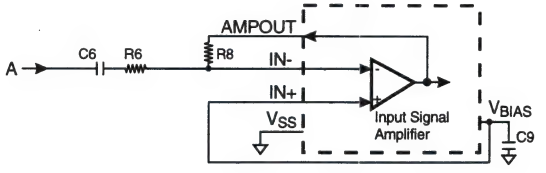


Figure 4: Input Signal Amplifier, unbalanced input configuration

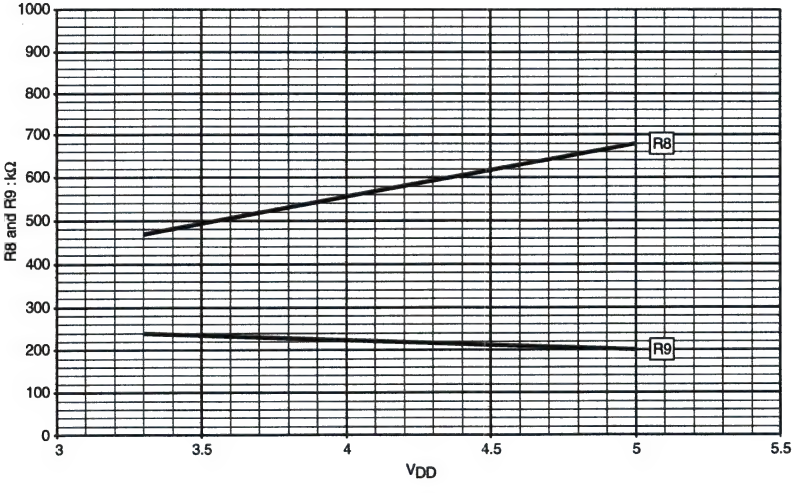


Figure 5: Input Signal Amplifier, optimum values of R8 and R9 vs. V_{DD}

4.3 Bandpass Filter

Is used to attenuate out of band noise and interfering signals from reaching the FSK Demodulator, Tone Alert Detector and Level Detector circuits. The characteristics of this filter, differs between FSK and Tone Alert modes. Switched Capacitor filter stages clocked at 57.7kHz provide primary filtering. If the input signal is band limited to 28.85kHz then no anti-aliasing filtering is required.

4.4 Level Detector

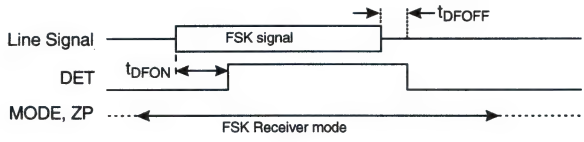
This block operates by measuring the level of the signal at the output of the Bandpass Filter. It then compares it against a threshold which depends on whether FSK Receive or Tone Alert Detect mode has been selected.

In Tone Alert Detect mode the output of the Level Detector block provides an input to the Tone Alert Signal Detector.

In FSK Receive mode the MX602 DET output will be set high when the level has exceeded the threshold for a sufficient duration. Amplitude and time hysteresis are used to reduce chattering of the DET output in marginal conditions.

Note: In FSK Receive mode, this circuit may also respond to non-FSK signals such as speech.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



See section 6.1 for definitions of t_{DFON} and t_{DFOFF}

Figure 6: FSK Level Detector operation

4.5 FSK Demodulator

This block converts the 1200 baud FSK input signal to a digital data stream which is output via the RXD pin as long as the Data Retiming function is not enabled (see section 4.6). This output does not depend on the state of the FSK Level Detector output.

Note: In the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data.

4.6 FSK Data Retiming

The Data Retiming block extracts the 8 data bits of each character from the received asynchronous data stream, and presents them to the µC under the control of strobe pulses applied to the RXCLK input. The timing of these pulses is not critical and they may easily be generated by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

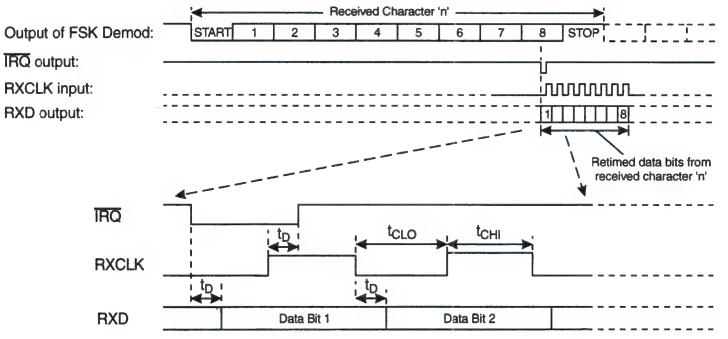
The block operates on a character by character basis by first looking for the mark to space transition which signals the beginning of the start bit. Using this transition as a timing reference, the block samples the output of the FSK Demodulator in the middle of each of the following 8 received data bits, and stores the results in an internal 8-bit shift register.

When the eighth data bit has been clocked into the internal shift register, the MX602 examines the RXCLK input. If this is low then the $\overline{IRQ}$ output will be pulled low and the first of the stored data bits put onto the RXD output pin. On detecting that the $\overline{IRQ}$ output has gone low, the µC should pulse the RXCLK pin high 8 times. The high to low transition at the end of the first 7 of these pulses will be used by the MX602 to shift the next data bit from the shift register onto the RXD output. At the end of the eighth pulse the FSK Demodulator output will be reconnected to the RXD output pin. The $\overline{IRQ}$ output will be cleared the first time the RXCLK input goes high.

Thus to use the Data Retiming function, the RXCLK input should be kept low until the $\overline{IRQ}$ output goes low; if the Data Retiming function is not required the RXCLK input should be kept high.

The only restrictions on the timing of the RXCLK waveform are those shown in Figure 7 and the need to complete the transfer of all eight bits into the µC within 8.3mSec (the time of a complete character at 1200 baud).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



t_D = Internal MX602 delay (max 1µS); t_{CLO} = RXCLK low time (min 1µS); t_{CHI} = RXCLK high time (min 1µS)

Figure 7: FSK Operation with Data Retiming

Note: If enabled, the Data Retiming block will interpret the FSK Channel Seizure signal (a sequence of alternating mark and space bits) as valid received characters, with values of 55 (hex). Similarly it may interpret speech or other signals as random characters. If the Data Retiming facility is not required, the RXCLK input to the MX602 should be kept high. The asynchronous data from the FSK Demodulator will then be connected directly to the RXD output pin, and the IRQ output will not be activated by the FSK signal. This case is illustrated in Figure 8.

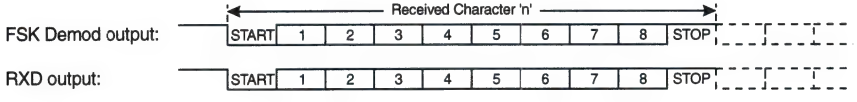
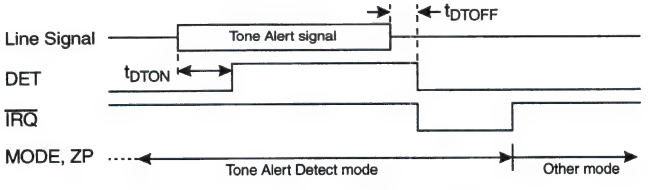


Figure 8: FSK Operation without Data Retiming (RXCLK always high)

4.7 Tone Alert Detector

This block is enabled when the MX602 is set to Tone Alert Detector operating mode. It then monitors the received signal for the presence of simultaneous 2130Hz and 2750Hz tones of sufficient level and duration.

The MX602 DET output will be set high while a valid Tone Alert signal is detected. At the end of the Tone Alert signal the DET output will go low and the IRQ output will be pulled low until the MX602 is switched out of Tone Alert Detector mode.



See section 6.1 for definitions of t_{DTON} and t_{DTOFF}

Figure 9: Tone Alert Detector Operation

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.8 Ring or Line Polarity Reversal Detector

These circuits are used to detect the Line Polarity Reversal and Ringing signals associated with the Calling Line Identification protocol. Figure 10 illustrates their use in a typical application.

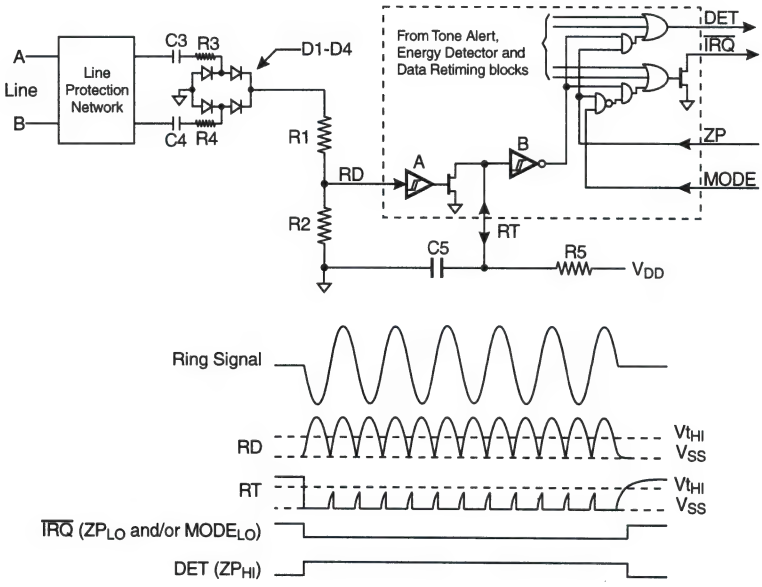


Figure 10: Ring or Line Polarity Reversal Operation

When no signal is present on the telephone line, RD will be at V_{SS} and RT pulled to V_{DD} by R5 so the output of the Schmitt trigger 'B' will be low.

The ring signal is usually applied at the subscriber's exchange as an ac voltage inserted in series with one of the telephone wires and will pass through either C3 and R3 or C4 and R4 to appear at the top end of R1 (point X in Figure 10) in a rectified and attenuated form.

When the amplitude of the signal appearing at RD is greater than the input threshold (Vt_{HI}) of Schmitt trigger 'A' then the N transistor connected to RT will be turned on, pulling the voltage at RT to V_{SS} by discharging the external capacitor C5.

The output of the Schmitt trigger 'B' will then go high, activating the DET and/or $\overline{IRQ}$ outputs depending on the states of the MODE and ZP inputs.

The minimum amplitude ringing signal that is certain to be detected is :

$$\left(0.7 + Vt_{HI}\frac{(R1+R2+R3)}{R2}\right)(0.707V_{RMS})$$

Where Vt_{HI} is the high-going threshold voltage of the Schmitt trigger A (see section 6.1).

With R1, R3 and R4 all 470kΩ as indicated in Figure 2, then setting R2 to 68kΩ will guarantee detection of ringing signals of $40V_{RMS}$ and above, for V_{DD}, over the range 3.0 to 5.5V.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

A line polarity reversal may be detected using the same circuit but there will be only one pulse at RD. The British Telecom specification SIN242 says that the circuit must detect a +15V to -15V reversal between the two lines slewing in 30msec. For a linearly changing voltage at the input to C3 (or C4), then the voltage appearing at the RD pin will be

$$\frac{dV}{dt}C3\left(1-e^{-\frac{t}{T}}\right)R2 \text{ where } T = C3(R1+R2+R3) \text{ and } \frac{dV}{dt} \text{ is the input slew rate.}$$

For dV/dt = 500V/sec (15V in 30msec), R1, R3 and R4 all 470kΩ and C3, C4 both 0.1µF as indicated in Figure 2, then setting R2 to 390kΩ will guarantee detection at V_{DD} = 5.5V.

If the time constant of R5 and C5 is large enough then the voltage on RT will remain below the threshold of the 'B' Schmitt trigger keeping the DET and/or $\overline{IRQ}$ outputs active for the duration of a ring cycle

The time for the voltage on RT to charge from V_{SS} towards V_{DD} can be derived from the formula

$$V_{RT} = V_{DD}\left(1-e^{-\frac{t}{R5C5}}\right)$$

As the Schmitt trigger high-going input threshold voltage (Vt_{HI}) has a minimum value of 0.56 x V_{DD} , then the Schmitt trigger B output will remain high for a time of at least 0.821 x R5 x C5 following a pulse at RD.

Using the values given in Figure 2(470kΩ and 0.33µF) gives a minimum time of 100 msec (independent of V_{DD}), which is adequate for ring frequencies of 10Hz or above.

If necessary, the µC can distinguish between a ring and a reversal by timing the length of the $\overline{IRQ}$ or DET output.

4.9 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the MX602 is determined by a 3.579545MHz clock present at the XTAL pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or may be supplied from an external source to the XTAL input, in which case C1, C2 and X1 should not be fitted.

The oscillator is turned off in the 'Zero-Power' modes.

If the clock is provided by an external source which is not always running, then the ZP input must be set high when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by MX602 as well as generating undefined states of the RXD, DET and $\overline{IRQ}$ outputs.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. Application Notes

5.1 Typical Caller Identity Delivery (Caller ID) System Signals

Figure 11, Figure 12, and Figure 13 illustrate the line signaling and MX602 input and output signals for typical Bellcore and British Telecom system use.

The Data Retiming function is not used in these examples (RXCLK kept high).

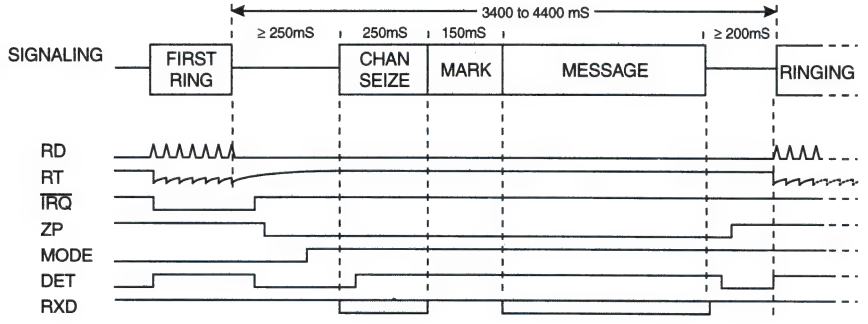


Figure 11: Bellcore System Signals

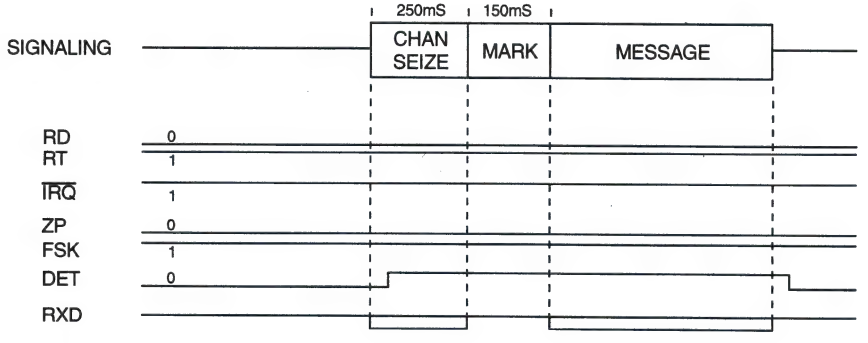
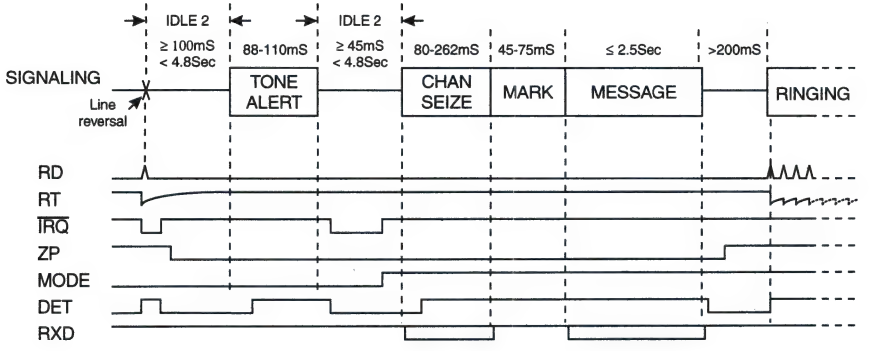


Figure 12: Bellcore System Signals (without ring)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

The British Telecom Tone Alert signal consists of simultaneous 2130Hz and 2750Hz tones. The 'Chan Seize' signal consists of a '1010..' FSK bit sequence in all cases.



Note: IDLE 1 + IDLE 2 ≤ 5 sec

Figure 13: British Telecom System Signals

5.2 MX602 CIDCW (Calling Line Identity on Call Waiting) Operation

5.2.1 Introduction

CIDCW is a telephone service which identifies a waiting caller without interrupting your current call. It eliminates the 'blind spot' in traditional Call Waiting by giving a telephone user the informed choice of whether or not to take the incoming call.

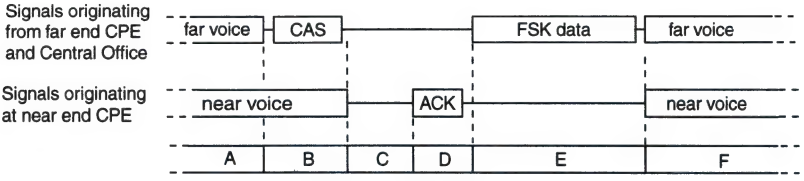
To support CIDCW, the circuits of Caller ID compatible telephone equipment and adjunct 'boxes' must detect a subtle CPE Alert Signal (CAS), a dual tone injected into phone conversations. The CAS is transmitted by the central office to initiate a CIDCW transaction consisting of an 80ms burst of simultaneous 2130Hz and 2750Hz tones. CAS detection accuracy is very important because both missed and false signal detection is evident and annoying to telephone users. Missed signal detection causes Caller ID information to be lost. False signal detection produces a disruptive tone which is heard by the far end caller. Because the tone signals must be detected in the presence of conversations which both mask and masquerade as the tone signals, this function is very difficult to accurately achieve.

This application note describes the use of the MX602 for CIDCW CAS detection. The MX602's 1µA ring detect supply current, 3.3 to 5.5 volt supply range, and 16 pin package offer significant advantages in battery life and final product size.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.2.2 Overview

A successful CIDCW transaction as described by Bellcore SR-TSV-002476, consists of a sequence of actions between the CPE (Customer Premises Equipment - e.g. a telephone) and the Central Office as indicated in Figure 14.



A. Normal conversation with both near and far voice present.
B. Central Office mutes far end voice, emits CAS and becomes silent
C. CPE recognizes CIDCW initiation and mutes near end voice and keypad
D. CPE emits DTMF ACK to Central Office to signal its readiness to receive Caller ID data stream
E. Central Office recognizes ACK and emits FSK Data stream of Caller ID data which is received and decoded by CPE
F. CIDCW transaction is complete. CPE unmutes near end voice and Central Office unmutes far end voice returning to normal conversation with both near and far voice present.

Figure 14, CIDCW Transaction From Near End CPE Perspective

From the near end CPE's perspective, the initiation of a CIDCW transaction is characterized by two events occurring in sequence: (1) a CAS dual tone is received, and (2) a subsequent quiet period passes as far end speech continues to be muted. These two events can be detected by the MX602's Dual Tone Alert detector and FSK level detector, respectively.

Caller ID and CIDCW end products typically use a microcontroller to manage the transfer and display of Caller ID data. The same microcontroller is easily used to observe and control the MX602 CIDCW transaction initiation detection process. It measures an MX602 DET output pulse duration, mutes near end voice, subsequently watches for DET output activity, and controls whether the MX602 is in Dual Tone Alert or FSK Receive modes as shown in Figure 15.

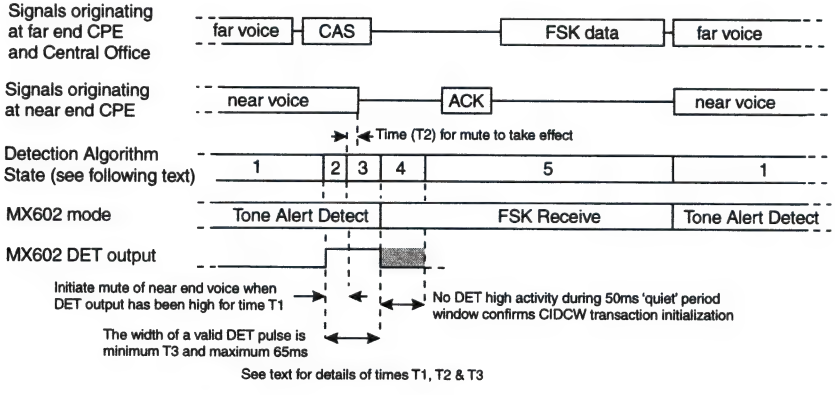

Signals originating at far end CPE and Central Office
far voice
CAS
FSK data
far voice
Signals originating at near end CPE
near voice
ACK
near voice
Time (T2) for mute to take effect
Detection Algorithm State (see following text)
1
2
3
4
5
1
MX602 mode
Tone Alert Detect
FSK Receive
Tone Alert Detect
MX602 DET output
Initiate mute of near end voice when DET output has been high for time T1
No DET high activity during 50ms 'quiet' period window confirms CIDCW transaction initialization
The width of a valid DET pulse is minimum T3 and maximum 65ms
See text for details of times T1, T2 & T3

Figure 15, CIDCW Transaction Initiation with MX602 Operation

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Different strategies may be used for CIDCW transaction initiation detection. The simplest strategy detects only the CAS dual tone. More complex strategies may detect both the CAS dual tone as well as the following far end voice quiet period if near end voice is muted. The choice of a specific strategy involves several tradeoffs which must be considered by the end product designer.

As previously described, the MX602 dual tone detector and FSK energy level detector functions provide the tools to implement a range of strategies. It is important to note that CIDCW transaction detection performance is influenced by factors which are external to the MX602 and under the control of its surrounding circuit. Such factors may include: (1) Input signal levels provided to the MX602, (2) The functional 'cost' associated with missed and false CIDCW transaction detections, (3) Pulse width measurement accuracy, and (4) Noise or other disturbances introduced by muting or other external circuits. The remainder of this section provides examples to assist end product designers develop their specific designs.

CIDCW Transaction Initiation Detection Algorithm

The following State Transition Diagram Figure 16 and following text provide a detailed description of the CIDCW detection procedure as shown in Figure 15.

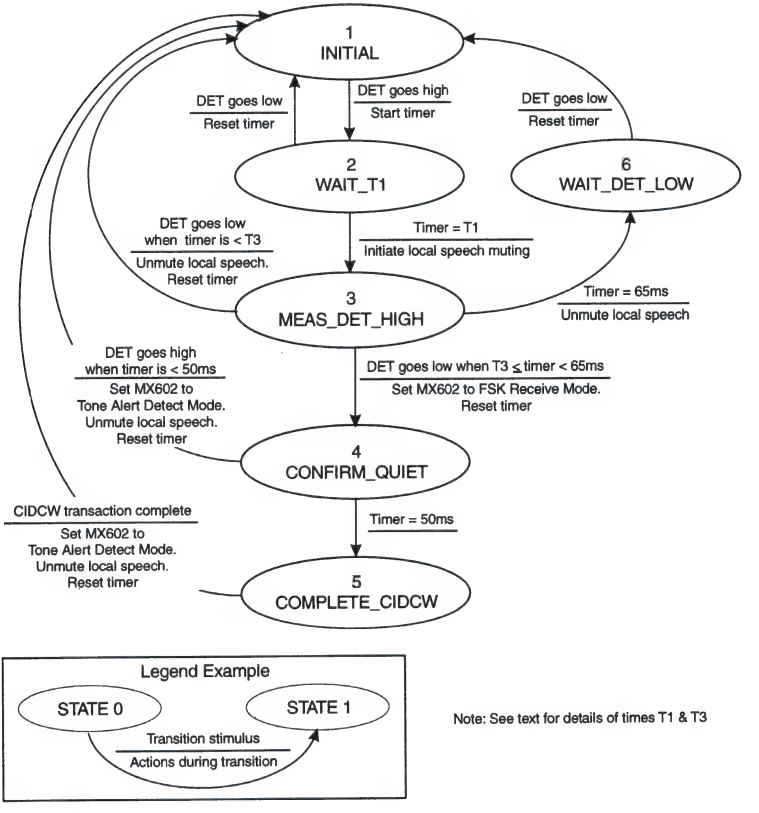


Figure 16, CIDCW State Flow Diagram

5.2.3 Detailed Procedure for CIDCW Transaction Initiation Detection

1. INITIAL state
The MX602 is in the Tone Alert Detect mode. On the rising edge of the DET line, start the timer, and transition to the WAIT_T1 state.

2. WAIT_T1 state
During this state, the DET output high time is measured so that pulses lasting less than T1 may be ignored.
WHILE Timer < T1
    IF DET goes low
        Reset the timer.
        Transition to the INITIAL state.
Initiate local speech muting.
Transition to MEAS_DET_HIGH state.

3. MEAS_DET_HIGH state
WHILE Timer < 65ms
    IF DET goes low
        IF Timer < T3
            Unmute local speech.
            Reset the timer.
            Transition to the INITIAL state.
        ELSE
            Set MX602 to FSK Receive Mode.
            Reset the timer.
            Transition to the CONFIRM_QUIET state.
Unmute local speech.
Transition to the WAIT_DET_LOW state.

4. CONFIRM_QUIET state
WHILE Timer < 50ms
    IF DET goes high
        Set MX602 to Tone Alert Detect Mode.
        Unmute local speech.
        Reset the timer.
        Transition to the INITIAL state.
Transition to the COMPLETE_CIDCW state.

5. COMPLETE_CIDCW state
This state handles the remaining CIDCW transaction functions e.g. determine that no near end extensions are off hook, emit a CPE ACK to Central Office via a DTMF D tone signal, receive the FSK Caller ID data stream, etc.
WHEN CIDCW transaction is complete
    Set the MX602 to Tone Alert Detect Mode.
    Unmute local speech.
    Reset the timer.
    Transition to the INITIAL state.

6. WAIT_DET_LOW state
WHEN DET goes low
    Reset the timer
    Transition to the INITIAL state.

Times T1, T2, & T3
The values given below have been selected to give an extremely low incidence of false CAS detections while maintaining a high probability of decoding correct CIDCW initiation signals by taking advantage of the specific profile of MX602's responses to typical speech and CAS signals. Two timing options are given, Telephone Set and Adjunct Box, the choice being determined principally by how easily local speech can be muted. The Adjunct Box option reduces the frequency of short speech mutes by a factor of about 5 at the expense of a small increase in the number of missed CAS signals when compared to the Telephone Set option.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Adjunct Box Timing

When the CIDCW circuits are housed in an adjunct box so that muting is only possible by interrupting the 2-wire connection to the telephone set, then it is recommended that:

T1 should be 15ms i.e. speech muting should only be initiated after the DET output has been high for 15ms.

T2, the time for speech muting to take effect, should be as short as possible and in any case not more than 5ms.

T3, the minimum length of a valid DET output high time, should be equal to T1 plus T2 plus 10ms, i.e. between 25 and 30ms.

Telephone Set Timing

When the CIDCW circuits are built into the telephone set so that locally generated speech can be muted quickly and without injecting noise then it is recommended that:

T1 should be zero, i.e. muting should be initiated as soon as the MX602 DET output goes high.

T2, the time for local speech muting to take effect, should be as short as possible and in any case not more than 5ms.

T3, the minimum length of a valid DET output high time, should be 15ms.

Notes:

1. The T1, T2, and T3 time values are intended to provide guidance, however, different times may be required for optimal operation in specific end product designs.
2. For optimum performance, the system transition times from tone detect to muting and tone detect de-response to FSK mode should be minimized. Tests have been performed with sub-millisecond response times but longer times may be used with some degradation in performance.
3. The 50ms monitoring period of the CONFIRM_QUIET state, when added to the 0.5 to 10ms de-response time of the MX602 in Tone Alert Detect and a nominal 0 to 5ms delay in changing from TONE mode to FSK mode, results in a valid CAS detection occurring at between 50 and 65ms after the end of the CAS. This leaves at least 35ms to mute the local handset fully, test for off-hook extensions, and initiate the DTMF ACK tone within the time permitted by CIDCW specifications.
4. During the CONFIRM_QUIET state, any high pulses on the DET output will last for at least 8ms (or until the mode is changed). This makes it simple to monitor and detect any DET high output pulses when in this state.
5. In adjunct box applications, it is important to avoid injecting noise to the MX602 input signal when performing near end voice muting because such noise could disrupt MX602 operation and reduce performance. Alternate approaches can be used which would delay such voice muting until after the CAS tone. One example would first qualify dual tone detector output pulses of 20ms to 65ms nominal duration as CAS tone indications and follow such pulses with near end voice muting and silence confirmation to further enhance performance.

5.2.4 Block Diagrams of Adjunct Box and Telephone Set Interfaces

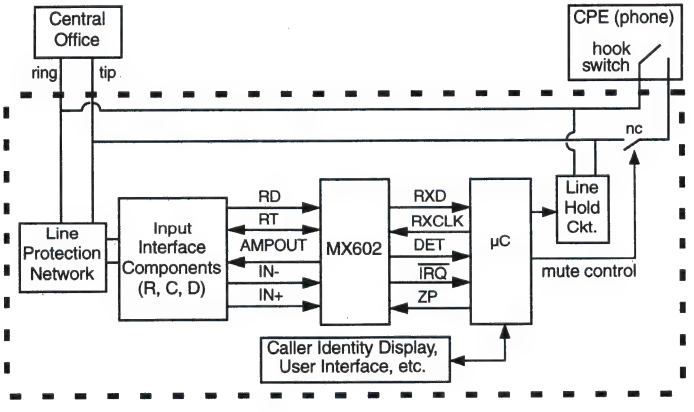


Figure 17: Adjunct Box Interface

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

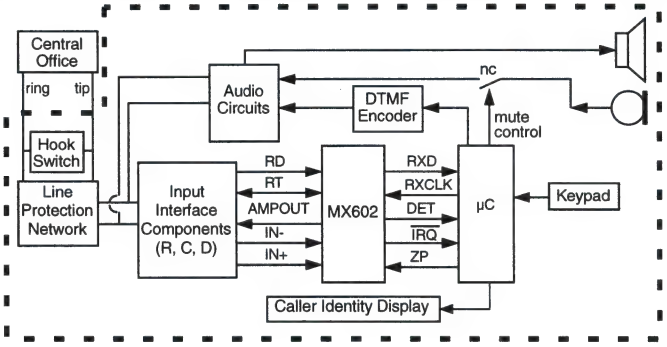
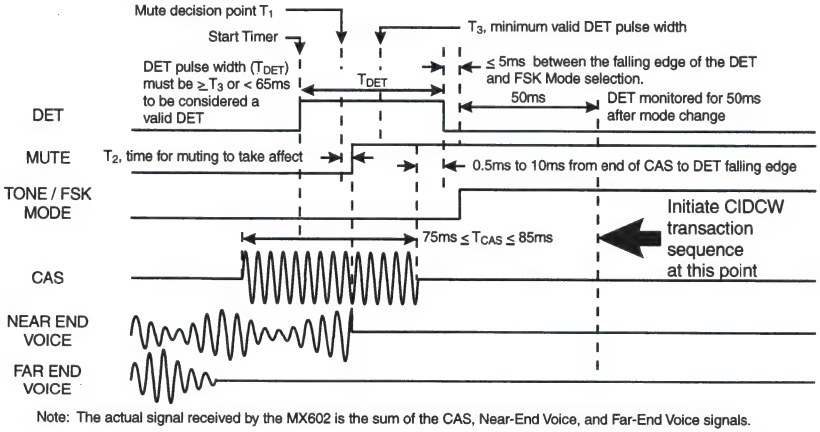


Figure 18: Telephone Set Interface

5.2.5 Timing Diagrams

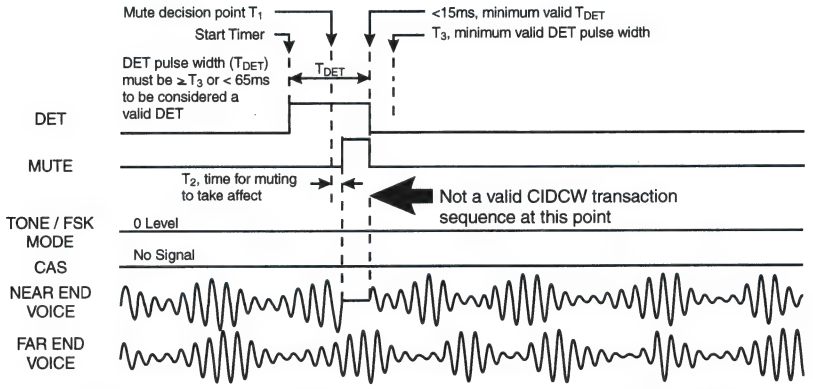
Figure 19, Figure 20, Figure 21, Figure 22, Figure 23, Figure 24, Figure 25, and Figure 26 are timing diagrams which illustrate the CIDCW transaction initiation sequence for various cases.


Mute decision point T1
Start Timer
T3, minimum valid DET pulse width
DET pulse width (TDET) must be ≥ T3 or < 65ms to be considered a valid DET
TDET
≤ 5ms between the falling edge of the DET and FSK Mode selection.
50ms
DET monitored for 50ms after mode change
DET
MUTE
T2, time for muting to take affect
0.5ms to 10ms from end of CAS to DET falling edge
TONE / FSK MODE
Initiate CIDCW transaction sequence at this point
75ms ≤ TCAS ≤ 85ms
CAS
NEAR END VOICE
FAR END VOICE

Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

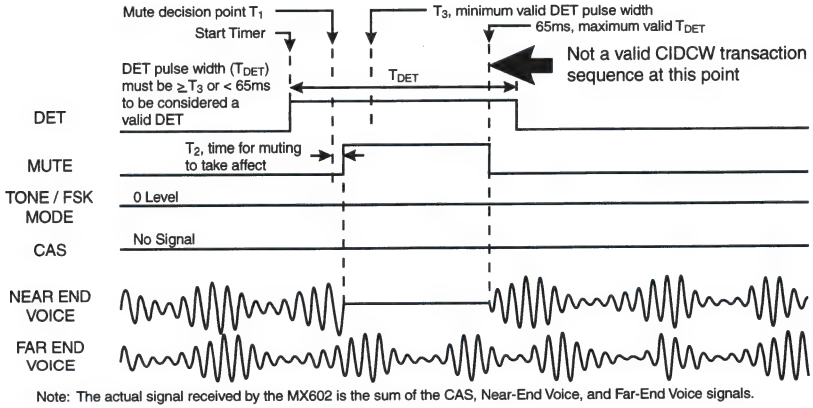
Figure 19, Valid CIDCW Transaction Initiation Adjunct Box Timing Sequence

© 1997 MX-COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.


Mute decision point T_1
Start Timer
<15ms, minimum valid T_{DET}
T_3, minimum valid DET pulse width
DET pulse width (T_{DET}) must be ≥ T_3 or < 65ms to be considered a valid DET
T_{DET}
DET
MUTE
T_2, time for muting to take affect
Not a valid CIDCW transaction sequence at this point
TONE / FSK MODE
0 Level
CAS
No Signal
NEAR END VOICE
FAR END VOICE

Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

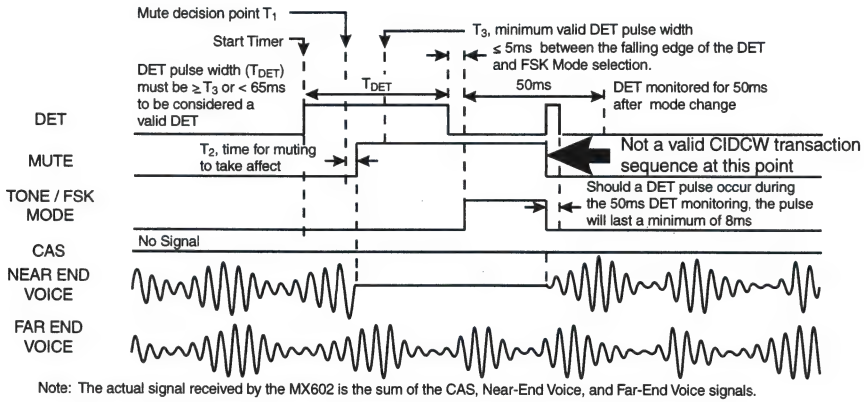
Figure 20, Invalid CIDCW Transaction Initiation Adjunct Box Timing Sequence (DET pulse < 15ms)


Mute decision point T_1
Start Timer
T_3, minimum valid DET pulse width
65ms, maximum valid T_{DET}
Not a valid CIDCW transaction sequence at this point
DET pulse width (T_{DET}) must be ≥ T_3 or < 65ms to be considered a valid DET
T_{DET}
DET
T_2, time for muting to take affect
MUTE
TONE / FSK MODE
0 Level
CAS
No Signal
NEAR END VOICE
FAR END VOICE

Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

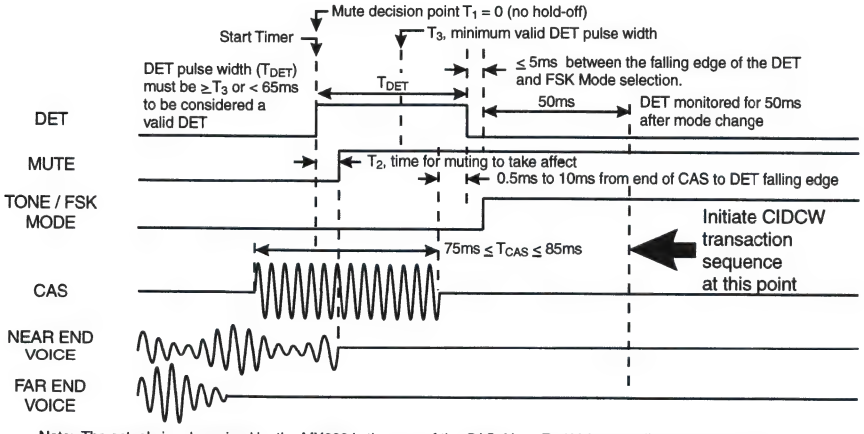
Figure 21, Invalid CIDCW Transaction Initiation Adjunct Box Timing Sequence (DET pulse ≥ 65ms)

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480136.003


Mute decision point T_1
Start Timer
T_3, minimum valid DET pulse width
≤ 5ms between the falling edge of the DET and FSK Mode selection.
DET pulse width (T_{DET}) must be ≥ T_3 or < 65ms to be considered a valid DET
T_{DET}
50ms
DET monitored for 50ms after mode change
DET
MUTE
T_2, time for muting to take affect
Not a valid CIDCW transaction sequence at this point
TONE / FSK MODE
Should a DET pulse occur during the 50ms DET monitoring, the pulse will last a minimum of 8ms
CAS
No Signal
NEAR END VOICE
FAR END VOICE

Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

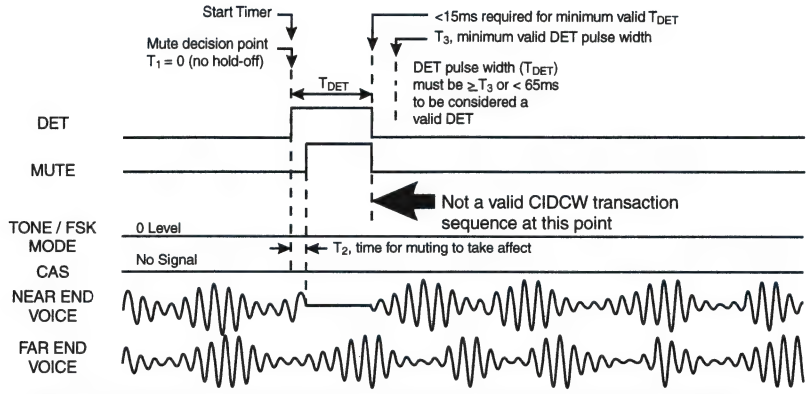
Figure 22, Invalid CIDCW Transaction Initiation Adjunct Box Timing Sequence (DET output goes high during 50ms quiet period)


Mute decision point T_1 = 0 (no hold-off)
Start Timer
T_3, minimum valid DET pulse width
DET pulse width (T_{DET}) must be ≥ T_3 or < 65ms to be considered a valid DET
T_{DET}
≤ 5ms between the falling edge of the DET and FSK Mode selection.
50ms
DET monitored for 50ms after mode change
DET
MUTE
T_2, time for muting to take affect
0.5ms to 10ms from end of CAS to DET falling edge
TONE / FSK MODE
Initiate CIDCW transaction sequence at this point
75ms ≤ T_{CAS} ≤ 85ms
CAS
NEAR END VOICE
FAR END VOICE

Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

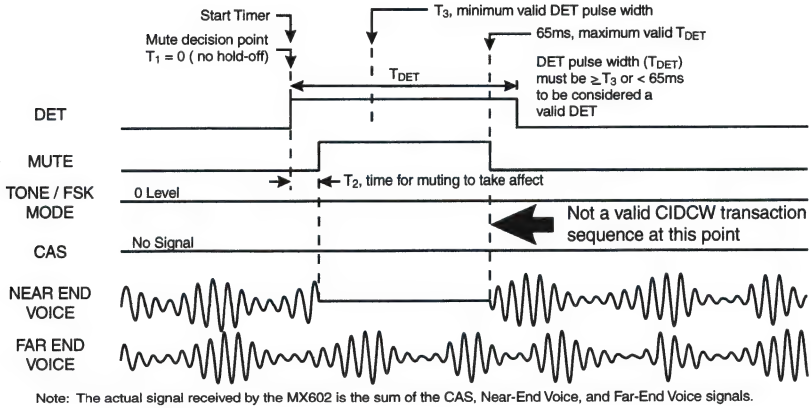
Figure 23: Valid CIDCW Transaction Initiation Telephone Set Timing Sequence

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

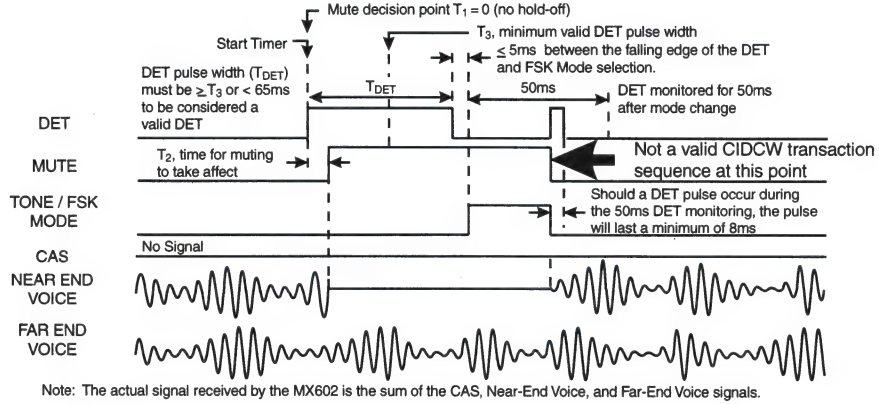
Figure 24: Invalid CIDCW Transaction Initiation Telephone Set Timing Sequence (DET pulse < 15ms)



Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

Figure 25: Invalid CIDCW Transaction Initiation Telephone Set Timing Sequence (DET pulse ≥ 65ms)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.


Mute decision point T_1 = 0 (no hold-off)
Start Timer
T_3, minimum valid DET pulse width
≤ 5ms between the falling edge of the DET and FSK Mode selection.
DET pulse width (T_{DET}) must be ≥ T_3 or < 65ms to be considered a valid DET
T_{DET}
50ms
DET monitored for 50ms after mode change
DET
MUTE
T_2, time for muting to take affect
Not a valid CIDCW transaction sequence at this point
TONE / FSK MODE
Should a DET pulse occur during the 50ms DET monitoring, the pulse will last a minimum of 8ms
CAS
No Signal
NEAR END VOICE
FAR END VOICE

Note: The actual signal received by the MX602 is the sum of the CAS, Near-End Voice, and Far-End Voice signals.

Figure 26: Invalid CIDCW Transaction Initiation Telephone Set Timing Sequence (DET output goes high during 50ms quiet period)

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - VSS)	-0.3	7.0	V
Voltage on any pin to VSS	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and VSS pins	-30	30	mA
Current into or out of any other pin	-20	20	mA
DW /DIP Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - VSS)		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal frequency	1	3.575965	3.583125	MHz

Operating Limits Notes:

1. A Xtal frequency of 3.579545MHz ±0.1% is required for correct Tone Alert and FSK detection.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.0V at T_{AMB} = 25°C and V_{DD} = 3.3V to 5.5V at T_{AMB} = - 40 to +85°C, V_{SS} = 0V
Xtal Frequency = 3.579545MHz ± 0.1%, 0dBV corresponds to 1.0V_{RMS}

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (ZP input high) at V_{DD} = 5.0V	1,2			1.0	µA
I_{DD} (ZP input low) at V_{DD} = 3.0V	1		0.5	1.0	mA
I_{DD} (ZP input low) at V_{DD} = 5.0V	1		1.0	2.0	mA
Logic 1 input level (RXCLK and XTAL inputs)		70%			V_{DD}
Logic 0 input level (RXCLK and XTAL inputs)				30%	V_{DD}
Logic input leakage current (V_{IN} = 0 to V_{DD}), XTAL input		-1.0		1.0	µA
Output logic 1 level (I_{OH} = 360µA)		V_{DD} - 0.4			V
Output logic 0 level (I_{OL} = 360µA)				0.4	V
$\overline{IRQ}$ output 'off' state current (V_{OUT} = V_{DD})				1.0	µA
Schmitt Trigger input thresholds (Figure 27)					
High going (Vt_{HI})		(0.56)(V_{DD})		(0.56)(V_{DD}) + 0.6	V
Low going (Vt_{LO})		(0.44)(V_{DD}) - 0.6		(0.44)(V_{DD})	V
Tone Alert Detector					
'Low' tone nominal frequency			2130		Hz
'High' tone nominal frequency			2750		Hz
Start of Tone Alert signal to DET high time (t_{DTON} Figure 9)			40		msec
End of Tone Alert signal to DET and $\overline{IRQ}$ low time (t_{DTOFF} Figure 9)		0.5		10.0	msec
To ensure detection:	3				
'Low' tone frequency tolerance				±20	Hz
'High' tone frequency tolerance				±30	Hz
Level (total)	4	-40.0		-2.2	dBV
2750Hz tone level with respect to 2130Hz tone level		-7.0		7.0	dB
Signal to Noise ratio	5	20.0			dB
Dual Tone Burst Duration		75			msec
To ensure non-detection:	6				
'Low' tone frequency tolerance		±75			Hz
'High' tone frequency tolerance		±95			Hz
Level (total)	4			-46.0	dBV
Dual Tone Burst Duration				25	msec
FSK Receiver					
Transmission rate		1188	1200	1212	Baud
V23 Mark (logic 1) frequency		1280	1300	1320	Hz
V23 Space (logic 0) frequency		2068	2100	2132	Hz
Bell202 Mark (logic 1) frequency		1188	1200	1212	Hz
Bell202 Space (logic 0) frequency		2178	2200	2222	Hz
Valid input level range	4	-40.0		-8.0	dBV

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

	Notes	Min.	Typ.	Max.	Units
Acceptable twist (mark level with respect to space level)					
V23s		-7.0		7.0	dB
Bell202		-10.0		10.0	dB
Acceptable Signal to Noise ratio					
V23	5	20.0			dB
Bell202	5	30.0			dB
Level Detector 'on' threshold level	4			-40.0	dBV
Level Detector 'off' to 'on' time (t_{FDON} Figure 6)				25.0	msec
Level Detector 'on' to 'off' time (t_{FDOFF} Figure 6)		8.0			msec
Input Signal Amplifier					
Input impedance	7	10.0			MΩ
Voltage gain			500		V/V
XTAL Input					
'High' pulse width	8	100			ns
'Low' pulse width	8	100			ns

Operating Characteristics Notes:

1. At 25°C, not including any current drawn from the MX602 pins by external circuitry other than X1, C1 and C2.
2. RD, MODE, RXCLK inputs at V_{SS}, ZP input at V_{DD}. See Figure 28
3. All conditions must be met to ensure detection.
4. For V_{DD} = 5.0V with equal level tones and with the input signal amplifier external components as section 3. The internal threshold levels are proportional to V_{DD}. For other supply voltages or different signal level ranges the voltage gain of the input signal amplifier should be adjusted by selecting the appropriate external components as described in section 4.2
5. Noise (either impulsive or random type that has a flat frequency spectrum at the frequency range of interest) in the 300Hz-3400Hz band for V23 and 200Hz-3200Hz for Bell202.
6. Meeting any of these conditions will ensure non-detection.
7. Open loop, small signal, low frequency measurements.
8. Timing for an external input to the CLOCK/XTAL pin.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

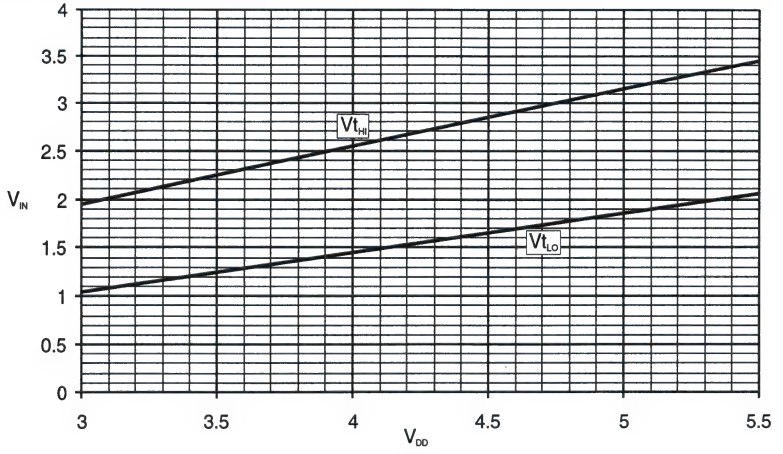


Figure 27: Schmitt Trigger typical input voltage thresholds vs. V_{DD}

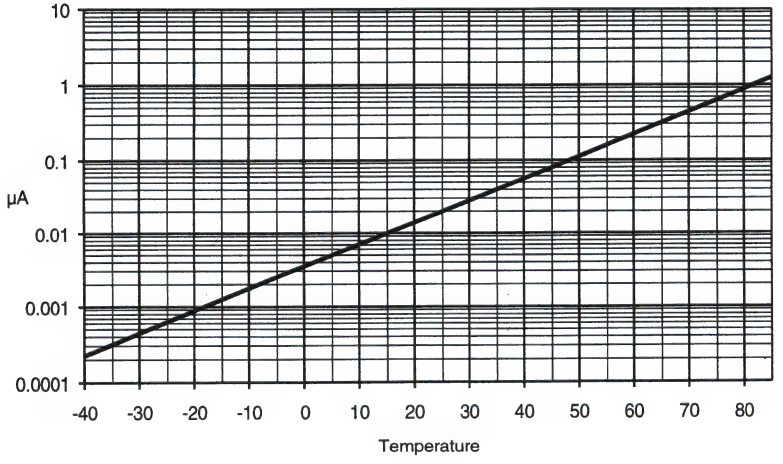
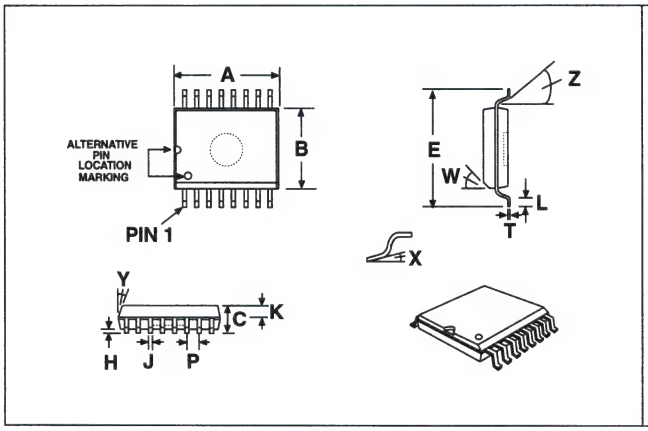


Figure 28: Typical 'Zero-Power' I_{DD} vs. Temperature (V_{DD} = 5.0V)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.2 Packaging

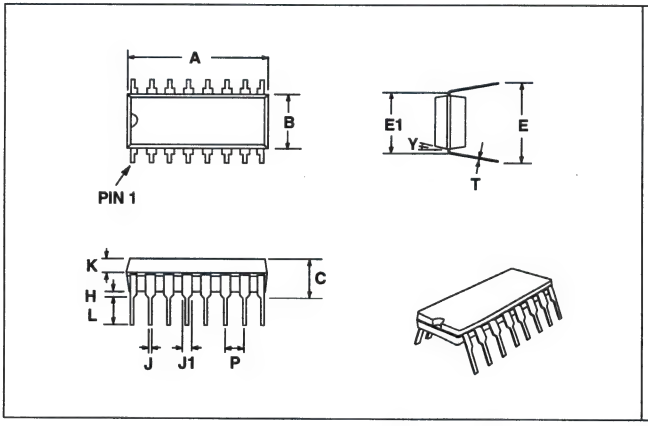


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 29 : 16-pin SOIC Mechanical Outline: *Order as part no. MX602DW*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 30 : 16-pin PDIP Mechanical Outline: *Order as part no. MX602P*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480136.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX604 v.23 Compatible Modem

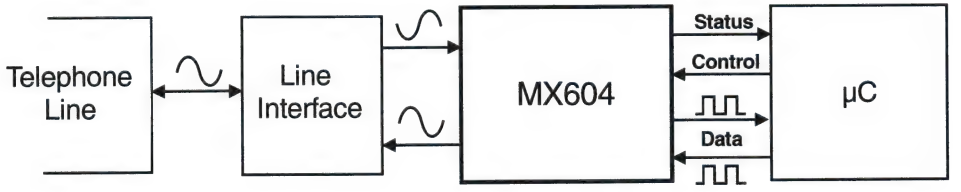
PRELIMINARY INFORMATION

FEATURES

- **1200bps forward, 75bps back channels**
- **Conforms to relevant sections of v.23 and ETSI specifications**
- **Line Equalization**
- **1200bps Data Retiming Facility can eliminate external UART**
- **Low Voltage Operation (3.3 to 5.0V)**

APPLICATIONS

- **Low Power Operation**
  1mA typ. @ 3.3V Operating Mode
  1μA typ. Zero-Power Mode
- **Standard 3.58Mhz Xtal/Clock**
- **Telephone Telemetry System Applications**



The MX604 is a low voltage, low power CMOS device, used for the reception or transmission of asynchronous 1200bps data and full-duplex 75bps back channel data in accordance with CCITT V.23 and ETSI specifications.

This device provides an optional Tx and Rx data retiming function which can eliminate, based on user preference, the need for an external UART when operating at 1200bps. The device can disable the back channel or be operated so only the mark or space tone is produced. The optional line equalizer is incorporated into the receive path and is controlled by an external logic level.

The MX604 may be used in a wide range of telephone telemetry systems. Low voltage capability, a low operating current (1mA typ. @ V_{DD} = 3.3V), and a very low current 'sleep' mode (1μA typ.) make the MX604 ideal for both portable terminal and line powered applications.

The MX604 is available in the following packages: 24-pin TSSOP (MX604TN), 16-pin SOIC (MX604DW) and 16-pin PDIP (MX604P).

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480152.002

CONTENTS

Section ..... **Page**

1. Block Diagram **2-31**

2. Signal List **2-32**

3. External Components **2-33**

4. General Description **2-33**

4.1 Xtal Osc and Clock Dividers 2-33
4.2 Mode Control Logic 2-34
4.3 Rx Input Amplifier 2-34
4.4 Receive Filter and Equalizer 2-34
4.5 Energy Detector 2-35
4.6 FSK Demodulator 2-35
4.7 FSK Modulator and Transmit Filter 2-35
4.8 Rx Data Retiming 2-37
4.9 Tx Data Retiming 2-38

5. Application **2-39**

5.1 Line Interface 2-39

6. Performance Specification **2-40**

6.1 Electrical Performance 2-40
6.2 Packaging 2-43

MX•COM, Inc. reserves the right to change specifications at any time and without notice

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480152.002

1. Block Diagram

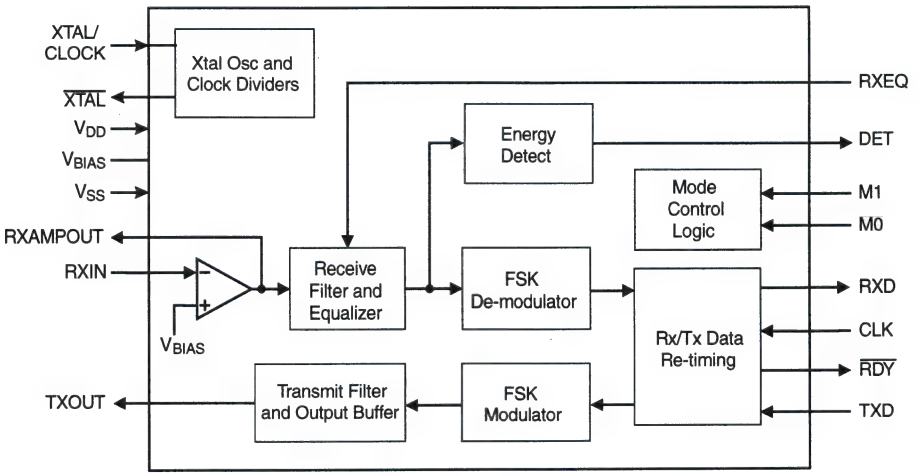


Figure 1: Block Diagram

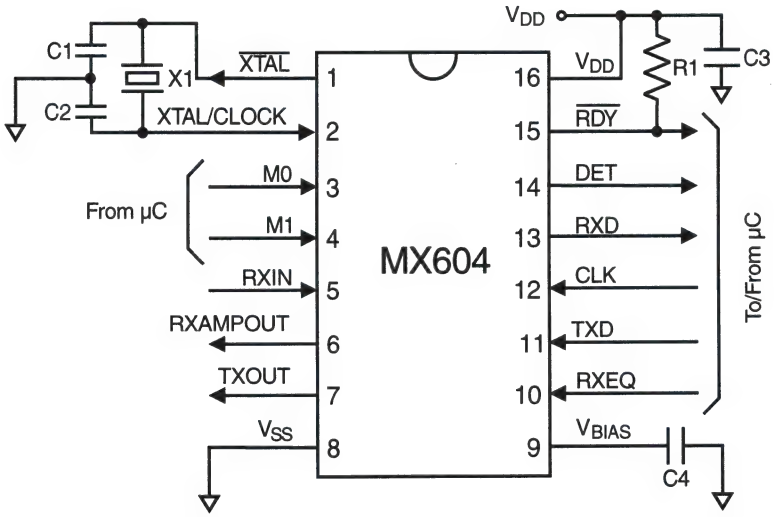
2. Signal List

Pin No.		Name	Type	Description
P, DW	TN			
1	1	$\overline{XTAL}$	output	Output of the on-chip Xtal oscillator inverter.
2	2	XTAL/CLOCK	input	Input to the on-chip Xtal oscillator inverter.
3	5	M0	input	A logic level input for setting the mode of the device. See section 4.2
4	6	M1	input	A logic level input for setting the mode of the device. See section 4.2
5	7	RXIN	input	Input to the Rx input amplifier.
6	8	RXAMPOUT	output	Output of the Rx input amplifier.
7	11	TXOUT	output	Output of the FSK generator.
8	12	V_{SS}	power	Negative supply (ground).
9	13	V_{BIAS}	output	Internally generated bias voltage, held at V_{DD} /2 when the device is not in 'Zero-Power' mode. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
10	14	RXEQ	input	A logic level input for enabling/disabling the equalizer in the receive filter. See section 4.4
11	17	TXD	input	A logic level input for either the raw input to the FSK Modulator or data to be re-timed depending on the state of the M0, M1 and CLK inputs. See section 4.9
12	18	CLK	input	A logic level input which may be used to clock data bits in/out of the FSK Data Retiming block.
13	19	RXD	output	A logic level output carrying either the raw output of the FSK Demodulator or re-timed characters depending on the state of the M0, M1 and CLK inputs. See section 4.8
14	20	DET	output	A logic level output of the on-chip energy detect circuit.
15	23	$\overline{RDY}$	output	"Ready for data transfer" output of the on-chip data retiming circuit. This open-drain active low output may be used as an Interrupt Request/Wake-up input to the associated µC. An external pull-up resistor should be connected between this output and V_{DD}.
16	24	V_{DD}	power	The positive supply rail. Levels and thresholds within the device are proportional to this voltage. Should be decoupled to V_{SS} by a capacitor mounted close to the device pins.
	3, 4, 9, 10 ,15, 16, 21, 22	N/C		No internal connections

This device is capable of detecting and decoding small amplitude signals. Achieving the V_{DD} and V_{BIAS} decoupling and protection of the receive path from extraneous in-band signals is very important. It is recommended that decoupling capacitors be placed so the connection between them and the device pins is as short as possible. A ground plane protecting the receive path will help attenuate interfering signals.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

3. External Components



R1		100kΩ	±5%,
C1, C2		18pF	±10%
C3		0.1µF	±10%
C4		0.1µF	±10%
X1	Note 1	3.579545MHz	

Figure 2: Recommended External Components for Typical Application

External Components Notes:

1. A crystal frequency of 3.579545MHz ±0.1% is required for correct FSK operation. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak-peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer. Operation of this device without a Xtal or Clock input may cause device damage.

4. General Description

4.1 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the MX604 is determined by a 3.579545MHz clock present at the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or it may be supplied from an external source to the XTAL/CLOCK input. If supplied from an external source, C1, C2 and X1 should not be used.

The on-chip oscillator is disabled in the 'Zero-Power' mode.

If the clock is provided by an external source which is not always running, then the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by MX604 as well as generating undefined states of the RXD, DET and $\overline{RDY}$ outputs.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480152.002

4.2 Mode Control Logic

The MX604's operating mode is determined by the logic levels applied to the M0 and M1 input pins:

M1	M0	Rx Mode	Tx Mode	Data Retime[1]
0	0	1200bps	75bps	Rx
0	1	off	1200bps	Tx
1	0	1200bps	off	Rx
1	1	'Zero-Power'		

[1] If enabled.

In the 'Zero-Power' mode, power is removed from all internal circuitry. When leaving 'Zero-Power' mode there must be a 20ms delay before any Tx data is passed to, or Rx data read from, the device to allow the bias level, filters and oscillator to stabilize. On applying power to the device the mode must be set to 'ZP', i.e. M0=1, M1=1, until V_{DD} has stabilized.

4.3 Rx Input Amplifier

The Rx Input Amplifier is used to adjust the signal received to the correct amplitude for the FSK receiver and Energy Detect circuits (see section 5.1).

4.4 Receive Filter and Equalizer

The Receive Filter and Equalizer is used to attenuate out of band noise and interfering signals, especially the locally generated 75bps transmit tones which might otherwise reach the 1200bps FSK Demodulator and Energy Detector circuits. This block also includes a switchable equalizer section. When the RXEQ pin is low the overall group delay of the receive filter is flat over the 1200bps frequency range. If the RXEQ pin is high the receive filter's typical overall group delay will be as shown in Figure 3.

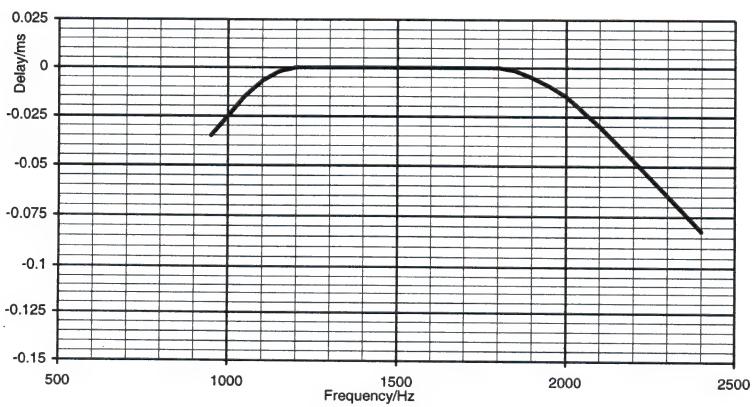


Figure 3: Rx Equalizer Group Delay (RXEQ = 1) with respect to 1700Hz

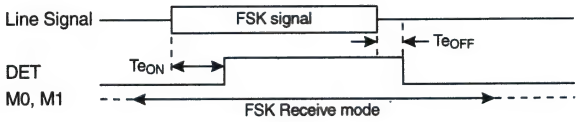
© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.5 Energy Detector

The Energy Detector block operates by measuring the level of the signal at the output of the Receive Filter, and comparing it against a preset threshold.

The DET output will be set high when the level has exceeded the threshold for a sufficient time. Amplitude and time hysteresis are used to reduce chattering of the DET output in marginal conditions.

Note: This circuit may also respond to non-FSK signals such as speech.



See section 6.1 for definitions of Te_{ON} and Te_{OFF}

Figure 4: FSK Level Detector Operation

4.6 FSK Demodulator

The FSK Demodulator block converts the 1200bps FSK input signal to a logic level received data signal which is output via the RXD pin as long as the Data Retiming function is not enabled (see section 4.8). This output does not depend on the state of the DET output.

When the Rx 1200bps mode is 'off' or in 'ZP' the DET and RXD pins are held low.

Note: In the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data. For this reason it is advised that the RXD pin be read only when data is expected.

4.7 FSK Modulator and Transmit Filter

The FSK Modulator and Transmit Filter blocks produce a tone according to the TXD, M0 and M1 inputs as shown in the table below, assuming data retiming is not being used:

M1	M0	TXD = 0	TXD = 1
1	1	-	
1	0	0Hz[1]	
0	0	450Hz	390Hz
0	1	2100Hz	1300Hz

FSK Modulator and Transmit Filter Note:

[1] TXOUT held at approx. $V_{DD}/2$.

When modulated at the appropriate baud rates, the Transmit Filter and associated external components (see section 5.1) limit the FSK out of band energy sent to the line in accordance with Figure 5 and Figure 6, assuming that the signal on the line is at -6dBm or less.

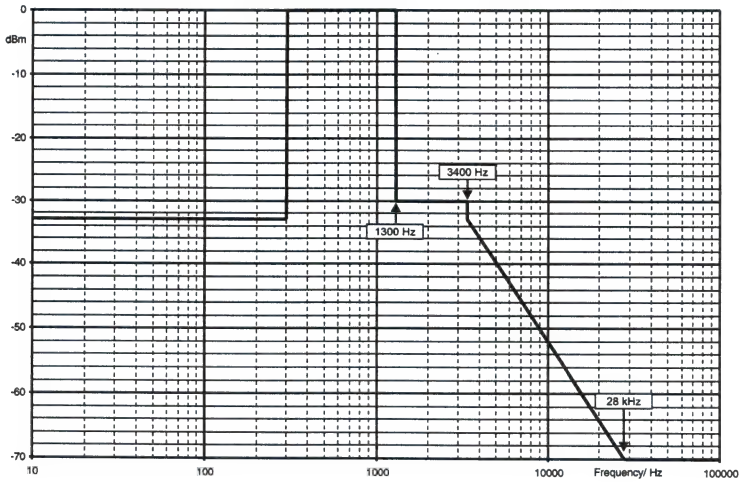


Figure 5: Tx limits at 75bps rate

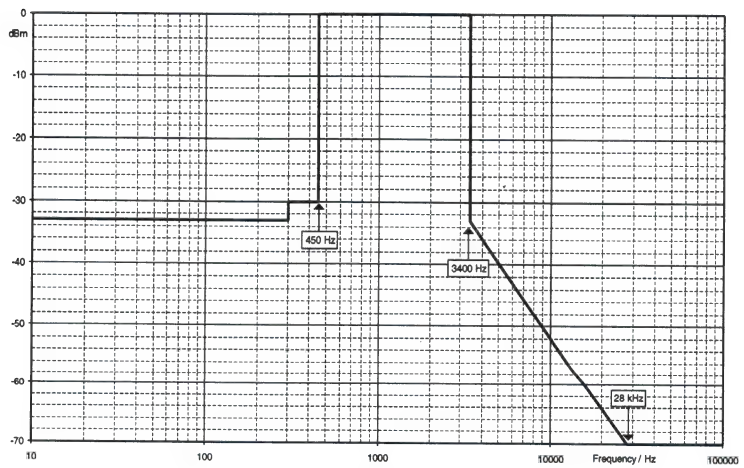


Figure 6: Tx limits at 1200bps rate

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.8 Rx Data Retiming

The Rx Data Retiming function may be used when the received data consists of 1200bps asynchronous characters, each character consisting of one start bit followed by a minimum of 9 formatted bits as shown in the table below.

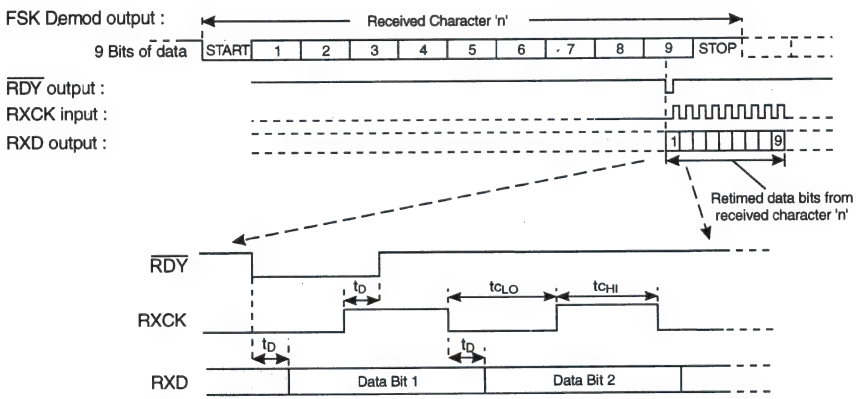
Data bits	Parity bits	Stop bits
7	0	≥2
7	1	≥1
8	0	≥1
8	1	≥1
9	0	≥1

When enabled in receive mode, the Data Retiming block extracts the first 9 bits of each character following the start bit, from the received asynchronous data stream, and presents them to the µC, under the control of strobe pulses applied to the CLK input. The timing of these pulses is not critical. They may be generated easily by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The receive retiming block consists of two 9-bit shift registers, the input of the first is connected to the output of the FSK demodulator and the output of the second is connected to the RXD pin. The first register is clocked by an internally generated signal that stores the 9 received bits following the timing reference of a high to low transition at the output of the FSK demodulator. When the 9th bit is clocked into the first register these 9 bits are transferred to the second register, a new stop-start search is initiated and the CLK input is sampled. If the CLK input is low at this time the $\overline{RDY}$ pin is pulled low and the first received bit is output on the RXD pin. The CLK pin should then be pulsed high 9 times, the first 8 high to low transitions will be used by the device to clock out the bits in the second register. The $\overline{RDY}$ output is cleared the first time the CLK input goes high. At the end of the 9th pulse the RXD pin will be connected to the FSK demodulator output.

To use the Data Retiming function, the CLK input should be kept low until the $\overline{RDY}$ output goes low; if the Data Retiming function is not required then the CLK input should be kept high at all times.

The only restrictions on the timing of the CLK waveform are those shown in Figure 7 and the need to complete the transfer of all nine bits into the µC within the time of a complete character at 1200bps.



t_D = Internal MX604 delay, t_{CHI} = CLK high time, t_{CLO} = CLK low time

Figure 7: FSK Operation with Rx Data Re-timing

Note: If enabled, the Data Retiming block may interpret speech or other signals as random characters.

If the Data Retiming facility is not required, the CLK input to the MX604 should be kept high at all times. The asynchronous data from the FSK Demodulator will then be connected directly to the RXD output pin, and the $\overline{RDY}$ output will not be activated by the FSK signal. This case is illustrated by the example in Figure 8

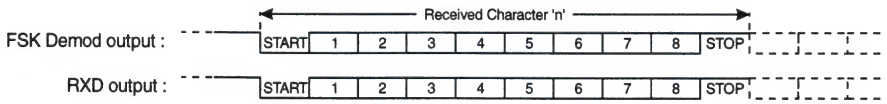


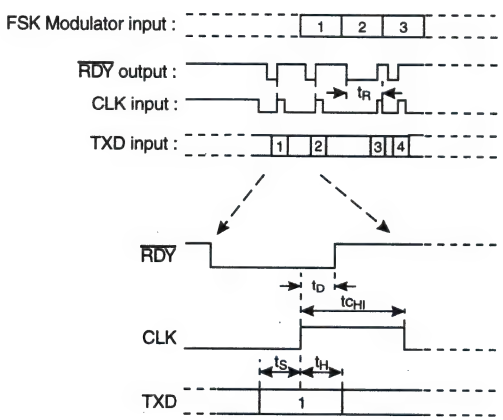
Figure 8: FSK Operation without Rx Data Re-timing (CLK always high)

4.9 Tx Data Retiming

The Tx Data Retiming block, when enabled in 1200bps transmit mode, requires the controlling µC to load 1 bit at a time into the device by a pulse applied to the CLK input. The timing of this pulse is not critical. It may be generated easily by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The Tx retiming circuit consists of two 1-bit registers in series, the input of the first is connected to the TXD pin and the output of the second feeds the FSK modulator. The second register is clocked by an internally generated 1200Hz signal and when this occurs the CLK input is sampled. If the CLK input is high the TXD pin directly controls the FSK modulator, if the CLK input is low the FSK modulator is controlled by the output of the second register and the $\overline{RDY}$ pin is pulled low. The $\overline{RDY}$ output is reset by a high level on the CLK input pin. A low to high change on the CLK input pin will latch the data from the TXD input pin into the first register ready for transfer to the second register when the internal 1200Hz signal next occurs.

To use the retiming option, the CLK input should be held low until the $\overline{RDY}$ output is pulled low. When the $\overline{RDY}$ pin goes low, the next data bit should be applied to the TXD input and the CLK input pulled high and then low within the time limits defined in Figure 9.



t_D = Internal MX604 delay; t_R = low to CLK going low; t_S = data set up time

t_{CHI} = CLK high time, t_H = data hold time

Figure 9: FSK Operation with Tx Data Retiming

To ensure synchronization between controlling device and the MX604 when entering Tx retiming mode the TXD pin must be held at a constant logic level from when the CLK pin is first pulled low to the end of loading in the second retimed bit.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Similarly when exiting Tx retiming mode the TXD pin should be held at the same logic level as the last retimed bit for at least 2 bit times after the CLK line is pulled high.

If the data retiming facility is not required, then the CLK input to the MX604 should be kept high at all times. The asynchronous data to the FSK modulator will then be connected directly to the TXD input pin. This is illustrated in Figure 10 and will also be the case when transmitting 75bps data which has no retime option.

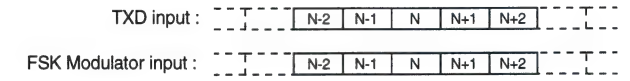


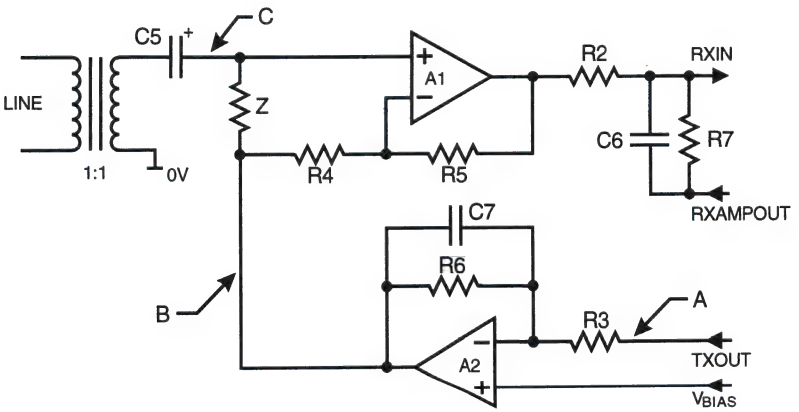
Figure 10: FSK Operation without Tx Data Re-timing (CLK always high)

5. Application

5.1 Line Interface

The signals on the telephone line are not suitable for direct connection to the MX604. A Line Interface circuit is necessary to:

- Provide high voltage and dc isolation
- Attenuate the Tx signal present at the Rx input
- Provide the low impedance drive necessary for the line
- Filter the Tx and Rx signals



R2	See Notes	±1%,
R3	See Notes	±1%,
R4-R7	100kΩ	±1%,

C5	22µF	±20%
C6	100pF	±10%
C7	330pF	±10%

Figure 11: Line Interface Circuit

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Line Interface Notes:

- The components 'Z' between points B and C should match the line impedance.
- Device A2 must be able to drive 'Z' and the line.
- R2: For optimum results R2 should be set so that the gain is $V_{DD}/5.0$, i.e. R2 = 100kΩ at V_{DD} = 5.0V, rising to 150kΩ at V_{DD} = 3.3V.
- R3: The levels in dB (relative to a 775mV_{RMS} signal) at 'A', 'B' and 'C' in the line interface circuit are:

'A' = 20Log(V_{DD}/5)

'B' = 'A' + 20Log(100kΩ/R3)

'C' = 'B' - 6

V_{DD}	'A'	R3	'B'	'C'
3.3V	-3.6dB	100kΩ	-3.6dB	-9.6dB
5.0V	0dB	150kΩ	-3.5dB	-9.5dB

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / PDIP Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Temperature		-40	85	°C
Xtal Frequency	1	3.575965	3.583125	MHz

Operating Limits Notes:

1. A crystal frequency of 3.579545MHz ±0.1% is required for correct FSK operation.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.3V at T_{AMB} = 25°C

Xtal Frequency = 3.579545MHz ± 0.1%, 0dBV corresponds to 1.0V_{RMS}, 0dB = 0dBm = 775mV_{RMS} into 600Ω.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (M0='1', M1='1')	1, 2		1		µA
I_{DD} (M0 or M1='0') at V_{DD} = 3.0V	1		1.0	1.25	mA
I_{DD} (M0 or M1='0') at V_{DD}= 5.0V	1		1.7	2.5	mA
Logic '1' Input Level		70%			V_{DD}
Logic '0' Input Level				30%	V_{DD}
Logic Input Leakage Current (V_{IN} = 0 to V_{DD}), Excluding XTAL/CLOCK Input		-1.0		1.0	µA
Output Logic '1' Level (I_{OH} = 360µA)		V_{DD}-0.4			V
Output Logic '0' Level (I_{OL} = 360µA)				0.4	V
Output 'off' State Current (V_{OUT} = V_{DD})				1.0	µA
FSK Demodulator					
Bit Rate		0	1200	1212	Baud
Mark (Logical 1) Frequency		1280	1300	1320	Hz
Space (Logical 0) Frequency		2068	2100	2132	Hz
Valid Input Level Range	3	-40.0		-8.0	dBV
Acceptable Twist (Mark Level WRT Space Level)		-7.0		7.0	dB
Acceptable Signal to Noise Ratio	4	20.0			dB
Level Detector 'On' Threshold Level	3			-40.0	dBV
Level Detector 'Off' to 'On' Time (Figure 4 Te_{ON})				25.0	ms
Level Detector 'On' to 'Off' Time (Figure 4 Te_{OFF})		8.0			ms
FSK Retiming					
Acceptable Rx Data Rate		1188	1200	1212	Baud
Tx Data Rate		1194		1206	Baud
FSK Modulator					
TXOUT Level	5	-1.0	0	1.0	dB
Twist (Mark Level WRT Space Level)		-2.0	0	2.0	dB
1200bps (M1='0', M0='1').					
Bit Rate		0	1200	1212	Baud
Mark (Logical 1) Frequency		1297		1303	Hz
Space (Logical 0) Frequency		2097		2103	Hz
75bps (M1='0', M0='0').					
Bit Rate		0	75	76	Baud
Mark (Logical 1) Frequency		388		392	Hz
Space (Logical 0) Frequency		448		452	Hz

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480152.002

	Notes	Min.	Typ.	Max.	Units
Input Amplifier					
Impedance (RXIN Pin)	6	10.0			MΩ
Voltage Gain	6		500		V/V
XTAL/CLOCK Input					
'High' Pulse Width	7	100			ns
'Low' Pulse Width	7	100			ns

Operating Characteristics Notes:

1. Not including any current drawn from the MX604 pins by external circuitry other than X1, C1 and C2.
2. TXD, RXEQ and CLK inputs at V_{SS}, M0 and M1 inputs at V_{DD}.
3. Measured at the Rx Input Amplifier output (pin RXAMPOUT) for 1300Hz and V_{DD}= 5.0V. The internal threshold levels are proportional to V_{DD}. To cater for other supply voltages or different signal level ranges the voltage gain of the Rx Input Amplifier should be adjusted by selecting the appropriate external components as described in section 5.1
4. Flat noise in 300-3400Hz band.
5. Relative to 775mV_{RMS} with V_{DD}= 5.0V for load resistance greater than 40kΩ.
6. Open loop, small signal low frequency measurements.
7. Timing for an external input to the XTAL/CLOCK pin.

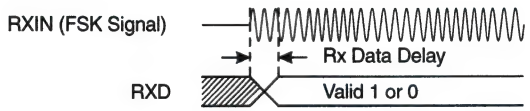
© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

6.2 Timing

Data and Mode Timing	Notes	Min.	Typ.	Max.	Units
Rx Data Delay (RXIN to RXD)	1, 5		2.55		ms
Tx Delay Data (TXD to TXOUT)	1, 6		0.1		ms
Mode change delay ZP to Tx or Rx	2			20	ms
Mode change delay Tx1200 to Rx1200	2			4.0	ms
Mode change delay Rx1200 to Tx1200	2			0.2	ms
t_D = Internal MX614 delay	3, 4			1	µs
tc_{HI} = CLK High time	3, 4	1			µs
tc_{LO} = CLK low time	3	1			µs
t_R = RDY low to CLK going low	4			800	µs
t_S = Data Set-up time	4	1			µs
t_H = Data Hold time	4	1			µs

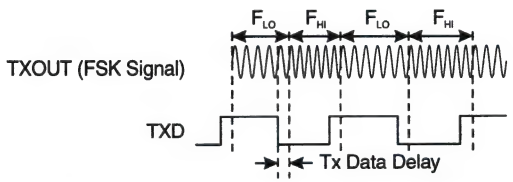
Timing Notes

1. When data retiming is not enabled.
2. Delay from mode change to reliable data at TXOUT or RXD pins.
3. Reference Figure 7.
4. Reference Figure 9.
5. Reference Figure 12.
6. Reference Figure 13.



Note: M0 and M1 are preset and stable.

Figure 12: RXIN to RXD Delay time

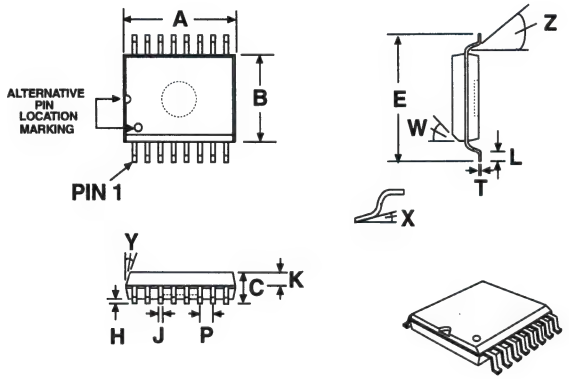


Note: M0 and M1 are preset and stable. F_{LO} and F_{HI} are the two FSK signaling frequencies.

Figure 13: TXD to TXOUT Delay time

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480152.002

6.3 Packaging

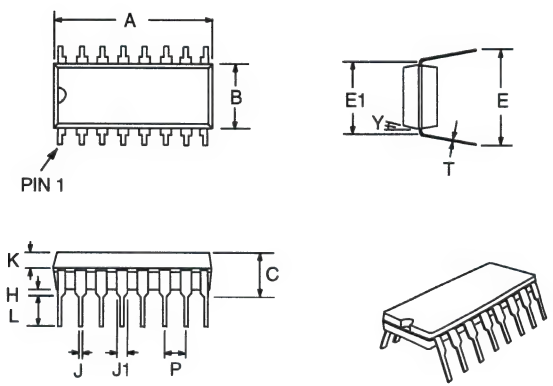


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 14: 16-pin SOIC Mechanical Outline: *Order as part no. MX604DW*



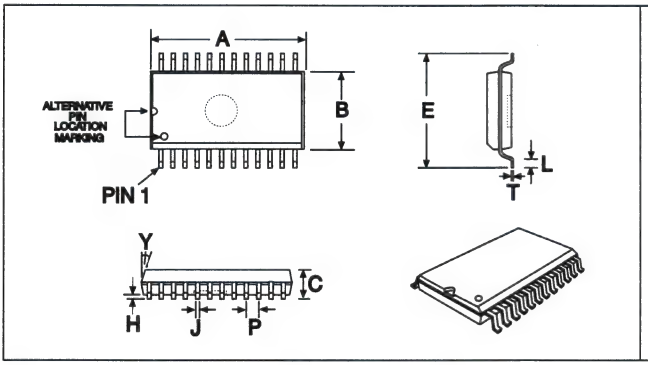
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE: All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 16-pin PDIP Mechanical Outline: *Order as part no. MX604P*

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 24-pin TSSOP Mechanical outline: *Order as part no. MX604TN*

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

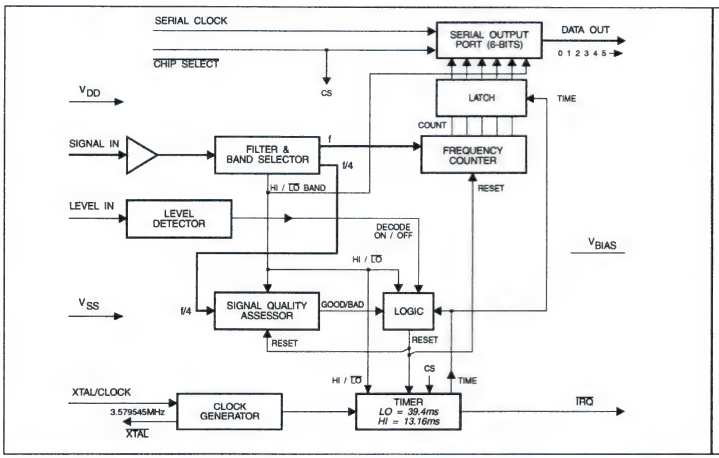
MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX613 Global Call Progress Detector

PRELIMINARY INFORMATION

- **MX•COM MiXed Signal CMOS**
- **Covers Worldwide Call Progress Frequencies (300Hz TO 2150Hz)**
- **Decode Single or Modulated Tones**
- **Analog In / Serial Data Out**
- **µProcessor Compatible Outputs**
- **Speech Discrimination Ability**
- **Low Power Operation**



AVAILABLE PACKAGES

MX613DW
16-pin SOIC

MX613P
14-pin PDIP

The MX613 is a wide-band, 'N-Tone' non-predictive tone decoder that measures telephone system call progress tones in PABX, Pay/Feature-Phone, Fax and Modem systems.

Adhering to Must/Must-Not Decode limits and able to measure inband frequencies in outband modulation, this decoder measures the frequency of input signals in the range 300 to 2,150Hz. The result of each measurement is presented to a system µProcessor as a 6-bit serial word.

The decode frequency range, which covers the world's call progress application spectrum, is processed internally as two bands: LO = 300 to 660Hz and HI = 900 to 2150Hz. Frequency measurement is achieved by counting the number of cycles in a set time period
(LO = 39.47ms or HI = 13.16ms). Bad signal/level quality or **NOTONE** results in a count-abort, timing-reset and no output from the decoder.

Front-end filtering is achieved using our patented Auto-Correlator. Current frequency information is output for the µProcessor using a Serial Data, Clock and Interrupt interface.

Data from the MX613 should be processed by a µProcessor whose algorithms are able to recognize the frequency, sequence and/or cadence of input signals as national call progress information; e.g.: 'Dial,' 'Busy,' 'Number-Unobtainable,' 'Ringing' and automatic tones used by fax and modem systems. Software can be simply configured to reject speech frequencies.

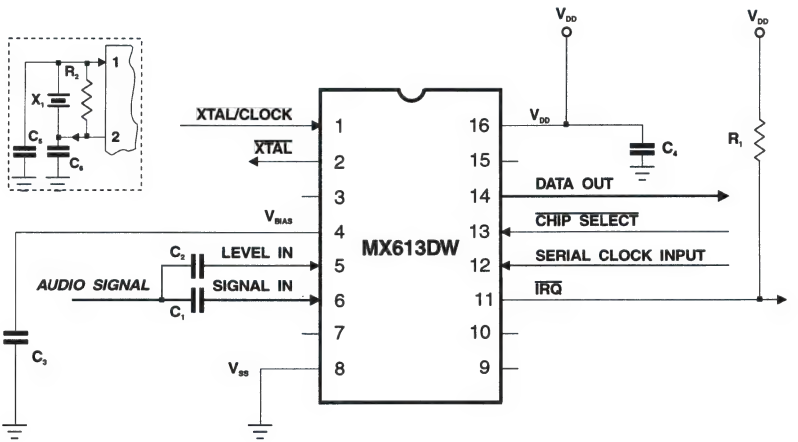
Available in SOIC and PDIP packages, this low-cost, mixed signal IC has a typical power requirement of less than 1mA at 3 volts and utilizes a telecom-system clock input of 3.579545MHz to maintain frequency accuracy.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480086.003
4800 Bethania Station Road. Winston-Salem. NC 27105-1201 USAAll trademarks and service marks are held by their respective companies

Pin Number		Function
MX613DW	MX613P	
1	1	**Xtal/Clock**: The input to the on-chip clock oscillator inverter. A 3.579545MHz Xtal or externally derived telephone system clock (f_{XTAL}) should be connected here. Operation of the MX613 without a suitable Xtal/Clock input may cause device damage.
2	2	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter. See Figure 2.
3	3	No internal connection.
4	4	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS}.
5	5	**Level In:** The input for level discrimination. This input is internally biased to V_{BIAS}. Signals must be a.c. coupled, and the audio signal must be fed to both this pin and the Signal In pin. Correct level detection determines the operation of this device (see Principles of Decoder Operation). But if you wish to disregard the amplitude of the input levels, the MX613 may be permanently enabled by pulling this pin to V_{DD} and disabled by pulling to V_{SS}.
6	6	**Signal In:** The input for frequency discrimination and decoding. This input is internally biased to V_{BIAS}. Signals must be a.c. coupled. The audio signal must be fed to both this pin and the Level In pin.
7		No internal connection.
8	7	**V_{SS}:** Signal ground (GND).
9	8	No internal connection.
10		No internal connection.
11	9	**$\overline{\text{IRQ}}$:** This Interrupt Request output from the MX613 is 'wire-OR able' allowing the interrupt outputs of other peripherals to be combined and connected to the Interrupt input of a µProcessor. This input has a low-impedance pulldown to V_{SS} when active and a high-impedance when inactive. An interrupt is produced on completion of a HI or LO frequency measurement.
12	10	**Serial Clock:** The serial clock from the µProcessor. Data Out is clocked into the µProcessor on the rising edge of the Serial Clock. See Data-Read Timing diagram.
13	11	**$\overline{\text{Chip Select}}$:** A logic "0" at this input will select this device.
14	12	**Data Out:** The serial data output. Under the control of the Chip Select and Serial Clock inputs, data should be read from this output in 6-bit blocks MSB (Bit-5) first. If 8 serial clock pulses are applied, two additional logic "0s" will be output after Bit-0.
15	13	No internal connection.
16	14	**V_{DD}:** Positive supply input. A single, stable supply is required. Levels and voltages within the MX613 are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor located close to the MX613 pins.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480086.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USAAll trademarks and service marks are held by their respective companies

Application Information



Notes

(1) The Xtal/Clock input may be driven from the host telephone system's 3.579545MHz clock; if a Xtal drive is required, the configuration shown in the INSET is recommended.

(2) The audio signal should be input to both Signal In and Level In pins via separate coupling capacitors. If it is wished to operate the device with disregard to on-chip level thresholds and permanently enable the MX613, the Level In pin should be held at V_{DD}.
To disable the MX613 the Level In pin should be held at V_{SS}.
Level thresholds are preset internally.

Component	Value
R_1	22.0kΩ
R_2	1.0MΩ
C_1	0.01µF
C_2	0.1µF
C_3	1.0µF
C_4	1.0µF
C_5	33.0pF
C_6	33.0pF
X_1	3.579545MHz

Tolerances: C = ± 20% R = ± 10%

Figure 2 - External Component Connections

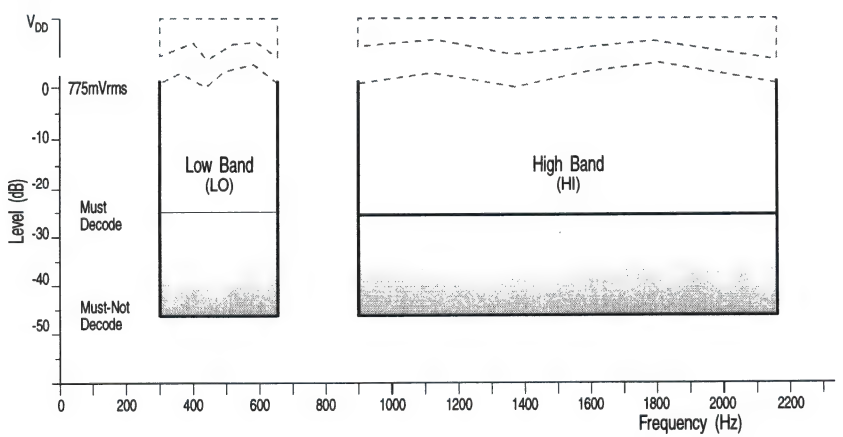


Figure 3 - HI/LO Decode Bands

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480086.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USAAll trademarks and service marks are held by their respective companies

Application Information .....

Principles of Decoder Operation

Level Detection

Because level and frequency discrimination operations take place in parallel, the audio signal should, under normal circumstances, be input to both Signal In and Level In pins via coupling capacitors.

If the input signal level (Level In) is outside the preset 'Must/Must Not Decode' thresholds (see Specifications), the Universal Call Progress Decoder will be disabled.

If it is wished to disregard signal input *levels* at the Level In pin and attempt to decode under all conditions, the decoder may be permanently enabled by holding the Level In pin at V_{DD}.

The MX613 can disabled by pulling Level In to V_{SS}.

NOTONE Recognition

The **NOTONE** condition can be recognized using µProcessor software timing as below.

a. Set the µP timer period to a period greater than the relevant frequency-band measurement period (13.16ms or 39.47ms).
b. Each 'Tone Measurement Complete' interrupt from the MX613 must reset the µP timer.
c. With **NOTONE** or white noise at the decoder input, the MX613 on-chip timer will be continually reset.
   i. 'Tone Measurement Complete' interrupt will not occur - the µP timer will run.
   ii. The µP Timer time-out can be considered as a **NOTONE** indication.

Level In	Timer	IRQ	Data Out	
In Limits	Running	Enabled	Enabled	
Out of Limits	Reset	Disabled	Disabled	(frozen to previous bit-5 level
V_{DD}	Running/Reset	Enabled/Disabled	Enabled	(dependent upon Quality measurement)
V_{SS}	Reset	Disabled	Disabled	(frozen to previous bit-5 level)

Frequency Band Discrimination

The input signal is amplified by a self-biased (zero-crossing) inverting amplifier and then 'filtered' to remove high-frequency noise and jitter.

High (HI) and Low (LO) counters are employed to determine the input frequency band (HI = 900Hz to 2150Hz, LO = 300Hz to 660Hz).

If the input frequency is in the LO Band, the device will operate as a LO Band decoder and will remain so until a HI frequency signal is detected. If the input frequency is in the HI Band, the device will operate as a HI Band decoder and will remain so until a LO frequency signal is detected.

Frequency band monitoring is continuous with the band selection taking place every 9.8ms. It will therefore take 9.8ms from Power-Up to set up the initial correct decode frequency band.

On-Chip Timer Operation

For frequency measurement, the MX613 counts the number of input cycles in a fixed time period. This fixed period, measured by the continuous on-chip timer, is set to 13.16ms for HI Band inputs and 39.47ms for LO Band inputs.

When the timer expires the following actions take place:

a. A HI or LO ("1" or "0") band indication bit is latched into Bit-5 of the Serial Output Port.
b. The Frequency Counter count of 5-bits is latched into the Serial Output Port (Bit-4 [MSB] to Bit-0). The Serial Output Port Contains 6-bits, if 8 Serial Clock edges are employed, two extra "0s", which should be ignored, will be output last.
c. An interrupt is generated (IRQ) to the µProcessor. The contents of the Serial Output Port should be read before the next interrupt is expected; if not data will be overwritten.

When the Chip Select input is set to "0" the interrupt is reset.

The On-Chip Timer and Frequency Counter will be reset in mid-count, and therefore unable to allow a valid measurement, under the following conditions:

a. A change of decode frequency band.
b. Decoder disabled; signal input level out of specification or Level Detect input set to V_{SS}.
c. Signal Quality Assessment considered 'Bad'.
d. Input signal frequency outside limits.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480086.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USAAll trademarks and service marks are held by their respective companies

Application Information .....

N = int (Frequency x Measurement Period)

Measurement Period = 39.47ms for Low Band (300Hz to 660Hz)
= 13.16ms for High Band (900Hz to 2150Hz)

Note: For input frequencies of between 661Hz and 899Hz the MX613 will give no reliable output.

When a 'correct' decode has been allowed and an interrupt generated, a 6-bit data word is presented at the Serial Output Port. This 6-bit word indicates the input frequency's band (Bit 5) and value 'N' as indicated below.

Bit 5 Output First	Band Bit (5)	MSB (4)	(3)	(2)	(1)	LSB (0)	Bits 0 to 4 = N
	HI-"1"/LO-"0"	Bits 0 to 4 represent the measured frequency in the selected band					

When a 'correct' decode has been allowed and an interrupt generated, a 6-bit data word will be presented at the Serial Output Port. This 6-bit word indicates the input frequency's band and value as described below.

As an example, the following binary-word presented at the Serial Output Port **(1 1 0 1 1 0)** will indicate a frequency in the **HI Band** of between **1680Hz** and **1740Hz (Bit-5 = "1" = HI, 'N' = 22).**

LO Band	HI Band	N	B_5	B_4	B_3	B_2	B_1	B_0	LO Band	HI Band	N	B_5	B_4	B_3	B_2	B_1	B_0
280	*840*	11	H/L	0	1	0	1	1	505	1515	19	H/L	1	0	0	1	1
285	*855*	11							510	1530	20	H/L	1	0	1	0	0
290	*870*	11							515	1545	20						
295	885	11							520	1560	20						
300	900	11							525	1575	20						
305	915	12	H/L	0	1	1	0	0	530	1590	20						
310	930	12							535	1605	21	H/L	1	0	1	0	1
315	945	12							540	1620	21						
320	960	12							545	1635	21						
325	975	12							550	1650	21						
330	990	13	H/L	0	1	1	0	1	555	1665	21						
335	1005	13							560	1680	22	H/L	1	0	1	1	0
340	1020	13							565	1695	22						
345	1035	13							570	1710	22						
350	1050	13							575	1725	22						
355	1065	14	H/L	0	1	1	1	0	580	1740	22						
360	1080	14							585	1755	23	H/L	1	0	1	1	1
	365	1095	14							590	1770	23					
370	1110	14							595	1785	23						
375	1125	14							600	1800	23						
380	1140	14							605	1815	23						
385	1155	15	H/L	0	1	1	1	1	610	1830	24	H/L	1	1	0	0	0
390	1170	15							615	1845	24						
395	1185	15							620	1860	24						
400	1200	15							625	1875	24						
405	1215	15							630	1890	24						
410	1230	16	H/L	1	0	0	0	0	635	1905	25	H/L	1	1	0	0	1
415	1245	16							640	1920	25						
420	1260	16							645	1935	25						
425	1275	16							650	1950	25						
430	1290	16							655	1965	25						
435	1305	17	H/L	1	0	0	0	1	660	1980	26	H/L	1	1	0	1	0
440	1320	17							*665*	1995	26						
445	1335	17							*670*	2010	26						
450	1350	17							*675*	2025	26						
455	1365	17							*680*	2040	26						
460	1380	18	H/L	1	0	0	1	0	*685*	2055	27	H/L	1	1	0	1	1
465	1395	18							*690*	2070	27						
470	1410	18							*695*	2085	27						
475	1425	18							*700*	2100	27						
480	1440	18							*705*	2115	27						
485	1455	19	H/L	1	0	0	1	1	*710*	2130	28	H/L	1	1	1	0	0
490	1470	19							*715*	2145	28						
495	1485	19							*720*	2160	28						
500	1500	19							*725*	*2175*	28						

Table 1 - Decode Frequency Data

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480086.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USAAll trademarks and service marks are held by their respective companies

Application Information .....

Decoder Timing

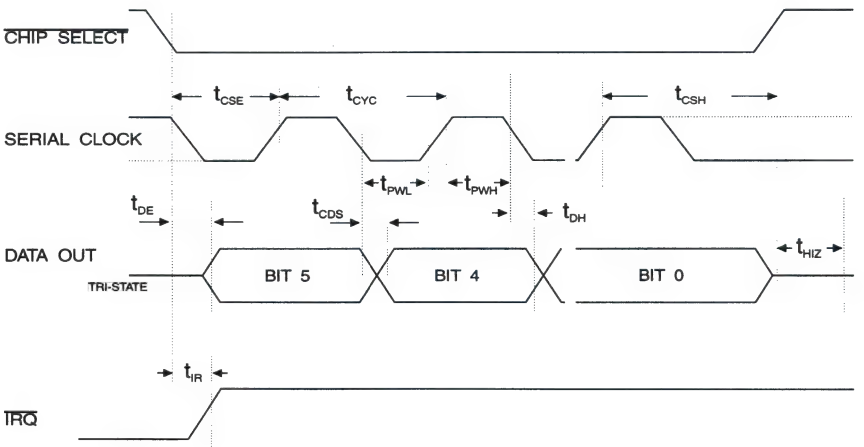


Figure 4 - Data-Read Timing

Decoder Timing Characteristics

With reference to Figure 4, *Data-Read Timing*.

	Characteristics	Min.	Typ.	Max.	Unit
t_{PWH}	Serial Clock "High" Pulse Width	250	-	-	ns
t_{PWL}	Serial Clock "Low" Pulse Width	250	-	-	ns
t_{CYC}	Serial Clock-Cycle Time	600	-	-	ns
t_{CSE}	Chip Select Low to Clock "High" Edge	450	-	-	ns
t_{CSH}	Last Clock "High" Edge to CS "High"	600	-	-	ns
t_{DH}	Data Out Hold Time	0	-	-	ns
t_{CDS}	Clock Edge to Data Out Set Time	-	-	200	ns
t_{IR}	Interrupt (IRQ) Reset Time	-	-	200	ns
t_{DE}	Chip Select "Low" to Data Enable	-	-	200	ns
t_{HIZ}	Chip Select "High" to Output Tri-State	-	-	1000	ns

Notes

1 Data is output bit 5 first. Bit 5 can be clocked into the µProcessor by the first Serial Clock rising edge. If 8 Serial Clock pulses are employed the last 2 data-bits will be "0" and should be ignored by the software.

2 Chip Select should be used to react to Interrupts and then returned to a logic "1". If Chip Select stays low there will be no further Interrupts and no Data Output update.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480086.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USAAll trademarks and service marks are held by their respective companies

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{SS}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current (supply pins)	± 30mA
(other pins)	±20mA
Total Device Dissipation (@ T_{AMB}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 3.3V

T_{OP} = 25°C

Audio Level 0dB ref = 775 mVrms

Xtal/Clock f_0 = 3.579545 MHz

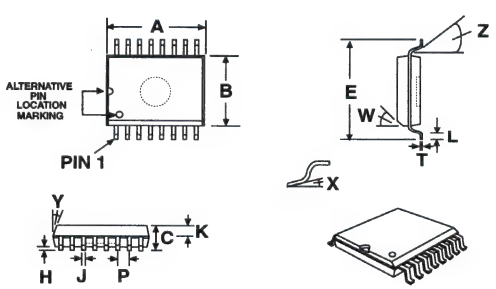
Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage (V_{DD}) at 25°C		3.0	-	5.5	V
Supply Current		-	0.3	1.0	mA
Input Logic "1"		70.0	-	100	% V_{DD}
Input Logic "0"		0	-	30.0	% V_{DD}
Output Logic "1"	1	90.0	-	100	% V_{DD}
Output Logic "0"	1	-	-	10.0	% V_{DD}
Impedances					
Chip Select and Serial Clock Input		10.0	-	-	MΩ
Signal Input		-	50.0	-	kΩ
Level Input		-	210	-	kΩ
IRQ Output (Logic "0")		-	-	500	Ω
Data Output (Logic "0")		-	500	-	Ω
(Logic "1")		-	-	2.5	kΩ
Dynamic Values					
On-Chip Xtal Oscillator					
R_{IN}		10.0	-	-	MΩ
R_{OUT}		-	230	825	kΩ
DC Voltage Gain		25.0	42.0	-	V/V
Bandwidth at Unity Gain		5.0	11.0	-	MHz
Single Tone Operation					
Must-Decode Input Level	2	-25.2	-	-	dB

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480086.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USAAll trademarks and service marks are held by their respective companies

Characteristics	See Note	Min.	Typ.	Max.	Unit
Must-Not Decode Input Level	2	-	-	-46.0	dB
LO Band Frequency Range	4	300		660	Hz
HI Band Frequency Range	4	900		2150	Hz
Frequency Resolution (Table 1)					
LO Band		-	-	25.0	Hz
HI Band		-	-	75.0	Hz
Input Signal/White-Noise Ratio (HI & LO Bands)		-	18.0	-	dB
Interrupt Rate (LO Band)	3	19.0	-	-	/sec
(HI Band)	3	57.0	-	-	/sec
False Decodes Due to Noise	6	-	1.0	-	/2 secs
Outband modulation level limits					
for correct decode (f_{IN} = 340Hz to 620Hz)	5	-	-	10.0	%

Notes

1. Into a high-impedance load (>1.0MΩ).
2. Must decode signal above -25.2dB; Must Not decode signal below -46.0dB.
   If a supply other than 3.3 volts is used, levels will change pro-rata.
3. Under 'Pure Tone' input conditions.
4. For input frequencies of between 661Hz and 899Hz the MX613 will provide no reliable output.
5. With an amplitude modulating frequency of between 16.0Hz and 100Hz.
6. Test noise input = 5.0kHz at 100mVrms



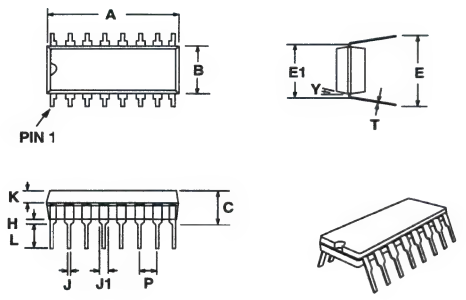
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 16-pin SOIC Mechanical Outline: *order as part no. MX613DW*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480086.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USAAll trademarks and service marks are held by their respective companies



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91)
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin PDIP Mechanical Outline: *order as part no. MX613P*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480086.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USAAll trademarks and service marks are held by their respective companies

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX614 Bell 202 Compatible Modem

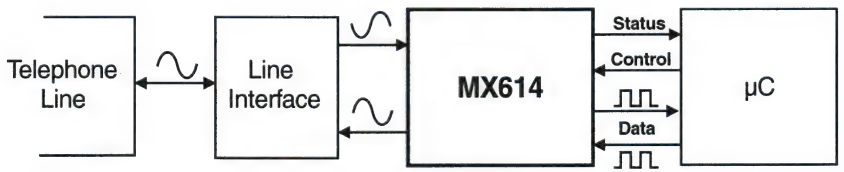
PRELIMINARY INFORMATION

Features

- **1200bps half duplex Bell 202 Compatible Modem**
- **Optional 1200bps Data Retiming Facility can eliminate external UART**
- **Optional 5bps and 150bps Back Channel**
- **Optional Line Equalization**

Applications

- **Low Voltage Operation (3.3V to 5.0V)**
- **Low Power Operation**
  - **1mA typ. @ 3.3V Operating Mode**
  - **1µA typ. Zero-Power Mode**
- **Standard 3.58MHz Xtal/Clock**
- **Telephone Telemetry Applications**



The MX614 is a low voltage, low power CMOS integrated circuit designed for the reception or transmission of asynchronous 1200bps data. This device is compatible with Bell 202 type systems. The MX614 supports 5bps and 150bps 'back channel' operation.

The MX614 provides an optional Tx and Rx data retiming function which can eliminate, based on user preference, the need for a UART in the associated µC when operating at 1200bps. An optional line equalizer has been incorporated into the receive path and is controlled by an external logic level.

The MX614 may be used in a wide range of telephone telemetry systems. A very low current "Zero Power Mode (1µA typ.) and an operating current of 1mA typ. @ V_{DD} = 3.3V, make the MX614 ideal for portable, terminal and line powered applications. A standard 3.58MHz Xtal/Clock is required and the device operates from a 3.0V to 5.5V supply.

The MX614 is available in 24-pin TSSOP (MX614TN), 16-pin SOIC (MX614DW) and 16-pin PDIP (MX614P) packages.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480162.001

CONTENTS

Section ..... Page

1. Block Diagram 2-59

2. Signal List 2-60

3. External Components 2-61

4. General Description 2-61
4.1 Xtal Osc and Clock Dividers 2-61
4.2 Mode Control Logic 2-62
4.3 Rx Input Amplifier 2-62
4.4 Receive Filter and Equalizer 2-62
4.5 Energy Detector 2-63
4.6 FSK Demodulator 2-63
4.7 FSK Modulator and Transmit Filter 2-63
4.8 Rx Data Retiming 2-65
4.9 Tx Data Retiming 2-66

5. Application Notes 2-67
5.1 Line Interface 2-67

6. Performance Specification 2-68
6.1 Electrical Performance 2-68
6.2 Timing 2-71
6.3 Packaging 2-72

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480162.001

1. Block Diagram

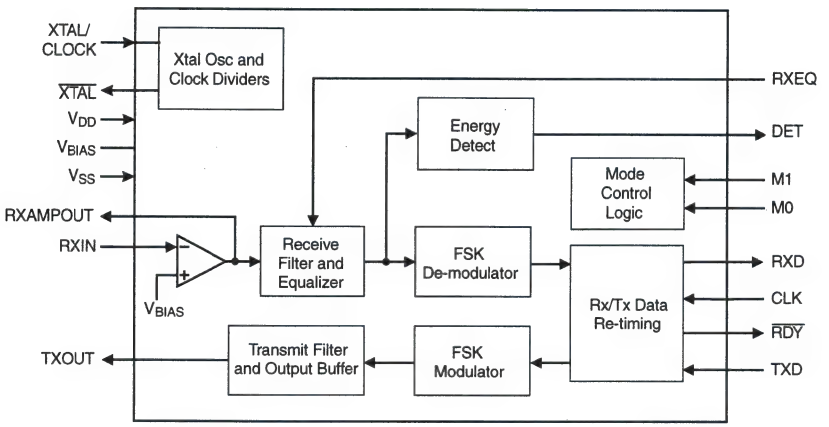


Figure 1: Block Diagram

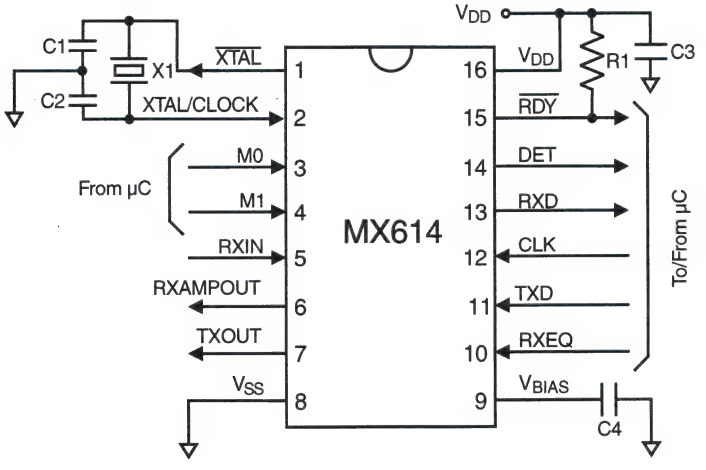
2. Signal List

Pin No.		Name	Type	Description
P, DW	TN			
1	1	$\overline{XTAL}$	output	Output of the on-chip Xtal oscillator inverter.
2	2	XTAL/CLOCK	input	Input to the on-chip Xtal oscillator inverter.
3	5	M0	input	A logic level input for setting the mode of the device. See section 4.2
4	6	M1	input	A logic level input for setting the mode of the device. See section 4.2
5	7	RXIN	input	Input to the Rx input amplifier.
6	8	RXAMPOUT	output	Output of the Rx input amplifier
7	11	TXOUT	output	Output of the FSK generator.
8	12	V_{SS}	Power	Negative supply (ground).
9	13	V_{BIAS}	output	Internally generated bias voltage, held at $V_{DD}/2$ when the device is not in 'Zero-Power' mode. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
10	14	RXEQ	input	A logic level input for enabling/disabling the equalizer in the receive filter. See section 4.4
11	17	TXD	input	A logic level input for either the raw input to the FSK Modulator or data to be re-timed depending on the state of the M0, M1 and CLK inputs. See section 4.9
12	18	CLK	input	A logic level input which may be used to clock data bits in or out of the FSK Data Retiming block.
13	19	RXD	output	A logic level output carrying either the raw output of the FSK Demodulator or re-timed characters depending on the state of the M0, M1 and CLK inputs. See section 4.8
14	20	DET	output	A logic level output of the on-chip Energy Detect circuit.
15	23	$\overline{RDY}$	output	"Ready for data transfer" output of the on-chip data retiming circuit. This open-drain active low output may be used as an Interrupt Request/Wake-up input to the associated µC. An external pull-up resistor should be connected between this output and V_{DD}.
16	24	V_{DD}	Power	Positive supply. Levels and thresholds within the device are proportional to this voltage. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
	3, 4, 9, 10 ,15, 16, 21, 22	N/C		No internal connection

This device is capable of detecting and decoding small amplitude signals. To achieve this V_{DD} and V_{BIAS} decoupling and protecting the receive path from extraneous in-band signals are very important. It is recommended that the decoupling capacitors be placed so that connections between them and the device pins are as short as practicable. A ground plane protecting the receive path will help attenuate interfering signals.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480162.001

3. External Components



R1		100kΩ	±5%
C1 C2		18pF	±10%
C3		0.1µF	±10%
C4		0.1µF	±10%
X1	Note 1	3.579545MHz	

Figure 2: Recommended External Components for Typical Application

External Components Notes

1. A crystal frequency of 3.479545MHz ±0.1% is required for correct FSK operation. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD} peak-peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

4.1 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the MX614 is determined by a 3.579545MHz clock signal present at the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or may be supplied from an external source to the XTAL/CLOCK input. If supplied from an external source, C1, C2 and X1 should not be fitted.

The on-chip oscillator is turned off in the 'Zero-Power' mode.

If the clock is provided by an external source which is not always running, then the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by MX614 as well as generating undefined states of the RXD, DET and $\overline{RDY}$ outputs.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.2 Mode Control Logic

The MX614's operating mode is determined by the logic levels applied to the M0 and M1 input pins:

M1	M0	Rx Mode	Tx Mode	Data Retime[1]
0	0	1200bps	150bps	Rx
0	1	Off	1200bps	Tx
1	0	1200bps	Off / 5bps	Rx
1	1	'Zero-Power'		-

[1] If enabled

In the 'Zero-Power' (ZP) mode, power is removed from all internal circuitry. When leaving the 'ZP' mode there must be a delay of 20ms before any Tx data is passed to, or Rx data read from the device to allow the bias level, filters, and oscillator to stabilize. On applying power to the device, the mode must be set to 'ZP', i.e. M0 = '1', M1 = '1', until V_{DD} has stabilized.

4.3 Rx Input Amplifier

This amplifier is used to adjust the received signal to the correct amplitude for the FSK receiver and Energy Detect circuits (see section 5.1).

4.4 Receive Filter and Equalizer

The Receive Filter and Equalizer section is used to attenuate out of band noise and interfering signals, especially the locally generated transmit tones which might otherwise reach the 1200bps FSK Demodulator and Energy Detector circuits. This block also includes a switchable equalizer section. When the RXEQ pin is low, the overall group delay of the receive filter is flat over the 1200bps frequency range. If the RXEQ pin is high the receive filter's typical overall group delay will be as shown in Figure 3.

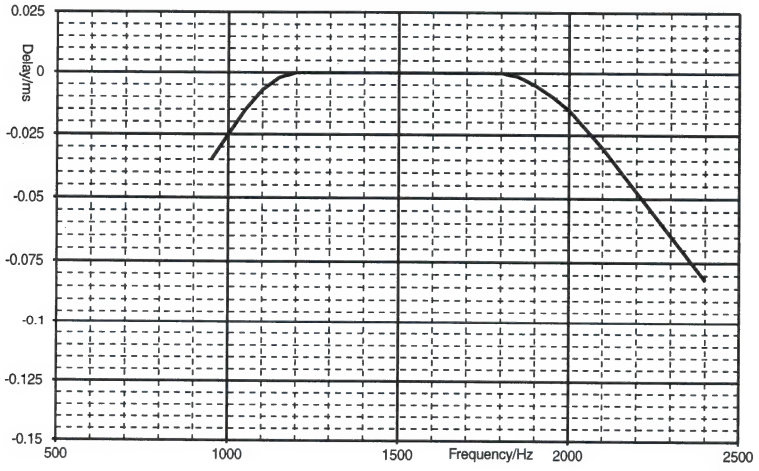


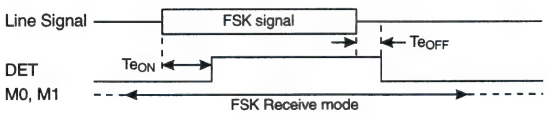
Figure 3: Rx Equalizer Group Delay (RXEQ = '1') wrt 1700Hz

4.5 Energy Detector

This block operates by measuring the level of the signal at the output of the Receive Filter, and comparing it against a preset threshold.

The DET output will be set high when the level has exceeded the threshold for a sufficient period of time. Amplitude and time hysteresis are used to reduce chattering of the DET output in marginal conditions.

Note that this circuit may also respond to non-FSK signals such as speech.



See section 6.1 for definitions of Te_{ON} and Te_{OFF}

Figure 4: FSK Level Detector Operation

4.6 FSK Demodulator

This block converts the 1200bps FSK input signal to a logic level received data signal which is output via the RXD pin as long as the Data Retiming function is not enabled (see section 4.8). This output does not depend on the state of the DET output.

When the Rx 1200bps mode is 'Off' or in 'ZP' the DET and RXD pins are held low.

Note that in the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data. For this reason it is advised that the RXD pin is read only when data is expected.

4.7 FSK Modulator and Transmit Filter

These blocks produce a tone according to the TXD, M0 and M1 inputs as shown in the table below, assuming data retiming is not being used:

M1	M0	TXD = 0	TXD = 1
1	1	-	-
1	0	0Hz[1]	387Hz
0	0	487Hz	387Hz
0	1	2200Hz	1200Hz

Note: [1] TXOUT held at approx. $V_{DD}/2$.

When modulated at the appropriate baud rates, the Transmit Filter and associated external components (see section 5.1) limit the FSK out of band energy sent to the line in accordance with Figure 5 and Figure 6, assuming that the signal on the line is at -6dBm or less.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

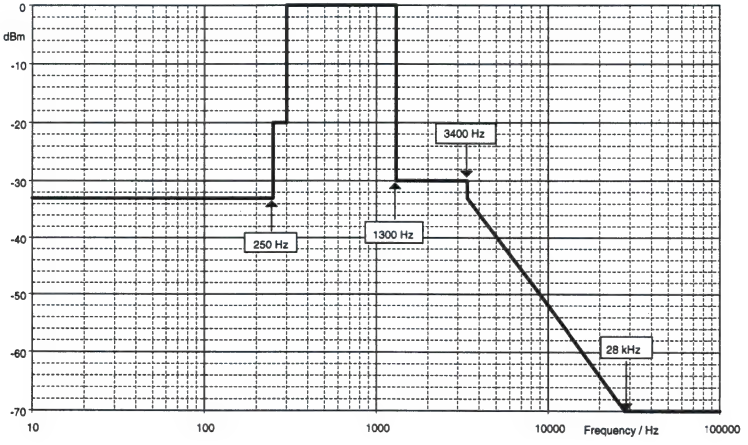


Figure 5: Tx limits at 5bps and 150bps rate

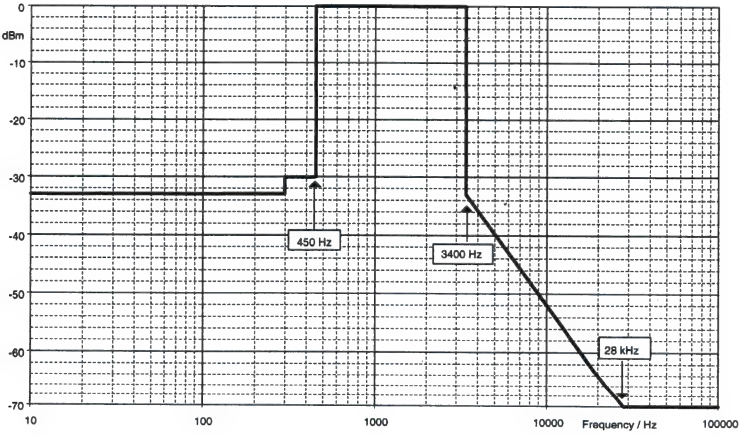


Figure 6: Tx limits at 1200bps rate

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

4.8 Rx Data Retiming

This function may be used when the received data consists of 1200bps asynchronous characters, each character consisting of one start bit followed by a minimum of 9 formatted bits as shown in the table below.

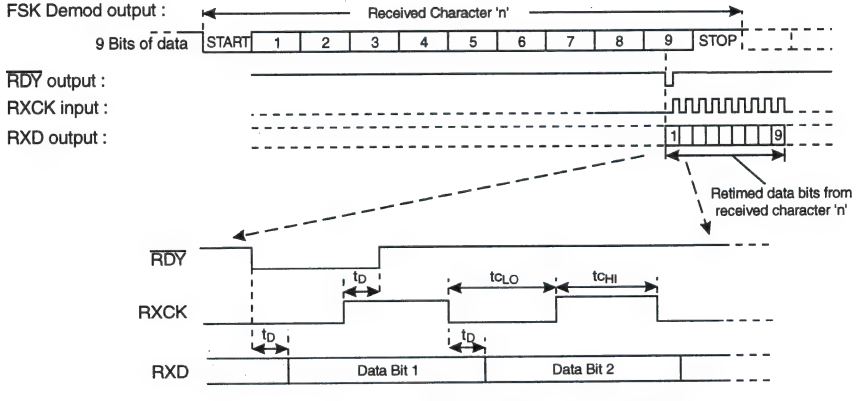
Data bits	Parity bits	Stop bits
7	0	≥ 2
7	1	≥ 1
8	0	≥ 1
8	1	≥ 1
9	0	≥ 1

The Data Retiming block, when enabled in receive mode, extracts the first 9 bits of each character following the start bit from the received asynchronous data stream, and presents them to the µC under the control of strobe pulses applied to the CLK input. The timing of these pulses is not critical and they may easily be generated by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The receive retiming block consists of two 9-bit shift registers, the input of the first is connected to the output of the FSK demodulator and the output of the second is connected to the RXD pin. The first register is clocked by an internally generated signal that stores the 9 received bits following the timing reference of a high to low transition at the output of the FSK demodulator. When the 9th bit is clocked into the first register these 9 bits are transferred to the second register, a new stop-start search is initiated and the CLK input is sampled. If the CLK input is low at this time the $\overline{RDY}$ pin is pulled low and the first received bit is output on the RXD pin. The CLK pin should then be pulsed high 9 times, the first 8 high to low transitions will be used by the device to clock out the bits in the second register. The $\overline{RDY}$ output is cleared the first time the CLK input goes high. At the end of the 9th pulse the RXD pin will be connected to the FSK demodulator output.

So to use the Data Retiming function, the CLK input should be kept low until the $\overline{RDY}$ output goes low; if the Data Retiming function is not required the CLK input should be kept high at all times.

The only restrictions on the timing of the CLK waveform are those shown in Figure 7 and the need to complete the transfer of all nine bits into the µC within the time of a complete character at 1200bps.



t_D = Internal MX614 delay, tc_{HI} = CLK high time, tc_{LO} = CLK low time

Figure 7: FSK Operation with Rx Data Retiming

Note that, if enabled, the Data Retiming block may interpret speech or other signals as random characters.

If the Data Retiming facility is not required, the CLK input to the MX614 should be kept high at all times. The asynchronous data from the FSK Demodulator will then be connected directly to the RXD output pin, and the $\overline{RDY}$ output will not be activated by the FSK signal. This case is illustrated by the example in Figure 8.

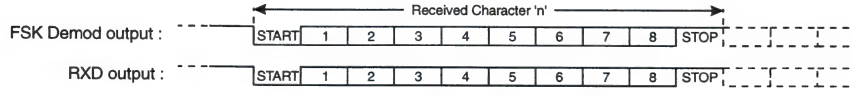


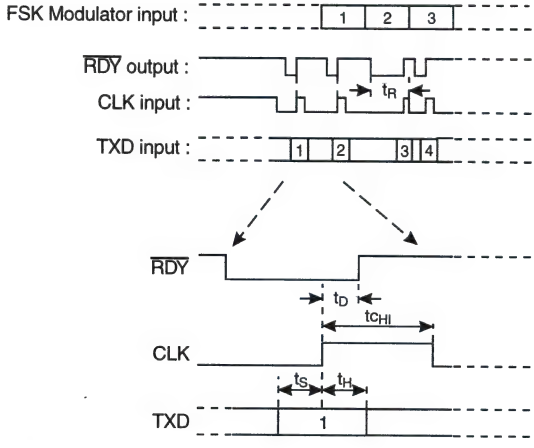
Figure 8: FSK Operation without Rx Data Retiming (CLK always high)

4.9 Tx Data Retiming

The Data Retiming block, when enabled in 1200bps transmit mode, requires the controlling µC to load one bit at a time into the device by a pulse applied to the CLK input. The timing of this pulse is not critical and it may easily be generated by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The Tx re-timing circuit consists of two 1-bit registers in series, the input of the first is connected to the TXD pin and the output of the second feeds the FSK modulator. The second register is clocked by an internally generated 1200Hz signal and when this occurs the CLK input is sampled. If the CLK input is high the TXD pin directly controls the FSK modulator, if the CLK input is low the FSK modulator is controlled by the output of the second register and the $\overline{RDY}$ pin is pulled low. The $\overline{RDY}$ output is reset by a high level on the CLK input pin. A low to high change on the CLK input pin will latch the data from the TXD input pin into the first register ready for transfer to the second register when the internal 1200Hz signal next occurs.

So to use the retiming option the CLK input should be held low until the $\overline{RDY}$ output is pulled low. When the $\overline{RDY}$ pin goes low the next data bit should be applied at the TXD input and the CLK input pulled high and then low within the time limits set out in Figure 9.



t_D = Internal MX614 delay, t_R = $\overline{RDY}$ low to CLK going low, t_S = data set up time

t_{CHI}= CLK high time, t_H = data hold time

Figure 9: FSK Operation with Tx Data Retiming

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

To ensure synchronization between the controlling device and the MX614 when entering Tx retiming mode the TXD pin must be held at a constant logic level from when the CLK pin is first pulled low to the end of loading in the second retimed bit. Similarly when exiting Tx retiming mode the TXD pin should be held at the same logic level as the last retimed bit for at least 2 bit times after the CLK line is pulled high.

If the data retiming facility is not required, the CLK input to the MX614 should be kept high at all times. The asynchronous data to the FSK modulator will then be connected directly to the TXD input pin. This is illustrated in Figure 10 and will also be the case when transmitting 5bps or 150bps data which has no retime option.

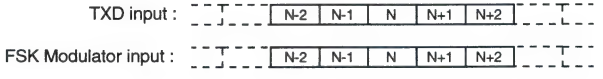


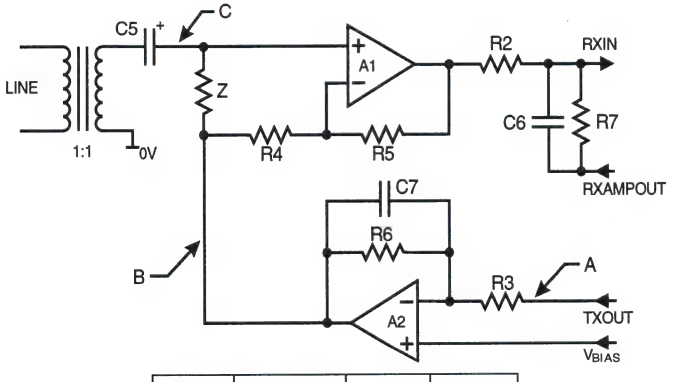
Figure 10: FSK Operation without Tx Data Retiming (CLK always high)

5. Application

5.1 Line Interface

The signals on the telephone line are not suitable for direct connection to the MX614. A Line Interface circuit is required to:

- Provide high voltage and dc isolation
- Attenuate the Tx signal present at the Rx input
- Provide the low impedance drive necessary for the line
- Filter the Tx and Rx signals



R2	See Notes		±1%,
R3	See Notes		±1%,
R4-R7		100kΩ	±1%,
C5		22µF	±20%
C6		100pF	±10%
C7		330pF	±10%

Figure 11: Line Interface Circuit

Line Interface Notes:

1. The components 'Z' between points B and C should match the line impedance.
2. Device A2 must be able to drive 'Z' and the line.
3. R2: For optimum results R2 should be set so that the gain is $V_{DD}/5.0$, i.e. R2 = 100kΩ at V_{DD} = 5.0V, rising to 150kΩ at V_{DD} = 3.3V.
4. R3: The levels in dB (relative to a 775mV_{RMS} signal) at 'A', 'B' and 'C' in the line interface circuit are:

   Level at 'A' = 20Log(V_{DD}/5)
   " 'B' = 'A' + 20Log(100kΩ/R3)
   " 'C' = 'B' - 6

Example:

V_{DD}	'A'	R3	'B'	'C'
3.3V	-3.6dB	100kΩ	-3.6dB	-9.6dB
5.0V	0dB	150kΩ	-3.5dB	-9.5dB

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of and pins			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / PDIP Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	**Min.**	**Max.**	**Units**
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency	1	3.575965	3.583125	MHz

Operating Limits Notes:

1. A crystal frequency of 3.579545MHz ±0.1% is required for correct FSK operation.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.3V at T_{AMB} = 25°C
Xtal Frequency = 3.579545MHz ± 0.1% 0dBV corresponds to 1.0V_{RMS}
0dBm corresponds to 775mV_{RMS} into 600Ω.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (M0 = '1', M1 = '1')	1, 2		1.0		µA
I_{DD} (M0 or M1 = '0') at V_{DD} = 3.0V	1		1.0	1.25	mA
I_{DD} (M0 or M1 = '0') at V_{DD} = 5.0V	1		1.7	2.5	mA
Logic '1' Input Level		70%			V_{DD}
Logic '0' Input Level				30%	V_{DD}
Logic Input Leakage Current (V_{IN} = 0 to V_{DD}), Excluding XTAL/CLOCK Input		-1.0		1.0	µA
Output Logic '1' Level (I_{OH} = 360µA)		V_{DD} -0.4			V
Output Logic '0' Level (I_{OL}= 360µA)				0.4	V
$\overline{RDY}$ Output 'off' State Current (V_{OUT} = V_{DD})				1.0	µA
FSK Demodulator					
Bit Rate		0	1200	1212	Baud
Mark (Logical '1') Frequency		1188	1200	1212	Hz
Space (Logical '0') Frequency		2178	2200	2222	Hz
Valid Input Level Range	3	-40.0		-8.0	dBV
Maximum Twist (Mark Level wrt Space Level)		±6.0			dB
Acceptable Signal to Noise Ratio	4	20.0			dB
Level Detector 'On' Threshold Level	3			-40.0	dBV
Level Detector 'Off' to 'On' Time (Figure 4 Te_{ON})				25.0	ms
Level Detector 'On' to 'Off' Time (Figure 4 Te_{OFF})		8.0			ms
FSK Retiming					
Acceptable Rx Data Rate		1188	1200	1212	Baud
Tx Data Rate		1194		1206	Baud
FSK Modulator					
TXOUT Level	5	-1.0	0	1.0	dB
Twist (Mark Level wrt Space Level)		-2.0	0	2.0	dB
Tx 1200bps (M1 = '0', M0 = '1').					
Bit Rate		0	1200	1212	Baud
Mark (Logical '1') Frequency		1197		1203	Hz
Space (Logical '0') Frequency		2196		2204	Hz
Tx 150bps (M1 = '0', M0 = '0').					
Bit Rate		0	150	152	Baud
Mark (Logical '1') Frequency		385		389	Hz
Space (Logical '0') Frequency		485		489	Hz

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480162.001

	Notes	Min.	Typ.	Max.	Units
Tx 5bps (M1 = '1', M0 = '0').					
Bit Rate		0	5.0	5.1	Baud
Mark (Logical '1') Frequency		385		389	Hz
Space (Logical '0') Frequency	6		0		Hz
Input Amplifier					
Impedance (RXIN Pin)	7	10.0			MΩ
Voltage Gain	7		500		V/V
XTAL/CLOCK Input					
'High' Pulse Width	8	100			ns
'Low' Pulse Width	8	100			ns

Operating Characteristics Notes:

1. Not including any current drawn from the MX614 pins by external circuitry other than X1, C1 and C2.
2. TXD, RXEQ and CLK inputs at V_{SS}, M0 and M1 inputs at V_{DD}.
3. Measured at the Rx Input Amplifier output (pin RXAMPOUT) for 1300Hz and V_{DD}= 5.0V. The internal threshold levels are proportional to V_{DD}. To cater for other supply voltages or different signal level ranges the voltage gain of the Rx Input Amplifier should be adjusted by selecting the appropriate external components as described in section 5.1
4. Flat noise in 300 - 3400Hz band.
5. Relative to 775mV_{RMS} at V_{DD}= 5.0V for load resistance greater than 40kΩ.
6. TXOUT held at approximately V_{DD}/2.
7. Open loop, small signal low frequency measurements.
8. Timing for an external input to the XTAL/CLOCK pin.

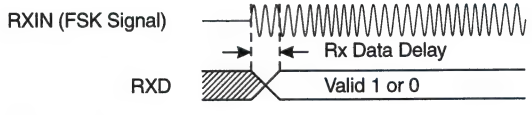
© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480162.001

6.2 Timing

Data and Mode Timing	Notes	Min.	Typ.	Max.	Units
Rx Data Delay (RXIN to RXD)	1, 5		2.55		ms
Tx Delay Data (TXD to TXOUT)	1, 6		0.1		ms
Mode change delay ZP to Tx or Rx	2			20	ms
Mode change delay Tx1200 to Rx1200	2			4.0	ms
Mode change delay Rx1200 to Tx1200	2			0.2	ms
t_D = Internal MX614 delay	3, 4			1	µs
tc_{HI} = CLK High time	3, 4	1			µs
tc_{LO} = CLK low time	3	1			µs
t_R = RDY low to CLK going low	4			800	µs
t_S = Data Set-up time	4	1			µs
t_H = Data Hold time	4	1			µs

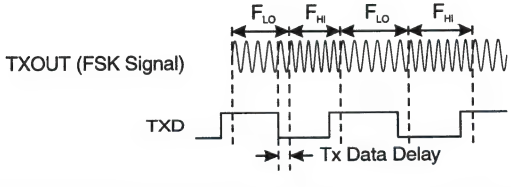
Timing Notes

1. When data retiming is not enabled.
2. Delay from mode change to reliable data at TXOUT or RXD pins.
3. Reference Figure 7.
4. Reference Figure 9.
5. Reference Figure 12.
6. Reference Figure 13.



Note: M0 and M1 are preset and stable.

Figure 12: RXIN to RXD Delay time

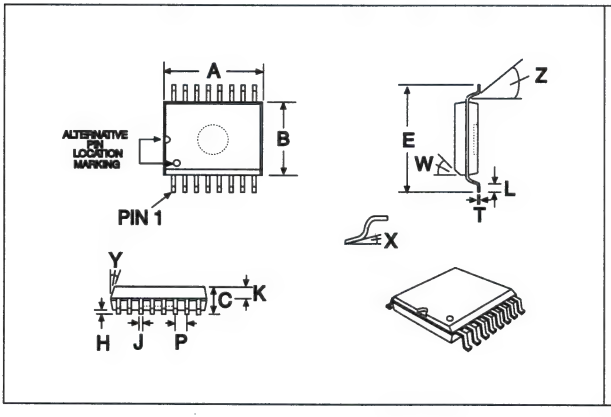


Note: M0 and M1 are preset and stable. F_{LO} and F_{HI} are the two FSK signaling frequencies.

Figure 13: TXD to TXOUT Delay time

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480162.001

6.3 Packaging

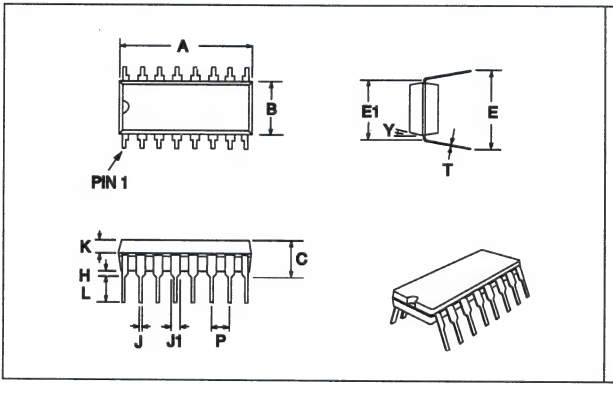


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 14: 16-pin SOIC Mechanical Outline: *Order as part no. MX614DW*



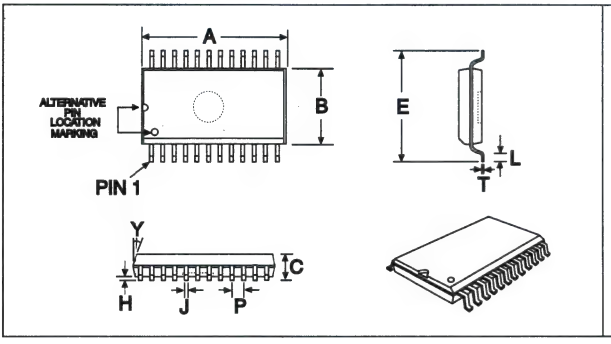
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 16-pin PDIP Mechanical Outline: *Order as part no. MX614P*

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16 : 24-pin TSSOP Mechanical Outline: *Order as part no. MX614TN*

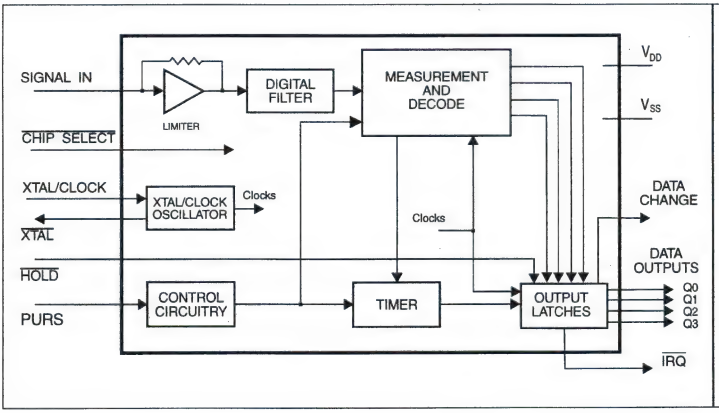
MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX623 Line-Powered Call Progress Tone Detector

PRELIMINARY INFORMATION

- **MX•COM MiXed Signal CMOS**
- **Custom Tone Decoder (13 Call-Progress Frequencies Recognized)**
- **Operates to a 3.579545MHz Telephone System Clock**
- **Operates Under Simple Logic or µProcessor System Control**
- **Measures Call Progress Tone Frequencies ('Busy', 'Dial', 'Fax-Tone' etc.)**
- **Telephone, PABX, Fax and Dial-Up Modem Applications**
- **Low-Power Requirement (600µA at 3.3 Volts$_{TYP}$) for Line-Powered Applications**



AVAILABLE PACKAGES

MX623P 16-pin PDIP

The MX623 is a low-power decoding integrated circuit that measures the frequency of telephone system call progress tones.

With progress signals input from the telephone line, this single-chip product is programmed to recognize up to thirteen of the World's most commonly used call-progress frequencies, analyze signal quality, and present the measured result as a 4-bit parallel data word at the tri-state Data Output.

Using the parallel information from the MX623, the host system, can recognize such call progress information as: 'Dial', 'Busy', 'Number Unobtainable', 'Ringing' and Fax/Modem system signals.

This information can then be used in simple or complex applications to control telephone operations. The data output will require a software format that can analyze the frequency information from the MX623.

Requiring only a single 3.0$_{[MIN]}$ volt power supply, the MX623 may be line-powered and will operate under simple logic or system µProcessor control using the 'Data-Change, 'Hold' and 'Chip-Select' functions.

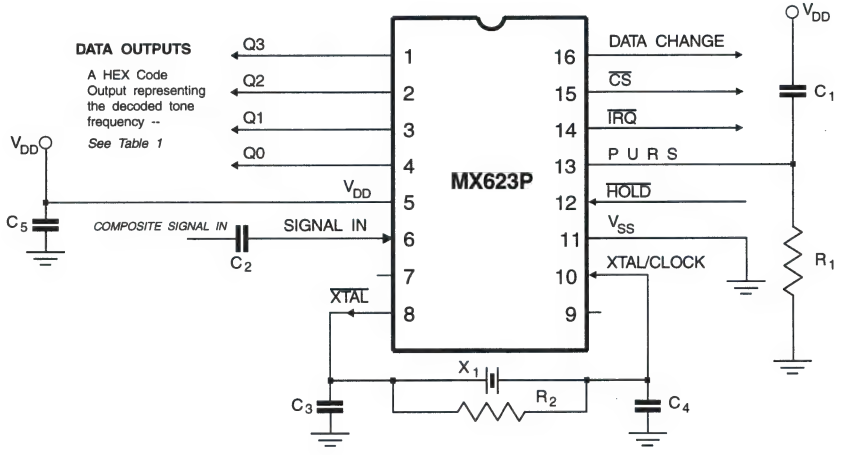
The MX623, whose small size and low power consumption makes it ideal for remote applications, requires a 3.579545MHz telephone system clock or Xtal input, is available in a 16-pin PDIP.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480091.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Pin	Function
1 2 3 4	**Q3:** **Data Outputs:** A 4-bit parallel data word, forming a HEX character representing the decoded **Q2:** tone frequency. This word is output after a successful decode. Table 1 details the Hex **Q1:** character output codes for the relevant decoded tone frequencies. Upon power-up this output **Q0:** is set to 'E_H', but no Data Change pulse generated. These are tri-state outputs.
5	**V_{DD}:** Positive supply rail. A minimum supply voltage of 3.0 volts is required. Levels and voltages within this decoder are dependent upon this supply.
6	**Signal In:** The composite audio input. Signals to this pin should be a.c. coupled. The d.c. bias of the limiter section is set internally; this pin should not be loaded with any other circuitry.
7	No internal connection. Leave open circuit.
8	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter.
9	No internal connection. Leave open circuit.
10	**Xtal/Clock:** The input to the clock oscillator inverter. A 3.579545MHz Xtal or externally derived clock should be connected here (see Figure 2).
11	**V_{SS}:** Negative supply rail (GND).
12	**$\overline{\text{Hold}}$:** An input to control the Output Latch condition; employed in combination with the Data Change output to facilitate, if required, Interrupt and/or handshake operations with a µProcessor. With $\overline{\text{Hold}}$ placed "Low", with a tone input, the Data Change output will be held "High" at the next data change, and the current output code is locked in the Output Latches regardless of any changes to the input signal. The output code remains as held until this input is returned "High" (see Figure 3). While this input is "High" the output data, Q0 - Q3, cycles normally with the input audio. This pin has an internal 1.0MΩ pullup resistor.
13	**PURS:** Power-Up ReSet. To reset internal circuitry at power-up; a logic "1" level is required at this pin for a duration of at least 2.5ms after the Xtal/Clock input and full V_{DD} levels are applied. The component configuration shown in Figure 2 is recommended; for slow-rising power supplies the time constant of components should be increased accordingly.
14	**$\overline{\text{IRQ}}$:** Interrupt Request. An output for µProcessor operation; normally "High" this output is latched "Low" when an internal data change occurs if the Chip Select input is "High". This output is reset ("High") the when Chip Select line is taken "Low". To permit "wire-OR" connection with other peripherals, this output has a low-impedance when "Low" and a high-impedance when "High".
15	**$\overline{\text{CS}}$:** Chip Select- A controlling function. When held "High" the Data Outputs Q0, Q1, Q2 and Q3 and the Data Change output are disabled. When taken "Low" the Data Outputs Q0, Q1, Q2 and Q3 and the Data Change output are enabled; the Interrupt Request (IRQ) is reset ("High") when CS is taken "Low". See Figures 3 and 4.
16	**Data Change:** A positive-going pulse is generated at this output when the data changes (Tone or NOTONE). New tone-data is presented to the Q0, Q1, Q2 and Q3 Data Outputs if the Hold input is set "High". This is a tri-state output.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480091.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Application Information



Component	Value	Component	Value
R_1	1.0MΩ	C_3	33.0pF
R_2	1.0MΩ	C_4	33.0pF
C_1	.047µF	C_5	1.0µF
C_2	.0047µF	X_1	3.579545MHz

Tolerances R = ±10%, C = ±20%

Figure 2 - Recommended External Components

Hex Character	Output Code Q3 Q2 Q1 Q0	Band Edges (Hz) Lower Edge	Band Edges (Hz) Upper Edge	Nominal Center Freq.
0	0 0 0 0	364	386	*375*
1	0 0 0 1	488	520	*500*
2	0 0 1 0	520	580	*550*
3	0 0 1 1	580	618	*600*
4	0 1 0 0	386	412	*400*
5	0 1 0 1	412	436	*425*
6	0 1 1 0	436	463	*450*
7	0 1 1 1	463	487	*475*
8	1 0 0 0	900	1008	*950*
9	1 0 0 1	1273	1325	*1300*
A	1 0 1 0	1350	1455	*1400*
B	1 0 1 1	1750	1855	*1800*
C	1 1 0 0	2062	2140	*2100*
D	1 1 0 1	frequency not guaranteed		
E	1 1 1 0	frequency not guaranteed		
F	1 1 1 1	NOTONE		

Table 1 - Tone Decode Frequencies

Timing Information

With CS Low - Figure 3

After initial power-up and the Hold input inactive (High), as frequencies are input, with the Data Change output as an active (High) indicator, the data is presented at the Data Outputs.

If/when the Hold input is placed active (Low), the data at the Data Outputs is frozen and the Data Change output held High at its next active excursion -until the Hold input is returned High.

With the Hold input held High - Figure 4

As frequencies are input a correct decode will produce an active (Low) interrupt level.

This interrupt (IRQ) is serviced and reset by an active (Low) CS input.

Note the 'valid data' period at the Data Outputs.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480091.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Application Information - Decoder Timing

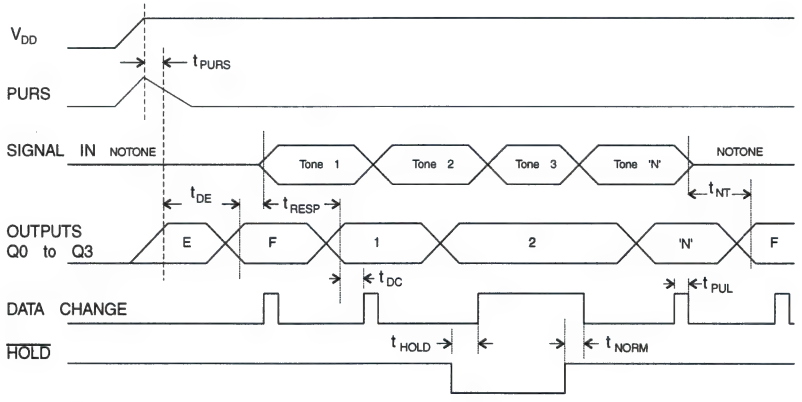


Figure 3 - Timing with the Chip Select Input Held "Low"; $\overline{CS}$ and $\overline{IRQ}$ are not used

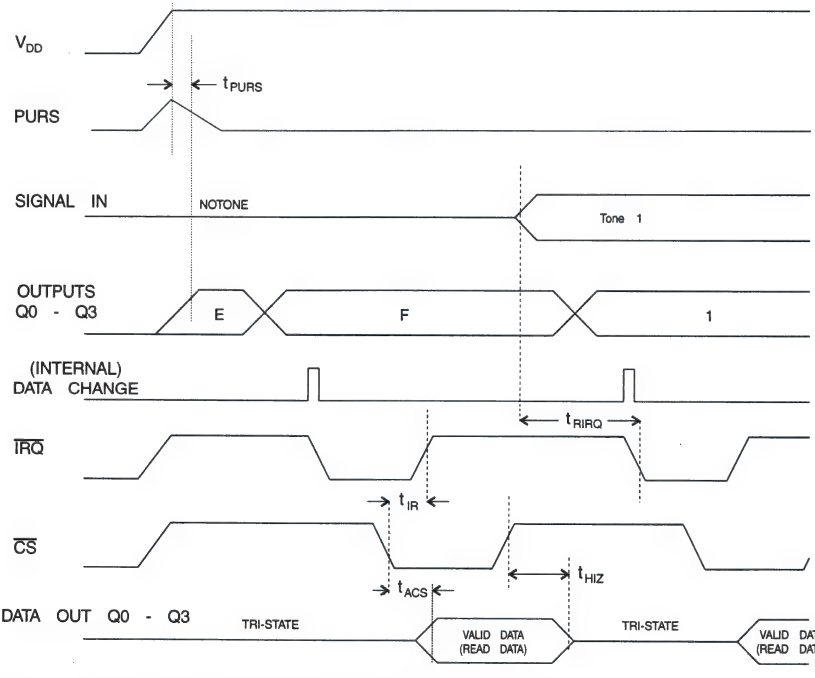


Figure 4 - Timing with the HOLD Input Held "High"; $\overline{CS}$ and $\overline{IRQ}$ are used

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480091.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)	+/- 30mA
(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Storage temperature range	-40°C to +85°C

Operating Limits

	Min.	Max.	Unit
Supply Voltage (V_{DD}) at 25°C	3.0	5.5	V
Operating Temperature	-40	+85	°C

All device characteristics are measured under the following conditions unless otherwise specified:

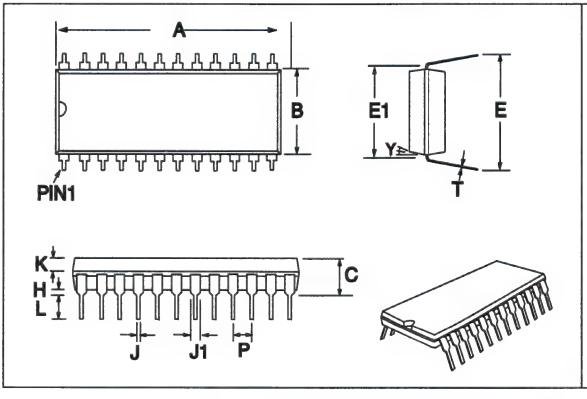
V_{DD} = 3.3V
T_{OP} = 25 °C
Audio Level 0dB ref: = 775mVrms
Xtal/Clock Frequency = 3.579545MHz

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Current			-	0.6	1.0	mA
Input Logic "1"			0.7	-	-	%V_{DD}
Input Logic "0"			-	-	0.3	%V_{DD}
Output Logic "1"			0.8	-	-	%V_{DD}
Output Logic "0"			-	-	0.2	%V_{DD}
Impedance						
CS and PURS Input			10.0	-	-	MΩ
Hold Input		1	0.5	-	-	MΩ
Signal Input			0.1	-	-	MΩ
IRQ Output (logic "1")			-	30.0	100	kΩ
IRQ Output (logic "0")			-	175	500	Ω
Q0 - Q3 & Data-Change Outputs (logic "1")			-	0.7	2.0	kΩ
Q0 - Q3 & Data-Change Outputs (logic "0")			-	175	500	Ω
Q0 - Q3 & Data-Change Outputs (high Z)			1.0	-	-	MΩ
Dynamic Values						
Signal Input Range		2, 5	35.0		1,166	mVrms
Decode Bandedge Tolerance		3	-1.0	-	1.0	%
Xtal Inverter						
Voltage Gain			20.0	-	-	V/V
Input Impedance			10.0	-	-	MΩ
Output Impedance			-	-	160	kΩ
Decoder Timing - *Figures 3 and 4*						
Power Up Reset Time	t_{PURS}		2.5	-	-	ms
Data 'E' Time	t_{DE}		31.0	-	-	ms
NOTONE to Tone Response Time	t_{RESP}	4	-	27.0	50.0	ms

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480091.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Characteristics		See Note	Min.	Typ.	Max.	Unit
Tone to NOTONE Response Time	t_{NT}	4	-	-	60.0	ms
Data to Data-Change Pulse Time	t_{DC}		0.625	-	1.15	ms
Data-Change Pulse Width	t_{PUL}		-	1.25	-	ms
Hold to Data-Change Rise Time	t_{HOLD}		63.0	-	-	µs
HOLD to Data-Change Fall Time	t_{NORM}		-	-	150	µs
IRQ Tone Response Time	t_{RIRQ}		-	29.0	52.0	ms
IRQ Reset Time	t_{IR}		-	-	250	ns
Data Access Time	t_{ACS}		-	-	250	ns
CS High to Output Tri-State Time	t_{HIZ}		-	-	100	ns

Notes
1. This pin has an on-chip 1.0MΩ pullup resistor.
2. An a.c. coupled sine or squarewave.
3. See Table 1, Tone Decode Frequencies.
4. Delay between the change of input (TONE/NOTONE) and the change at the Q0 - Q3 outputs.
5. The signal input maximum value is determined by the formula $V_{DD}/2.83$.



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 16-pin PDIP Mechanical Outline: *order as part no. MX623P*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480091.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

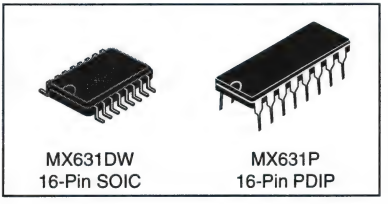
MX•COM, INC. MiXed Signal ICs

DATABULLETIN

MX631 LOW VOLTAGE SPM DETECTOR

Features

- Detects 12 & 16kHz SPM Frequencies
- Low Power (3.0 $Volt_{MIN}$ <1.0mA) Operation
- High Speechband Rejection Properties
- Tone-Follower and Packet Mode Outputs
- Applications
  - •Complex and/or Simple Telephone Systems
  - •Call-Charge/-Logging Systems



MX631DW
16-Pin SOIC

MX631P
16-Pin PDIP

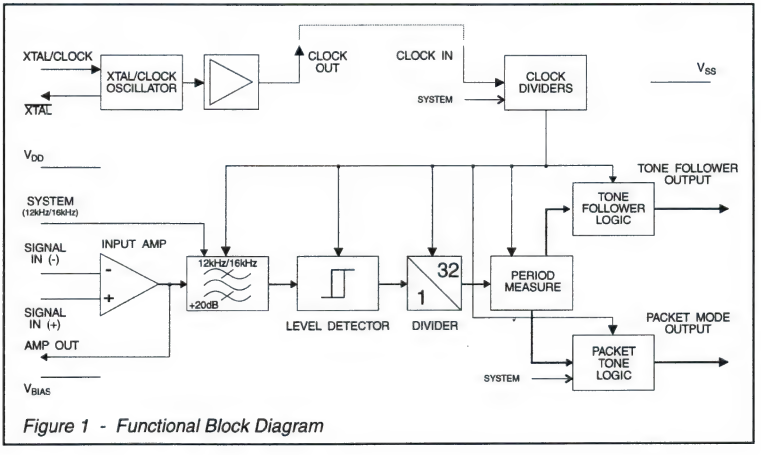


Figure 1 - Functional Block Diagram

Description

The MX631 is a low-power, system-selectable Subscriber Pulse Metering (SPM) detector that indicates the presence of both 12kHz or 16kHz telephone call-charge frequencies on a telephone line.

Deriving its input directly from the telephone line, input amplitude/sensitivities are component adjustable to the user's national 'Must/Must-Not Decode' specifications via an on-chip input amplifier, while the 12kHz and 16kHz frequency limits are accurately defined by the use of an external 3.579545MHz telephone-system Xtal or clock-pulse input.

The MX631, which demonstrates high 12kHz and 16kHz performance in the presence of both voice and noise, can operate from either a single or differential analog signal input from which it will produce two individual logic outputs:

1. Tone Follower Output - A 'tone-following' logic output producing a "Low" level for the period of a correct decode and a "High" level for a bad decode or NOTONE.
2. Packet (Cumulative Tone) Mode Output - To respond and/or de-respond after a cumulative 40ms of good tone (orNOTONE) in any 48ms period. This process will ignore small fluctuations or fades of a valid frequency input and is available for µProcessor 'Wake-Up', Minimum Tone detection, NOTONE indication or transient avoidance.

This system (12kHz/16kHz) selectable integrated circuit, which may be line-powered, is available in 16-pin plastic DIP and SOIC surface mount packages.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc.#20480087.003
All trademarks and service marks are held by their respective companies

Pin	Function
1	**Xtal/Clock :** The input to the on-chip clock oscillator; for use with a 3.579545MHz Xtal in conjunction with the Xtal output (see Figure 2). Circuit components are on-chip. Using this mode of clock operation, the Clock Out pin should be connected directly to the Clock In pin. If a clock pulse input is employed to the Clock In pin, this pin must be connected directly to V_{DD} (see Figure 2).
2	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator inverter.
3	**Clock Out:** The buffered output of the on-chip clock oscillator inverter. If a Xtal input is employed this output should be connected directly to the Clock In pin.
4	**Clock In:** The 3.579545MHz clock pulse input to the internal clock-dividers. In the clock pulse input mode the Xtal/Clock input (pin 1) should be connected to V_{DD}. (See Figure 2.)
5	No internal connection, leave open circuit.
6	No internal connection, leave open circuit.
7	**V_{BIAS}:** The output of the on-chip analog bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} (see Figure 2).
8	**V_{SS}:** Negative supply (GND).
9	**Signal In (+):** The positive and negative inputs to, and the output from, the input gain adjusting signal amplifier. Refer to Figure 4 for guidance on setting level sensitivities to national specifications, and the selection of gain adjusting components.
10	**Signal In (-):**
11	**Amp Out:**
12	No internal connection, leave open circuit.
13	**Tone Follower Output:** This output provides a logic "0" (Low) for the period of a detected tone and a logic "1" (High) for NOTONE detection. See Figure 5.
14	**Packet Mode Output:** A logic output that will be available after a cumulation of 40ms of 'good' tone has been received. This packet tone follower will only respond when a tone frequency of sufficient quality has been received for sufficient time, i.e. a cumulation of 40ms in any 48ms; short tone bursts or breaks will be ignored. This output provides a logic "0" (Low) for a detected tone and a logic "1" (High) for NOTONE detection. See Figure 6.
15	**System:** The logic input to select device operation to either 12kHz (logic "1" - High) or 16kHz (logic "0" - Low) SPM systems. This input has an internal 1MΩ pullup resistor (12kHz).
16	**V_{DD}:** Positive supply. A single, stable power supply is required. Critical levels and voltages within the MX631 are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin. Note that if this device is 'line' powered, the resulting supply must be stable. See notes on IC Protection from high and spurious line voltages.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.#20480087.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Application Information: External Components

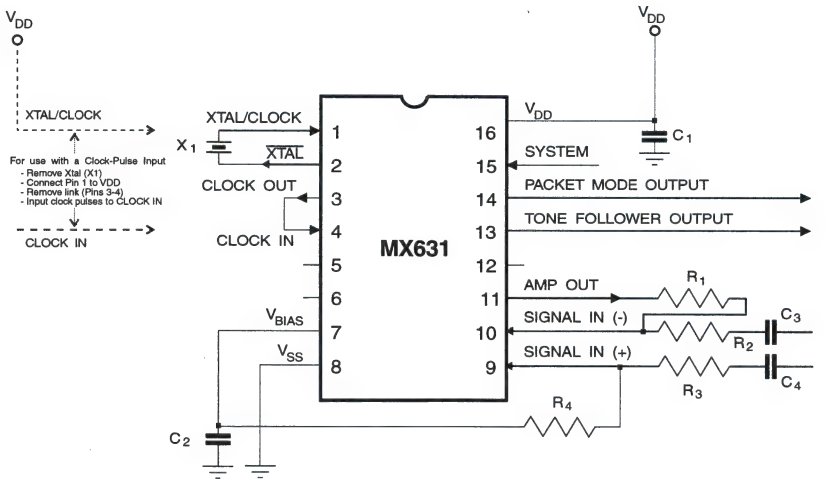


Figure 2 - Recommended External Components - Differential Input Mode

Component	Value
R_1	$R_{FEEDBACK}$
R_2	$R_{IN(-)}$
R_3	$R_{IN(+)}$
R_4	R_{BIAS}
C_1	1.0µF ±20%
C_2	1.0µF ±20%
C_3	$C_{IN(-)}$
C_4	$C_{IN(+)}$
X_1	3.579545MHz

External Components

1. The values of the Input Amp gain components illustrated are calculated using the Input Gain Calculation Graph (Figure 4).
   When calculating input gain components, for correct operation, it is recommended that the values of resistors R_1 and R_4 do not go below 100kΩ.

2. Refer to following pages for advice on IC Protection from high and spurious line voltages.

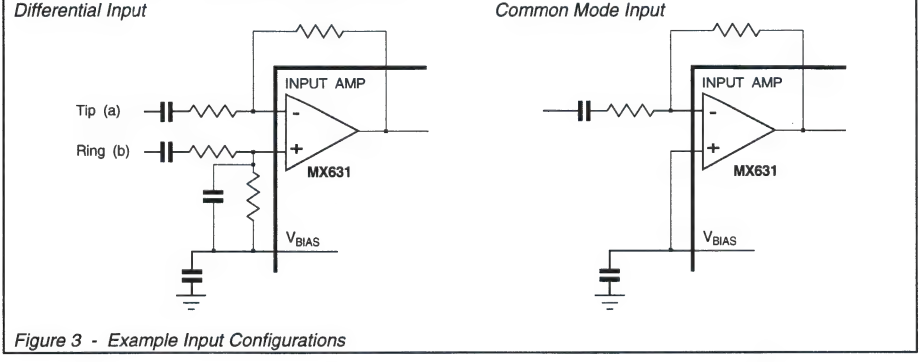


Figure 3 - Example Input Configurations

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.#20480087.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Application Information .....

Application Information .....

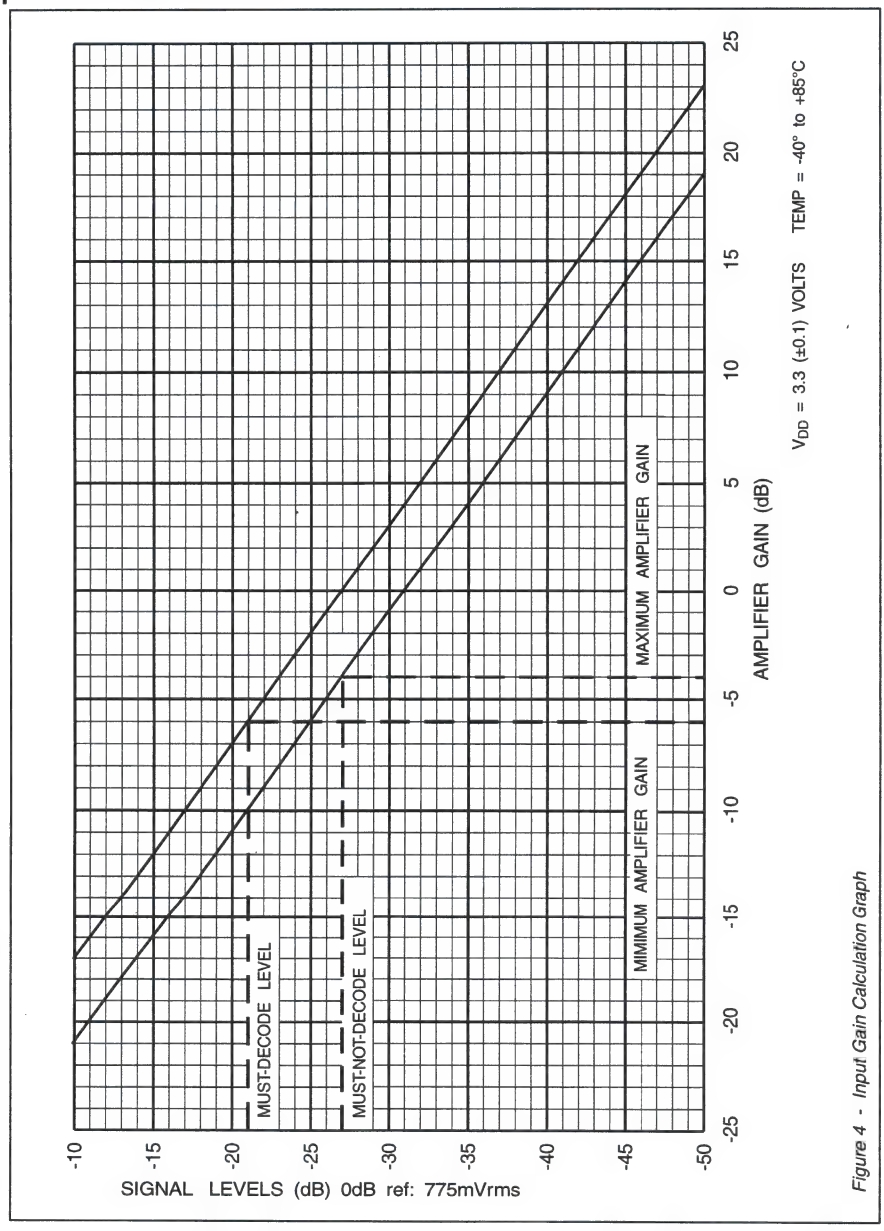


Figure 4 - Input Gain Calculation Graph

© 1997 MX-COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc.#20480087.003
All trademarks and service marks are held by their respective companies

Application Information .....

Input Gain Calculation

The input amplifier, with its external circuitry, is provided on-chip to set the sensitivity of the MX631 to conform to the user's national level specification with regard to 'Must' and 'Must-Not' decode signal levels.

With reference to Figure 4, the following steps will assist in the determination of the required gain/ attenuation.

Step 1

Draw two horizontal lines from the Y-axis (Signal Levels (dB)). The upper line represents your required 'Must' decode level. The lower line represents your required 'Must-Not' decode level.

Step 2

Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis (Amplifier Gain (dB)).

The point where the vertical line meets the X-axis indicates the MINIMUM Input Amp gain required for reliable decoding of valid signals.

Step 3

Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis.

The point where the vertical line meets the X-axis indicates the MAXIMUM allowable Input Amp gain.

Input signals at or below the 'Must-Not' decode level will not be detected as long as the amplifier gain is no higher than this level.

Input Gain Components

The following paragraphs refer to the gain components shown in Figures 2 and 3.

The user should calculate and select external components (R_1, R_2/C_3, R_3/C_4, R_4) to provide an amplifier gain within the limits obtained in Steps 2 and 3.

Component tolerances should not move the gain-figure outside these limits.

It is recommended that the designed gain is near the center of the calculated range. The graph in Figure 4 is for calculations for the input gain components for an MX631 using a V_{DD} of 3.3 (±0.1) volts.

Use this area to keep a permanent record of your calculated gains and components

Implementation Notes

Aliasing

Due to the switched-capacitor filters employed in the MX631, be careful to avoid the effects of alias distortion with the external components you choose.

Possible Alias Frequencies:
12kHz Mode= 52kHz
16kHz Mode= 69kHz

If these alias frequencies are liable to cause problems and/or interference, it is recommended that anti-alias capacitors are used across input resistors R_1 and R_4.

Values of anti-alias capacitors should be chosen to provide a highpass cutoff frequency, in conjunction with R_1 (R_4) of approximately 20kHz to 25kHz (12kHz system) or 25kHz to 30kHz (16kHz system).

$$\text{i.e. } C = \frac{1}{2 \times \pi \times f_0 \times R_1}$$

When anti-alias capacitors are used, make allowance for reduced gain at the SPM frequency (12kHz or 16kHz).

Signal Input Protection

Telephone systems may have high d.c. and a.c. voltages present on the line. If the MX631 is part of host equipment that has its own signal input protection circuitry, there will be no need for further protection as long as the voltage on any pin is limited to within V_{DD} + 0.3V and V_{SS} -0.3V.

If the host system does not have input protection, or there are signals present outside the device's specified limits, the MX631 will require protection diodes at its signal inputs (+ and -). The breakdown voltage of capacitors and the peak inverse voltage of the diodes must be sufficient to withstand the sum of the d.c. voltages plus all expected signal peaks.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.#20480087.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} +0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage temperature range	-40°C to +85°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 3.3V

T_{AMB} = +25 °C

Audio Level 0dB ref: = 775mVrms

Noise Bandwidth = 50kHz

Xtal/Clock or 'Clock In' Frequency = 3.579545MHz

12kHz or 16kHz System Setting

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD}) at 25°C		3.0	-	5.5	V
Supply Current		-	-	1.0	mA
Input Logic "1" (High)		2.3	-	-	V
Input Logic "0" (Low)		-	-	1.0	V
Output Logic "1" (High)		2.9	-	-	V
Output Logic "0" (Low)		-	-	0.4	V
Xtal/Clock or Clock In Frequency		3.558918	-	3.589368	MHz
"High" External Clock Pulse Width		0.1	-	-	µs
"Low" External Clock Pulse Width		0.1	-	-	µs
Input Amp					
D.C. Gain		60.0	-	-	dB
Bandwidth (-3dB open loop)		-	100	-	Hz
Input Impedance		-	1.0	-	MΩ
Logic Impedances					
Input (System)		0.7	-	3.8	MΩ
(Clock In)		10.0	-	-	MΩ
Output		-	14.0	30.0	kΩ
Overall Performance					
12kHz Detect Bandwidth	1	11.820		12.180	kHz
12kHz Not-Detect Frequencies (below 12kHz)	1	-	-	11.520	kHz
12kHz Not-Detect Frequencies (above 12kHz)	1	12.480	-	-	kHz
16kHz Detect Bandwidth	1	15.760		16.240	kHz
16kHz Not-Detect Frequencies (below 16kHz)	1	-	-	15.360	kHz
16kHz Not-Detect Frequencies (above 12kHz)	1	16.640	-	-	kHz
Sensitivity	2	7.8	10.0	15.5	mVp-p
Tone Operation Characteristics					
Signal-to-Noise Requirements (Amp Input)	3,4,5,6	22.0	20.0	-	dB
Signal-to-Voice Requirements (Amp Input)	3,4,5,7	-36.0	-40.0	-	dB
Signal-to-Voice Requirements (Amp Output)	5,6	-25.0	-	-29.0	dB
Tone Follower Output					
Response and De-Response Times	1,8	-	-	10.0	ms
Packet Mode Output					
Response and De-Response Times	1,8	40.0	-	48.0	ms

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies
Doc.# 20480087.003

Characteristics Notes

1. With adherence to Signal-to-Voice and Signal-to Noise specifications.
2. With Input Amp gain setting: $15.5dB_{MIN}/19.5dB_{MAX}$.
3. Common Mode SPM and balanced voice signal.
4. Immune to false responses.
5. Immune to false de-responses
6. With SPM and voice signal amplitudes balanced; To avoid false de-responses due to saturation, the peak-to-peak voice+noise level at the output of the Input Amp (12/16kHz Filter Input) should be no greater than the dynamic range of the device.
7. Maximum voice frequencies = 3.4kHz
8. Response, De-Response and Power-up Response Timing.

Application Information .....

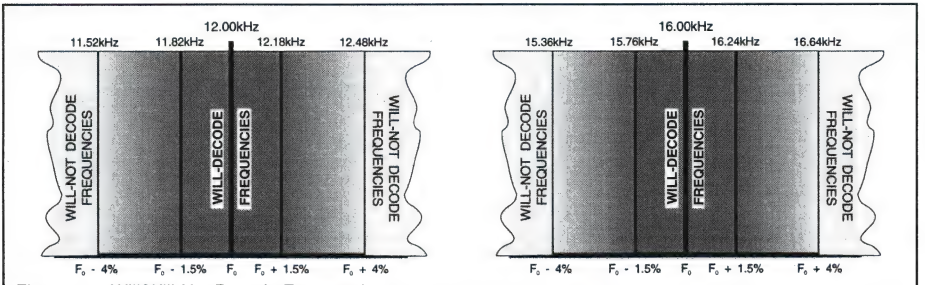


Figure 5 - Will/Will-Not Decode Frequencies

System Timing

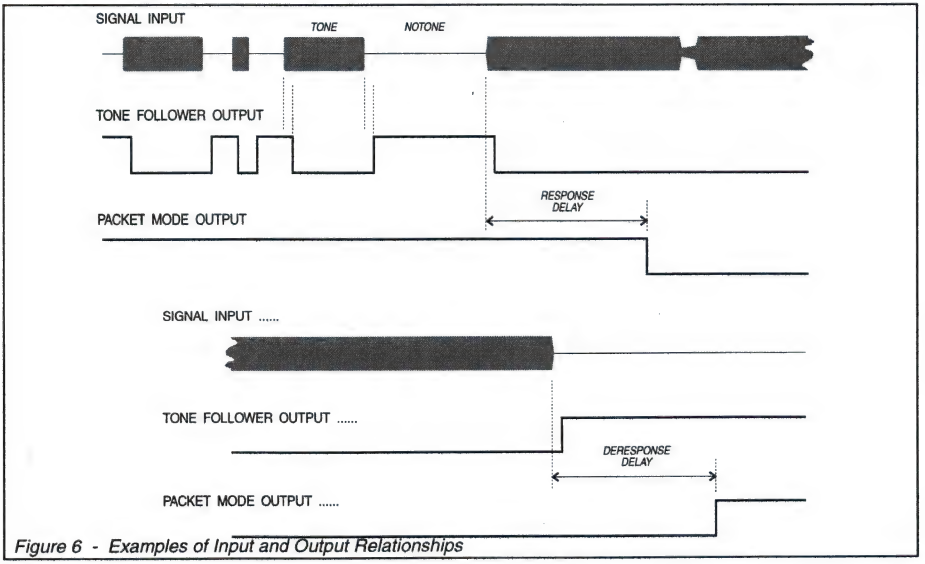
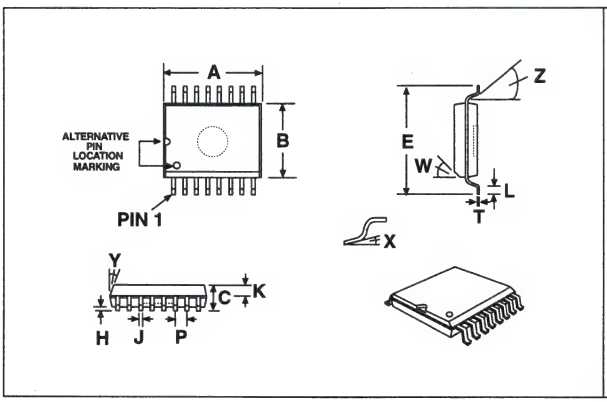


Figure 6 - Examples of Input and Output Relationships

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480087.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

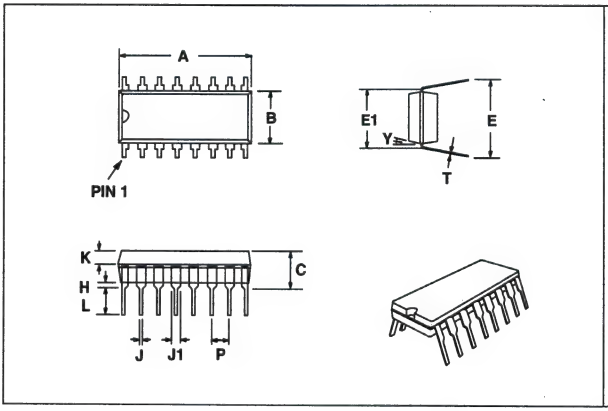


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure7: 16-pin SOIC Mechanical Outline: order as part no. MX631DW



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure7: 16-pin PDIP Mechanical Outline: order as part no. MX631P

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc.# 20480087.003
All trademarks and service marks are held by their respective companies

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX633 Call Progress Tone Detector

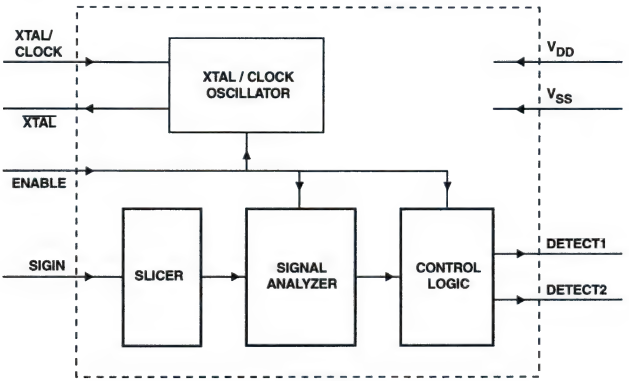
PRELIMINARY INFORMATION

Features

- **Worldwide Tone Compatibility**
- **Single and Dual Tones Detected**
- **U.S. Busy-Detect Output**
- **Voice-Detect Output**
- **Wide Dynamic Range > 40dBm**
- **Low Supply Current (0.3mA/0.5mA)**
- **Low Supply Voltage (3.3V/5.0V)**
- **Standard 3.58MHz Xtal**

Applications

- **Automatic Calling Products**



The MX633 is a low cost, low power device that uses signal processing techniques to detect audible tone signals such as Dial, Ringing, Busy and other conditions found when placing a call throughout the world's telecom systems. Detection of these call progress stages is essential to the proper operation of automatic calling products.

The MX633 adds new features to Call Progress monitoring. It detects and indicates the 'U.S. Busy' tones, reducing the need to measure 'tone cadence' to identify 'U.S. Busy'. It also detects and indicates voice and other signals from Call Progress tones, reducing voice-falsing and adding voice-answer as a connection prompt.

The MX633 may be used with a 3.0V to a 5.5V supply and is available in the following package styles: 8-pin PDIP (MX633P) and 16-pin SOIC (MX633DW).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480135.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

CONTENTS

Section ..... **Page**

1. Block Diagram **2-91**

2. Signal List **2-92**

3. External Components **2-93**

4. General Description **2-94**

4.1 Glossary 2-94

4.2 Overall Function Description 2-94

4.3 Block Diagram Description (Reference Figure 1) 2-94

4.3.1 Slicer 2-94

4.3.2 Signal Analyzer 2-94

4.3.3 Control Logic 2-95

4.3.4 Xtal/Clock Oscillator 2-95

4.4 Decode Output Truth Table 2-95

5. Performance Specification **2-95**

5.1 Electrical Performance 2-95

5.1.1 Absolute Maximum Ratings 2-95

5.1.2 Operating Limits 2-96

5.1.3 Operating Characteristics 2-96

5.1.4 Timing 2-97

5.2 Packaging 2-99

MX•COM, Inc. reserves the right to change specifications at any time and without notice

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480135.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Block Diagram

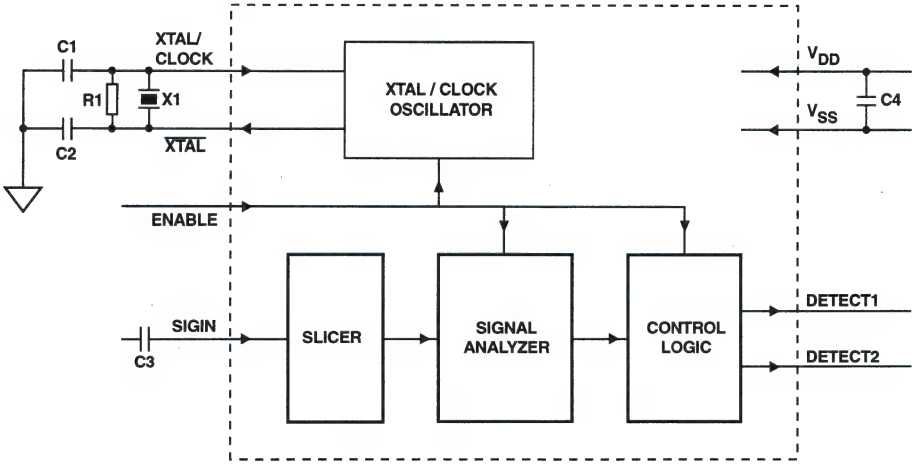


Figure 1: Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480135.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Signal List

Package / Pin No.		Signal	Type	Description
P	DW			
1	2	XTAL/CLOCK	input	Input to the on-chip oscillator, for external Xtal circuit or clock
2	3	$\overline{XTAL}$	output	Output of the on-chip oscillator inverted
3	5	ENABLE	input	A logic 1 applied to this input enables the decoder and detection outputs. A logic 0 pulse of at least 1µs applied to this input resets the decoder circuits and forces both DETECT1 and DETECT2 outputs to a logic 0.
4	7	DETECT1	output	When a Call Progress signal is detected, DETECT1 output state changes to a logic 1
5	10	SIGIN	input	Signal input. Signals to this pin should be ac coupled. The dc bias of this pin is set internally.
6	12	V_{SS}	power	Negative supply
7	13	DETECT2	output	Output used in conjunction with DETECT1. When a Call Progress High Band signal is detected and DETECT1 output state is a logic 1, then DETECT2 output state changes to a logic 1. When a Non Call Progress signal is detected and DETECT1 output state is a logic 0, then DETECT2 output state changes to a logic 0.
8	15	V_{DD}	power	Positive supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

Table 1: Signal List

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480135.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

External Components

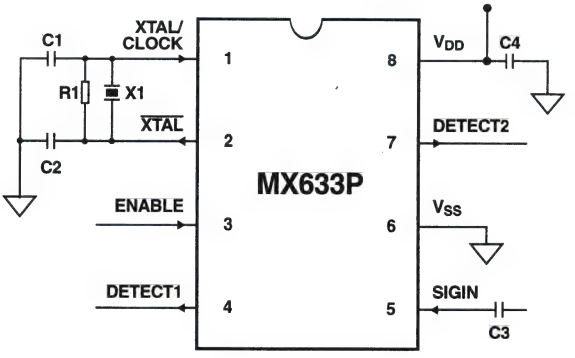


Figure 2: Recommended External Components

R1		1 MΩ	±10%
C1		33pF	±20%
C2		33pF	±20%
C3		560pF at 3.3V_{DD} 1nF at 5.0V_{DD}	±20%
C4		1.0µF	±20%
X1	Note 1	3.579545MHz	refer to sec.0

Table 2: Recommended External Components

Notes:

1. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480135.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

General Description

The following Glossary and Decode Truth Table (found in section 0), describe the MX633 decoding features and functions.

Glossary

Call Progress Tones: The single and dual frequency tones in the range 350Hz to 620Hz specified widely for call progress signaling.

Call Progress Band: The nominal range 340Hz to 650Hz within which the MX633 will detect Call Progress tones. The detection algorithm requires that the tones have the characteristics typical of Call Progress Tones.

Call Progress Low Band: The nominal range 340Hz to 490Hz. The MX633 will detect single or dual tones falling entirely within this range as Call Progress Low Band tones.

Call Progress High Band: The nominal range 600Hz to 650Hz. Single tones in this range, or dual tones (e.g. 480 + 620Hz), having a material frequency component within this range are detected as Call Progress High Band tones.

Non Call Progress Signal: A signal falling within the nominal range (a) 200Hz to 800Hz, but NOT within the Call Progress Band, or (b) within the nominal range 200Hz to 800Hz, but NOT meeting the detection requirements when the signal falls in the Call Progress Band.

Subject to the duration and other characteristics of such signals, the MX633 will usually interpret this as a Non Call Progress Signal (e.g. speech or other signal activity).

Minimum Input Signal: The minimum signal level for the specified tone decoding performance.

No Signal: A signal falling outside the nominal range 120Hz to 900Hz or the absence of an input signal. Either will be detected as a No Signal condition.

Nominal: Subject to dynamic tolerances within the signal analysis process. Absolute values are not material or adverse to performance.

Overall Function Description

The MX633 Call Progress Tone Detector uses tone detection methods different from those methods commonly found in other Call Progress Tone Detectors.

Many Call Progress Tone Detectors use a bandpass filter followed by an energy detector. The filter is usually designed to pass input signals with a frequency between about 300Hz and 700Hz. Each signal amplitude in this range is checked against a level threshold. Any signal of acceptable level in this frequency band is classified as a Call Progress tone, including speech and noise signals. False outputs caused by speech are commonly indicated by such products and background noise may lead to a stuck detect output.

In contrast, the MX633, uses a stochastic signal processing technique. This technique is based on analysis of both the frequency and time domains, with signal amplitude forming a small part in the decision process. This analysis includes checks on whether the signal has a profile that matches international standards for Call Progress tones, speech, noise or other Non-Call-Progress signals. It also checks for U.S. Busy signal tones.

Block Diagram Description (Reference Figure 1)

Slicer

The input signal to the slicer is amplified by a self-biased inverting amplifier. The dc bias of this input is internally set at $V_{DD}/2$.

Signal Analyzer

The frequency range, quality and consistency of the input signal is analyzed by this functional block. To be classified as a call progress signal, the input signal frequencies should lie between 340Hz and 650Hz. The signal to noise ratio must be 16dB or greater and the signal must be consistent over a period of about 140 ms. This decode criteria is continuously monitored and the assessment updated every 7 ms, reference Figure 3.

The Signal Analyzer samples the call progress signal at 9.3kHz. Care should be taken to avoid high frequency signals (≥ 8.4kHz) aliasing into the call progress band.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480135.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Control Logic

This block categorizes the nature of the signal into various decode output states and controls the two output pins. See Table 3.

Xtal/Clock Oscillator

If the on-chip Xtal oscillator is to be used, then external components X1, R1, C1 and C2 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin and the $\overline{XTAL}$ pin should be left unconnected.

Decode Output Truth Table

DETECT2	DETECT1	CONDITIONS
0	0	No Signal
0	1	Call Progress Low Band: Will detect 350+440, 400+450, 440+480,400, 425, 440, and 450Hz tones
1	1	Call Progress High Band: Will detect 480+620, 600 and 620Hz tones
1	0	Non Call Progress signal, e.g. voice activity

Note:

1. DETECT1 responds to the entire range of call progress tones from 340Hz to 650Hz.

Table 3: Decode Output Truth Table

Performance Specification

Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW / DIP Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480135.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} – V_{SS})		3.0	5.5	V
Xtal Frequency		3.57	3.59	MHz

Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz, S/N = 16 dB, Noise Bandwidth = 5 kHz,
V_{DD} = 3.3V to 5.0V, V_{SS} = 0V, T_{AMB} = 25°C, 0dB = 775mV_{RMS}.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
Supply Current					
I_{DD} (ENABLE = 1) (V_{DD} = 5.0V)	1		0.5	1.0	mA
I_{DD} (ENABLE = 1) (V_{DD} = 3.3V)	1		0.3	0.7	mA
Enable Input					
Input Logic 1 Level	2	80%			V_{DD}
Input Logic 0 Level	2			20%	V_{DD}
Input Leakage Current (V_{IN} = 0 to V_{DD})	2	-5.0		5.0	µA
Input Capacitance	2		10.0		pF
Detect Output					
Output Logic 1 Level (I_{OH} = 120µA)	3	90%			V_{DD}
Output Logic 0 Level (I_{OL} = 360µA)	3			10%	V_{DD}
AC Parameters					
SIGIN pin					
Input Impedance (from 100Hz to 2kHz at 5.0V)	4		350		kΩ
Input Signal Level	5		-40		dB
Input Signal Dynamic Range	5	40			dB
Signal to Noise Ratio		16			dB
Xtal/Clock Oscillator					
'High' Input Pulse Width	6	40			ns
'Low' Input Pulse Width	6	40			ns
Input Impedance (at 100Hz)		10			MΩ
Gain (input = 1mV_{RMS} at 100Hz)		20			dB

Operating Characteristics Notes:

1. Not including any current drawn from the device pins by external circuitry.
2. ENABLE pin.
3. DETECT1 and DETECT2 pins.
4. Small signal impedance over the frequency range 100Hz to 2000Hz and at 5.0V
5. The input level is not critical as the detector uses a stochastic algorithm.
6. Timing for an external input to the XTAL/CLOCK pin.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480135.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Timing

For the following conditions unless otherwise specified:
Xtal Frequency = 3.579545MHz, V_{DD} = 3.3V to 5.0V, T_{AMB} =25°C, S/N = 20dB

Timing (ref. Figures 3, 4, 5 and 6)		Notes	Min.	Typ.	Max.	Units
t_I	Call Progress Burst Length Ignored				70	ms
t_L	Burst Length Detected		145			ms
t_{GI}	Call Progress Tone Gap Length Ignored	1			20	ms
t_{GD}	Call Progress Tone Gap Length Detected	1	40			ms
t_{RP}	Call Progress Tone Response Time	2			145	ms
t_{DRP}	Call Progress Tone De-response Time				145	ms
t_{GDR}	Gap Detected Recorded	3	6			ms
t_{NG}	Non Call Progress Signal Gap Length Ignored	4		80		ms
t_{NRP}	Non Call Progress Signal Response Time		145			ms
t_{NDRP}	Non Call Progress Signal De-response Time			80		ms
t_{CH}	State Change		0			ms
t_V	DETECT1 and DETECT2 Response Time	5			145	ms

Timing Notes:

1. Only applies to bursts of the same frequency.
2. For dual tones in 16dB SNR the Response Time may be longer.
3. To acknowledge a short tone gap ≥ 40 ms, No Signal is indicated for a minimum of 6ms.
4. If the gap > 90 ms, a No Signal state will be decoded.
5. Time between a stable XTAL/CLK and a valid DETECT1 and DETECT2 state when ENABLE is high.

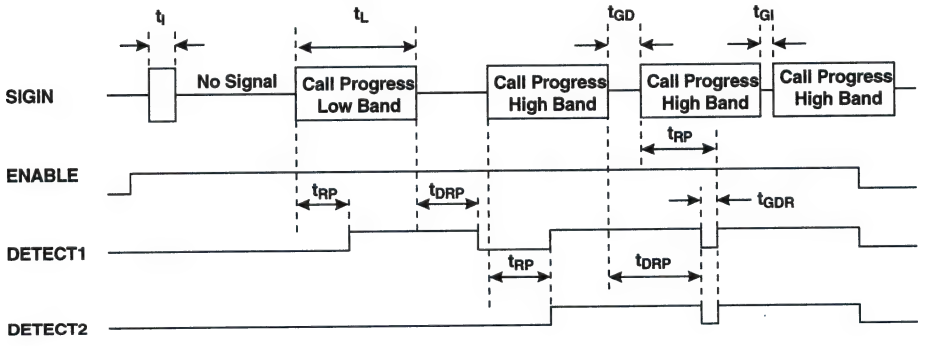


Figure 3: Timing Diagram: Call Progress Tone (s)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480135.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

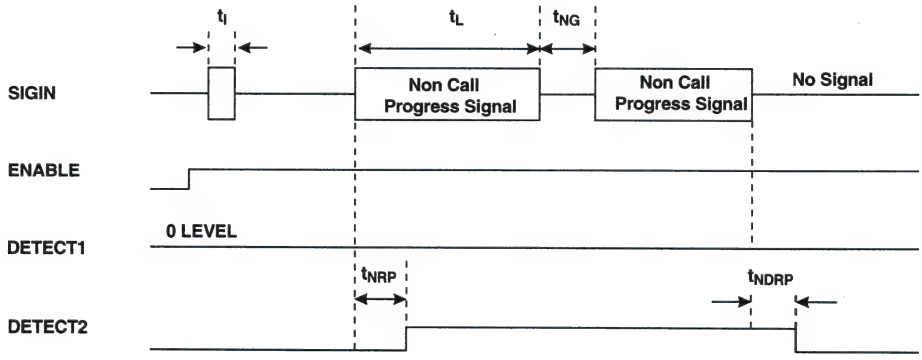


Figure 4 : Timing Diagram: Non Call Progress Signal

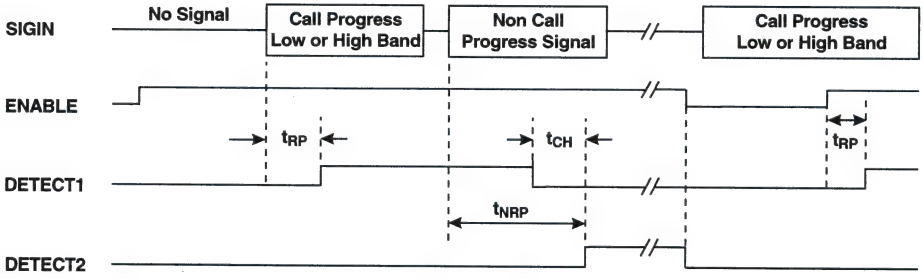


Figure 5 : Timing Diagram: Call Progress Tone (s) to Non Call Progress Signal

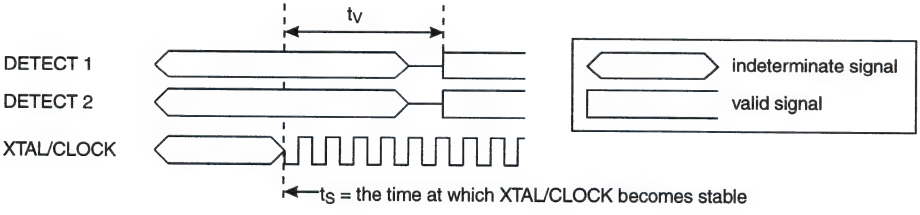
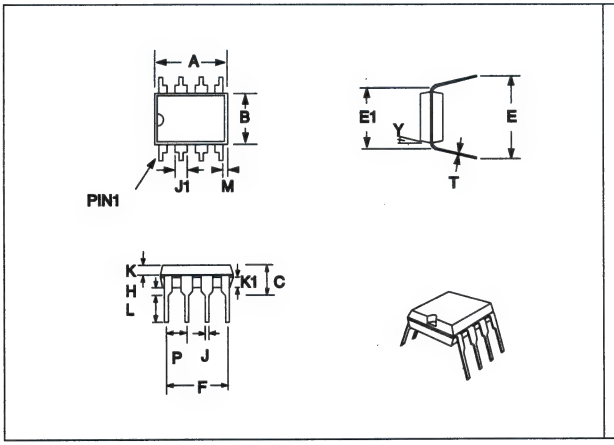


Figure 6: Timing Diagram: DETECT 1 and DETECT 2 Response Time when ENABLE is high

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480135.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Packaging

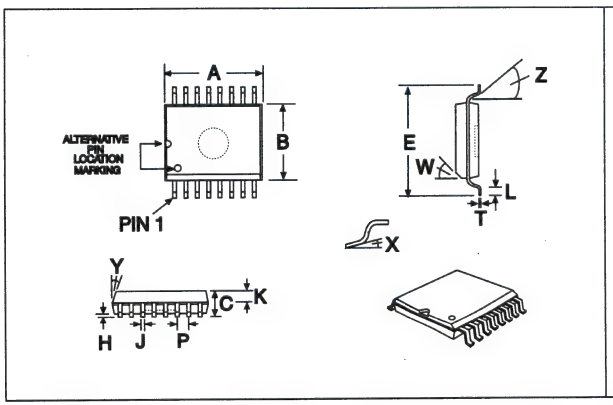


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.346 (8.790)		0.400 (10.16)
B	0.240 (6.10)		0.260 (6.60)
C	0.145 (3.68)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.87).
E1	0.290 (7.37)		0.325 (8.22)
F		0.30 (7.62)	
H	0.015 (0.38)		0.040 (1.01)
J	0.015 (0.38)		0.023 (0.58)
J1	0.045 (1.14)		0.065 (1.65)
K		0.060 (1.52)	
K1		0.060 (1.52)	
L	0.121 (3.07)		0.150 (3.81)
M	0.020 (0.51)		0.033 (0.84)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7 : 8-pin PDIP Mechanical Outline: *Order as part no. MX633P*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8 : 16-pin SOIC Mechanical Outline: *Order as part no. MX633DW*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480135.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX641 Dual SPM Detector

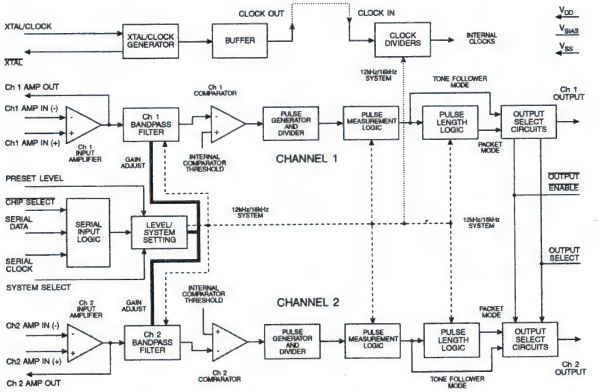
PRELIMINARY INFORMATION

Features

- **Two (12kHz / 16kHz) SPM Detectors on a Single Chip**
- **Detects 12 or 16kHz SPM Frequencies**
- **'Controlled' (μC) & 'Fixed' Signal Sensitivity Modes**
- **Selectable Tone Follower or Packet Mode Outputs**
- **High Speech-Band Rejection Properties**
- **'Output Enable' Multiplexing Facility**

Applications

- **Call Charge Applications on PABX Line Cards**
- **Remote Telephone Applications**



The MX641 is a low-power, system-selectable Dual Subscriber Pulse Metering (SPM) Detector designed to indicate the presence, on a telephone line, of either 12kHz or 16kHz telephone call-charge frequencies. It is designed for PBX and PABX line-card and remote telephone installations. Under μProcessor control via a common serial interface, each channel of the MX641 will detect call-charge pulses from a telephone line and provide a digital output for recording, billing or security purposes. A common set of external components and a stable 3.579545MHz Xtal/clock input ensures that the MX641 adheres accurately to most national "Must and Must-Not" decode band-edges and threshold levels. For non-μProcessor systems a preset sensitivity/system input allows external channel level and system setting

The digital output is pin-selectable to one of three modes:

(1) Tone Follower mode: logic level for the period of a correct decode.
(2) Packet mode: respond/de-respond after a cumulative period of tone or notone in a fixed (intrinsic hardwired period that is not user controlled) period.
(3) High-impedance output: for device multiplexing.

The MX641 requires a 5V supply and is available in the following packages: 24-pin SOIC (MX641DW) and 24-pin PDIP (MX641P).

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480115.002
All trademarks and service marks are held by their respective companies.

CONTENTS

Section **Page**

1. Block Diagram 2-103

2. Signal List 2-104

3. External Components 2-106

4. General Description 2-107

4.1 Xtal/Clock Distribution 2-107

4.2 Channel Outputs 2-107

4.3 Sensitivity Setting 2-108

4.3.1 Controlled Sensitivity Setting 2-108

4.3.2 Fixed Sensitivity Setting 2-111

5. Applications 2-112

5.1.1 Input Configurations 2-112

5.1.2 Protection Against High Voltages 2-112

5.1.3 Aliasing 2-113

6. Performance Specification 2-113

6.1 Electrical Specifications 2-113

6.1.1 Absolute Maximum Ratings 2-113

6.1.2 Operating Limits 2-113

6.1.3 Operating Characteristics 2-113

6.2 Timing 2-115

6.3 Packages 2-116

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1. Block Diagram

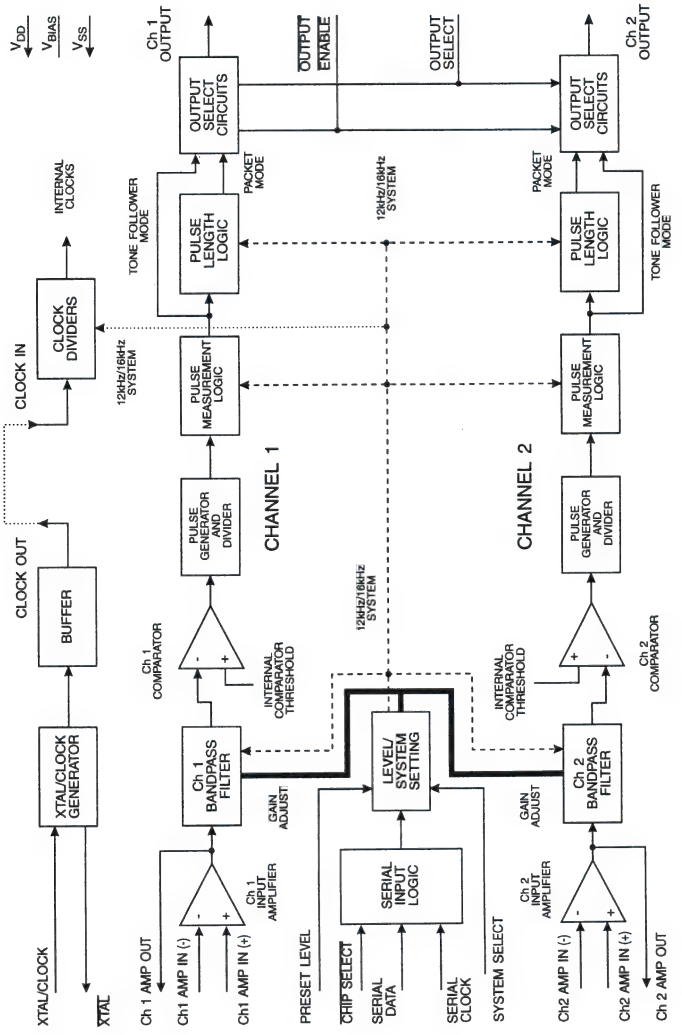


Figure 1: Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. Signal List

Pin No.	Name	Type	Description
1	Xtal/Clock	input	The input to the on-chip clock oscillator; for use with a 3.579545MHz Xtal in conjunction with the Xtal output; circuit components are on-chip. When using a Xtal input, the Clock Out pin should be connected directly to the Clock In pin. If a clock pulse input is used at the Clock In pin, this (Xtal/Clock) pin must be connected directly to V_{DD} (see Figure 2). See Figure 3 for details of clock frequency distribution.
2	$\overline{XTAL}$	output	The output of the on-chip clock oscillator inverter.
3	Clock Out	output	The buffered output of the on-chip-clock oscillator inverter. If a Xtal input is used, this output should be connected directly to the Clock In pin. This output can support up to 3 additional MX641 ICs. See Figure 3 for details of clock frequency distribution.
4	Clock In	input	The 3.579545 clock pulse input to the internal clock dividers. If an externally generated clock pulse input is used, the Xtal/Clock input pin should be connected to V_{DD}.
5	$\overline{\text{Output Enable}}$	input	For multi-chip output multiplexing; controls the state of both Ch1 and Ch2 outputs. When this input is placed high (logic '1') both outputs are set to a high impedance. When placed low (logic '0') both outputs are enabled.
6	Ch 2 Output	output	The digital output of the Channel 2 SPM detector when enabled. The format of the signal at this pin, in common with Ch 1, is selectable to either 'Tone Follower' or 'Packet' mode via the Output Select input.
7	Ch 1 Output	output	The digital output of the Channel 1 SPM detector when enabled. The format of the signal at this pin, in common with Ch 2, is selectable to either 'Tone Follower' or 'Packet' mode via the Output Select input.
8	V_{BIAS}	power	The output of the on-chip analog bias circuitry. Held internally at $V_{DD}/2$, this pin should be decoupled to V_{SS} (see Figure 2).
9	Ch 1 Amp Out	output	The output of the Channel 1 Input Amplifier. See Figure 2 and Figure 8.
10	Ch 1 Amp In (-):	input	The negative input to the Channel 1 Input Amplifier. See Figure 2 and Figure 8.
11	Ch 1 Amp In (+):	input	The positive input to the Channel 1 Input Amplifier. See Figure 2 and Figure 8.
12	V_{SS}	power	Negative supply (GND).
13	N/C		No internal connection; leave open circuit.
14	Ch 2 Amp In (+):	input	The positive input to the Channel 2 Input Amplifier. See Figure 2 and Figure 8.
15	Ch 2 Amp In (-):	input	The negative input to the Channel 2 Input Amplifier. See Figure 2 and Figure 8.
16	Ch 2 Amp Out	output	The output of the Channel 2 Input Amplifier. See Figure 2 and Figure 8.
17	Output Select	input	A logic input to set the Channel 1 and Channel 2 output modes. When high (logic '1'), the outputs are in the Tone Follower mode; when low (logic '0'), the outputs are in the Packet mode.
18	Preset Level	input	A logic input to set the sensitivity mode of the MX641. When high (logic '1'), both channels are in the Fixed Sensitivity mode. The external components govern the input sensitivity; the System Select input selects 12kHz or 16kHz operation. When low (logic '0'), both channels are in the Controlled Sensitivity mode. Device sensitivities and system selection are via the Chip Select/Serial Data/Serial Clock inputs. This input has an internal pullup resistor on chip (Fixed Sensitivity Mode).
19	$\overline{\text{Chip Select}}$	input	The Chip Select input for use in data loading when using the MX641 in the Controlled Sensitivity mode (see Figure 9). The device is selected when this input is set low (logic '0'). When the MX641 is in the Fixed Sensitivity mode this input should be connected to either V_{SS} or V_{DD}.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Pin No.	Name	Type	Description
20	Serial Clock	input	The Serial Clock input for use in data loading when using the MX641 in the Controlled Sensitivity mode (see Figure 9). Data is loaded to the MX641 on this clock's rising edge. When the MX641 is in the Fixed Sensitivity mode this input should be connected to either V_{SS} or V_{DD}.
21	Serial Data	input	The Serial Data input for use in data loading when using the MX641 in the Controlled Sensitivity mode (see Figure 9 and Table 4). When the device is in the Fixed Sensitivity mode this input should be connected to either V_{SS} or V_{DD}.
22	System Select	input	In the Fixed Sensitivity mode this pin selects the system frequency. High (logic '1') = 12kHz; Low (logic '0') = 16kHz. In the Controlled Sensitivity mode this pin is inactive and may be left unconnected. This pin has an internal pullup resistor on chip.
23	N/C		No internal connection; leave open circuit.
24	V_{DD}	power	Positive supply rail; a single, stable power supply is required. Critical levels and voltages within the MX641 are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin

Table 1: Signal List

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components

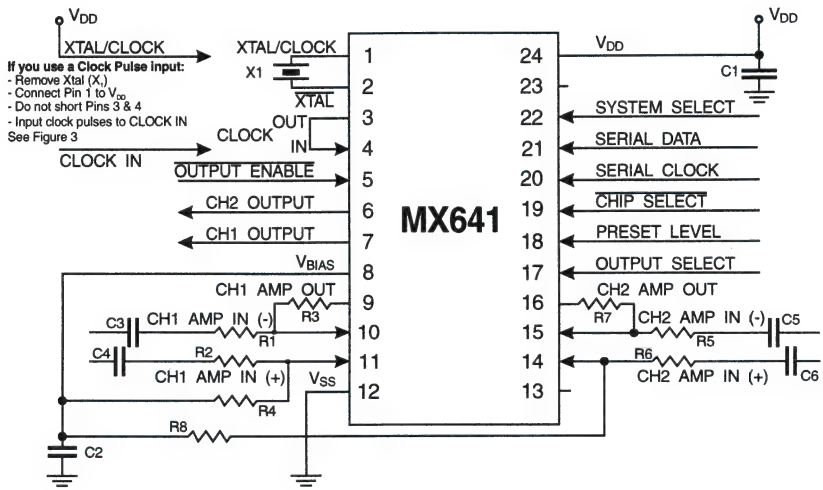


Figure 2: Recommended External Components

R1		68kΩ	± 1%
R2		68kΩ	±1%
R3	Note 1	750kΩ	±1%
R4	Note 1	750kΩ	±1%
R5		68kΩ	± 1%
R6		68kΩ	± 1%
R7	Note 1	750kΩ	±1%
R8	Note 1	750kΩ	±1%

C1		1.0µF	±20%
C2		1.0µF	±20%
C3		270pF	±5%
C4		270pF	±5%
C5		270pF	±5%
C6		270pF	±5%
X1	Note 2, 3	3.579545MHz	

Table 2: Recommended External Components

Note:

1. Fixed Sensitivity Setting: when calculating/selecting gain components, R3, R4, R7 and R8 should always be greater than or equal to 100kΩ.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
3. The on-chip crystal circuitry includes a feedback resistor (nominally 2MΩ) between pins 1 & 2 and load capacitors on pins 1 & 2 (nominally 10pF each, excluding package and board parasitics).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4. General Description

4.1 Xtal/Clock Distribution

The MX641 requires a 3.579545MHz Xtal or clock pulse input. With the exception of the Xtal, all oscillator components are incorporated on chip. If a Xtal input is employed the Clock Out pin should be directly linked to the Clock In pin.

To reduce component and layout complexity, the clock requirements of up to 3 additional MX641 microcircuits may be supplied from a Xtal-driven MX641 acting as the system master clock. With reference to Figure 3, the clock should be distributed as illustrated and the Xtal/Clock pins of the driven microcircuits should be connected directly to V_{DD}.
Note (see section 6.1.3) that the maximum load on the master Clock Out pin should not be exceeded.

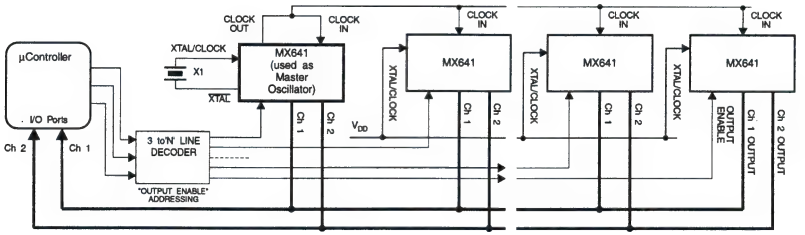


Figure 3: Xtal/Clock Distribution and Output Multiplexing

4.2 Channel Outputs

Channel 1 and Channel 2 outputs operate together under the control of the Output Enable and Output Select inputs. Table 3 describes the operations.

The digital output is pin-selectable to one of three modes:

(1) Tone Follower mode: a logic level for the period of a correct decode.
(2) Packet mode: respond/de-respond after a cumulative period of tone or notone in a fixed (intrinsic hardwired period that is not user controlled) period.
(3) High-impedance output: for device multiplexing.

System Select	Preset Level	Output Select	Output Enable	Operating Mode		
				Mode	Sensitivity	Frequency
X	0	0	0	Packet Mode Output;	Serial Data Control (see note)	
X	0	1	0	Tone Follower Output;	Serial Data Control (see note)	
0	1	0	0	Packet Mode Output;	Fixed Sensitivity	16kHz
1	1	0	0	Packet Mode Output;	Fixed Sensitivity	12kHz
0	1	1	0	Tone Follower Output;	Fixed Sensitivity	16kHz
1	1	1	0	Tone Follower Output;	Fixed Sensitivity	12kHz
X	X	X	1	Tristate Output (High Z)		

X = don't care

Note: Device sensitivity and system frequency must be serially loaded

Table 3: Operating Mode Configuration

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

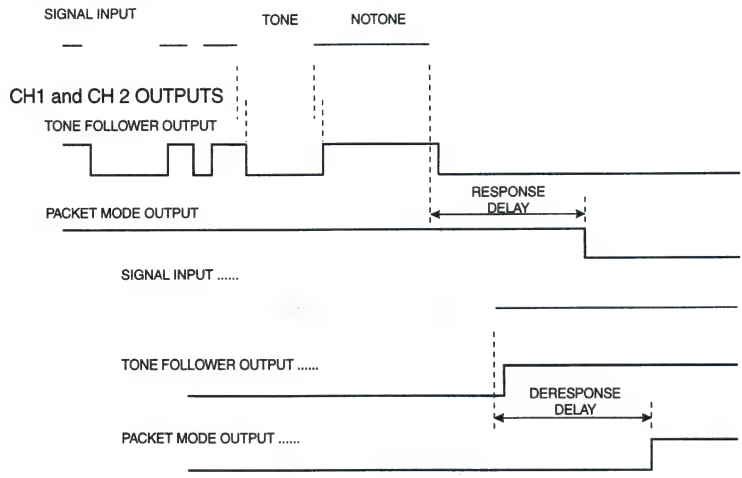


Figure 4: Tone Follower and Packet Mode Outputs

4.3 Sensitivity Setting

To enable the MX641 to operate correctly to most national 12kHz and 16kHz SPM specifications, the input sensitivity can be accurately adjusted and set.

There are two different pin-selectable modes of sensitivity setting available to the MX641: Controlled Sensitivity Mode and Fixed Sensitivity Mode

The Controlled Sensitivity mode allows the sensitivity setting from a µController via a 6-bit serial data input. This same serial input also sets operation (bit 0) to either 12kHz or 16kHz systems. Both channels are set identically.

The Fixed Sensitivity mode allows the sensitivity of each channel to be set to a fixed "gain" by external components at the input amplifiers. Operation to either 12kHz or 16kHz is by the System Select input.

4.3.1 Controlled Sensitivity Setting

With the external gain (sensitivity) components used as shown in Figure 2, the gain of the input stages is 19.8dB (12kHz) or 20.5dB (16kHz). For controlled sensitivity setting the gain of each bandpass filter, and therefore the device sensitivity, is adjusted by the applied serial bits D1 to D5.

In the Controlled Sensitivity mode the system frequency is selected by bit D0 ('1' = 12kHz; '0' = 16kHz). Data is loaded Bit 5 (D5) first. Table 4 details the serial data inputs for the required sensitivity. Minimum, Nominal and Maximum Sensitivity figures are provided to make complete allowance for internal circuit offsets and component tolerances. 0dB(ref.) = 775mV_{RMS} at V_{DD} = 5.0 volts; varies directly with V_{DD}.

Note: Device sensitivity is directly proportional to V_{DD}

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.3.1.1 Controlled Sensitivity Setting Information

The sensitivity figures in Table 4 are based on the following:

1. The recommended amplifier components (see Figure 2) are used, providing an amplifier gain at 16kHz of 19.8dB ±0.3dB or at 12kHz of 19.1dB ±0.3dB.
2. A comparator sensitivity of 1.6dB(ref.) ±1dB (the variation is due to filter gain error, filter output offset, comparator input offset or a combination of all 3).
3. The applied V_{DD} is 5.0 volts; 0dB (ref.) = 775mV_{RMS}.

		12kHz System Bit D0 = '1'			16kHz System Bit D0 = '0'		
Serial Data Bits	**Bandpass Filter Gain**	**Minimum Sensitivity**	**Nominal Sensitivity**	**Maximum Sensitivity**	**Minimum Sensitivity**	**Nominal Sensitivity**	**Maximum Sensitivity**
D5 - D1	(dB)	dB(ref.)	dB(ref.)	dB(ref.)	dB(ref.)	dB(ref.)	dB(ref.)
00000	0	-16.2	-17.5	-18.8	-16.9	-18.2	-19.5
00001	1.0	-17.2	-18.5	-19.8	-17.9	-19.2	-20.5
00010	2.0	-18.2	-19.5	-20.8	-18.9	-20.2	-21.5
00011	3.0	-19.2	-20.5	-21.8	-19.9	-21.2	-22.5
00100	4.0	-20.2	-21.5	-22.8	-20.9	-22.2	-23.5
00101	5.0	-21.2	-22.5	-23.8	-21.9	-23.2	-24.5
00110	6.0	-22.2	-23.5	-24.8	-22.9	-24.2	-25.5
00111	7.0	-23.2	-24.5	-25.8	-23.9	-25.2	-26.5
01000	8.0	-24.2	-25.5	-26.8	-24.9	-26.2	-27.5
01001	9.0	-25.2	-26.5	-27.8	-25.9	-27.2	-28.5
01010	10.0	-26.2	-27.5	-28.8	-26.9	-28.2	-29.5
01011	11.0	-27.2	-28.5	-29.8	-27.9	-29.2	-30.5
01100	12.0	-28.2	-29.5	-30.8	-28.9	-30.2	-31.5
01101	13.0	-29.2	-30.5	-31.8	-29.9	-31.2	-32.5
01110	14.0	-30.2	-31.5	-32.8	-30.9	-32.2	-33.5
01111	15.0	-31.2	-32.5	-33.8	-31.9	-33.2	-34.5
10000	16.0	-32.2	-33.5	-34.8	-32.9	-34.2	-35.5
10001	17.0	-33.2	-34.5	-35.8	-33.9	-35.2	-36.5
10010	18.0	-34.2	-35.5	-36.8	-34.9	-36.2	-37.5
10011	19.0	-35.2	-36.5	-37.8	-35.9	-37.2	-38.5
10100	20.0	-36.2	-37.5	-38.8	-36.9	-38.2	-39.5
10101	21.0	-37.2	-38.5	-39.8	-37.9	-39.2	-40.5
10110	22.0	-38.2	-39.5	-40.8	-38.9	-40.2	-41.5
10111	23.0	-39.2	-40.5	-41.8	-39.9	-41.2	-42.5
11000	24.0	-40.2	-41.5	-42.8	-40.9	-42.2	-43.5
11001	25.0	-41.2	-42.5	-43.8	-41.9	-43.2	-44.5
11010	26.0	-42.2	-43.5	-44.8	-42.9	-44.2	-45.5
11011	27.0	-43.2	-44.5	-45.8	-43.9	-45.2	-46.5
11100 11101 11110 11111	These states should never be used. If sensitivities of this order are required (e.g. the Swedish Rural SPM specification), it is recommended that the Controlled Sensitivity setting be set to 20dB (10100) and external components selected to set the Input Amp gain to a higher figure. This action will prevent falsing by sub-harmonic frequencies.						

Table 4: Controlled Sensitivity Setting Information

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.3.1.2 German FTZ Specification (16kHz)

The FTZ system has a Must Decode level of -21dB (ref.) and a Must-Not Decode level of -27dB (ref.). Reference to Table 4 shows that Bandpass Filter Gain settings of 5dB, 6dB or 7dB will enable an MX641 channel to meet this level specification. Figure 5 illustrates the range of these various settings.

To meet the German FTZ specification, the input data (D5 to D0) must be:

	0 0 1 0 1	0	5.0dB
or	0 0 1 1 0	0	6.0dB
or	0 0 1 1 1	0	7.0dB

Note:

1. By selecting the middle setting, the greatest noise immunity is achieved.

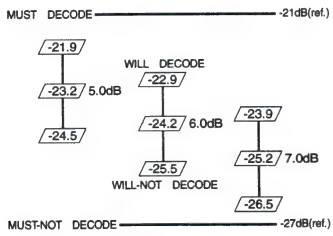


Figure 5: German Specification - Possible Settings

4.3.1.3 French Specification (12kHz)

This system has a Must Decode level of -17.36dB (ref.) and a Must-Not Decode level of -23.8dB (ref.). Reference to Table 4 shows that Bandpass Filter Gain settings of 2dB, 3dB or 4dB will enable an MX641 channel to meet this level specification. Figure 6 illustrates the range of these various settings.

To meet the French SPM specification, the input data (D5 to D0) must be:

	0 0 0 1 0	1	2.0dB
or	0 0 0 1 1	1	3.0dB
or	0 0 1 0 0	1	4.0dB

Note:

1. By selecting the middle setting, the greatest noise immunity is achieved.

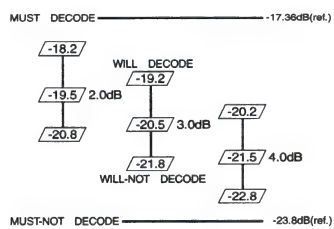


Figure 6: French Specifications - Possible Settings

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.3.2 Fixed Sensitivity Setting

In this mode the sensitivity of each channel is set by the correct selection of the components around the Channel Input Amplifier. Note that the device sensitivity is directly proportional to the applied power supply (V_{DD}).

4.3.2.1 Input Gain Calculation

The input amplifier, with external circuitry, is used to set the sensitivity of the MX641 to conform to the user's national level specification with regard to 'Must' and 'Must-Not' decode signal levels.

With reference to the graph in Figure 7, the following steps will assist in the determination of the required gain/attenuation.

Step 1 Draw two horizontal lines from the Y-axis (Signal Level) in Figure 7. The upper line represents the required 'Must' decode level. The lower line represents the required 'Must-Not' decode level

Step 2 Mark the intersection of the upper horizontal line and the upper sloping line; drop a vertical line from this point to the X-axis (Amplifier Gain (dB)). The point where the vertical line meets the X-axis indicates the minimum Input Amp gain required for reliable decoding of valid signals

Step 3 Mark the intersection of the lower horizontal line and the lower sloping line; drop a vertical line from this point to the X-axis. The point where the vertical line meets the X-axis will indicate the maximum allowable Input Amp gain. Input signals at or below the 'Must-Not' decode level will not be detected as long as the amplifier gain is no higher than this level.

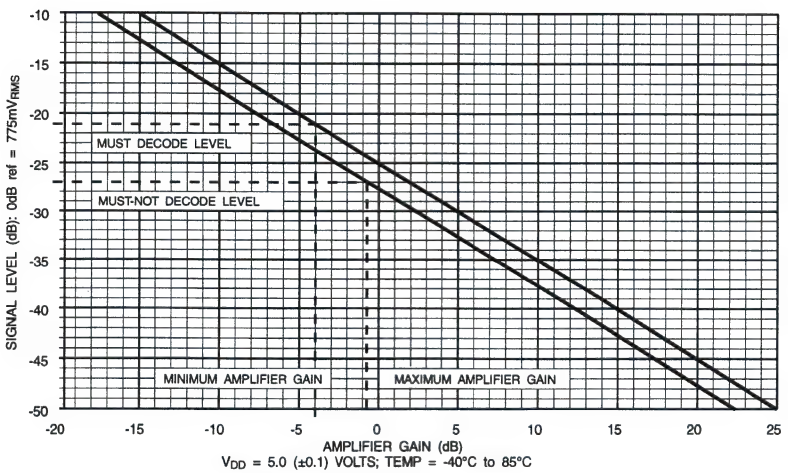


Figure 7: Input Gain Calculation Graph for use in the Fixed Sensitivity Mode

4.3.2.2 Input Gain Components

Refer to the gain components shown in Figure 2. The user should calculate and select external components (R1/R3/C3, R2/R4/C4 and R5/R7/C5, R6/R8/C6) to provide amplifier gains within the limits obtained in Steps 2 and 3.

Component tolerances should not move the gain-figure outside these limits. The graph in Figure 7 is for the calculation of input gain components for an MX641 using a V_{DD} of 5.0 (±0.1) volts.

It is recommended that the designed gain is near the center of the calculated range.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. Applications

5.1.1 Input Configurations

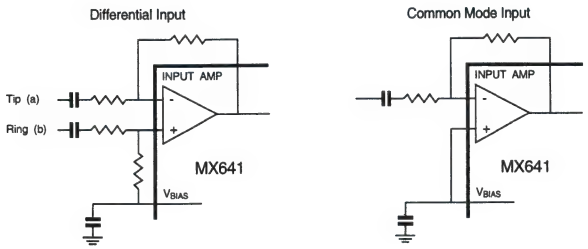


Figure 8: Input Configurations

5.1.2 Protection Against High Voltages

Telephone systems may have high d.c. and a.c. voltages present on the line. If the MX641 is part of a host equipment that has its own signal input protection circuitry, there will be no need for further protection as long as the voltage on any pin is limited to within V_{DD} +0.3V and V_{SS} -0.3V.

If the host system does not have input protection, or there are signals present outside the device's specified limits, the MX641 will require protection diodes at its signal inputs (+ and -). The breakdown voltage of capacitors and the peak inverse voltage of the diodes must be sufficient to withstand the sum of the d.c. voltages plus all expected signal peaks.

5.1.3 Aliasing

Due to the sampling nature of switched-capacitor filters used in the MX641, high frequency noise or unwanted signals can alias into the passband, disrupting detection. External components must be chosen carefully to avoid alias effects.

Possible Alias Frequencies:

12kHz Mode = 52kHz

16kHz Mode = 69kHz

If other filtering in the system has not attenuated these alias frequencies, capacitors should be employed across resistors R3, R4, R7 and R8 to provide anti-alias filtering.

The low-pass cutoff frequency should be chosen to be approximately 20kHz to 25kHz for a 12kHz system, or 25kHz to 30kHz for a 16kHz system.

$$\text{i.e. } C = \frac{1}{2 \times \pi \times f_0 \times R3}$$

When anti-alias capacitors are used, an allowance must be made for reduced gain at the SPM frequency (12kHz or 16kHz).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6. Performance Specification

6.1 Electrical Specifications

6.1.1 Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage.

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD}-V_{SS})	-0.3		7.0	V
Voltage on any pin to V_{SS}	-0.3		(V_{DD} + 0.3)	V
Current				
V_{DD}	-30		30	mA
V_{SS}	-30		30	mA
Any other pin	-20		20	mA
DW / P Packages				
Total allowable device dissipation at T_{AMB} 25°C			800	mW
Derating above T_{AMB} 25°C			10	mW/°C above T_{AMB} 25°C
Operating Temperature	-40		85	°C
Storage Temperature	-40		85	°C

6.1.2 Operating Limits

Correct Operation of the device outside these limits is not implied.

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD})	4.5	5.0	5.5	V
Operating Temperature	-40		85	
Xtal/Clock Frequency	3.558918		3.589368	MHz

6.1.3 Operating Characteristics

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V @ T_{AMB} = 25°C
Audio Level 0dB (ref.) = 775mV_{RMS}, Noise Bandwidth = 50kHz
Xtal/Clock Frequency = 3.579545MHz, System Setting = 12kHz or 16kHz

	Notes	Min.	Typ.	Max.	Units
Supply Current			2.0	5.0	mA
Input/Output Parameters					
Clock Out Load	17			15.0	pF
Logic Inputs					
Input Logic '1' (High)		3.5			V
Input Logic '0' (Low)				1.5	V
Input Leakage Current (V_{IN} = 0 to V_{DD})	13	-5.0		5.0	µA
Input Current (V_{IN} = 0)	14	-15.0			µA

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

		Notes	Min.	Typ.	Max.	Units
Channel Outputs						
Output Logic '1'	I_{OH} = 120mA (Enabled)	1	4.6			V
Output Logic '0'	I_{OL} = 360mA (Enabled)	1			0.4	V
Output Leakage Current	High-Z Output	2	-5.0		5.0	µA
Input Amplifier						
D. C. Gain			60.0			dB
Bandwidth (-3dB)				100		Hz
Input Impedance			1.0			MΩ
Overall Performance						
12kHz Detect Bandwidth		3	11.82		12.18	kHz
12kHz Not-detect Frequencies	(Below 12kHz)	3			11.52	kHz
12kHz Not-detect Frequencies	(Above 12kHz)	3	12.48			kHz
16kHz Detect Bandwidth		3	15.76		16.24	
16kHz Upper Decode Band Edge	(Below 16kHz)	3			15.36	kHz
16kHz Lower Decode Band Edge	(Above 16kHz)	3	16.64			kHz
Level Sensitivity						
Controlled Sensitivity Mode		3,4,12,15	2.6	1.6	0.6	dB(ref.)
Preset Sensitivity Mode		3,4,5,16	-25.4	-26.4	-27.4	dB(ref.)
Signal Quality Requirements						
Signal-to-Noise	(Amp Input)	4,8,9,10	22.0	20.0		dB
Signal-to-Voice	(Amp Input)	4,8,9,11	-36.0	-40.0		dB
Signal-to-Voice	(Amp Output)	4,8,10,11	-1.0		-27.0	dB
Channel Outputs	(Ch1 and Ch2) Figure 4					
Mode Change Time		6			500	ns
Tone Follower Mode (Table 3)						
Response and De-Response Time		3, 4, 7			10.0	ms
Packet Mode (Table 3)						
Response and De-Response Time		3, 4, 7	40.0		48.0	ms

Note:

1. Tone Follower or Packet mode enabled; see Table 3
2. Tristate selected; see Table 3.
3. With adherence to Signal-to-Voice and Signal-to Noise specifications.
4. 12kHz and/or 16kHz system.
5. With Input Amp gain setting = 0dB.
6. Time taken to change between any two of the operational modes: Tone Follower, Packet or Tristate, and with a maximum capacitive load of 30pF on an output.
7. The time delay, after a valid serial data load (or after device powerup), before the condition of the outputs can be guaranteed correct.
8. Immunity to false responses and/or de-responses.
9. Common Mode SPM and balanced voice input signal.
10. With SPM and voice signal amplitudes balanced; to avoid false de-responses due to saturation, the peak-to-peak voice + noise level at the output of the Input Amp should be no greater than the dynamic range of the device. For this reason, the signal-to-voice figure at the AMP Output will vary with the sensitivity setting. The lowest signal-to-voice figure occurs at the highest sensitivity setting. (Table 4 27dB)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

11. Maximum voice frequencies = 3.4kHz.
12. With the Input Amplifier gain at 0dB and the Bandpass Filter gain set at 0dB (Table 4); subtract 1.0dB from this specification for each extra single dB of Bandpass Filter gain programmed.
    Alternatively, with the input components as recommended in Figure 2, the sensitivity is as defined in Table 4.
13. Logic inputs with no internal pullup; Chip Select, Serial Data, Serial Clock, Output Enable, Output Select and Clock In pins.
14. Logic inputs with an internal pullup; Preset Level and System Select pins.
15. Preset Level = '0', System Select = don't care; Chip Select, Serial Clock and Serial Data inputs active; see Table 3.
16. Preset Level = '1', System Select = input active; Chip Select, Serial Clock and Serial Data inputs inactive; see Table 3
17. Maximum Clock Output Fan out = 4 (including master)

6.2 Timing

Parameter		Min.	Typ.	Max.	Unit
t_{PWH}	Serial Clock 'High' Pulse Width	250			ns
t_{PWL}	Serial Clock 'Low' Pulse Width	250			ns
t_{CYC}	Serial Clock Period	600			ns
t_{CSE}	Chip Select 'Low' to Clock 'High' Edge	450			ns
t_{DH}	Data Hold Time	50.0			ns
t_{DS}	Data Setup Time	250			ns

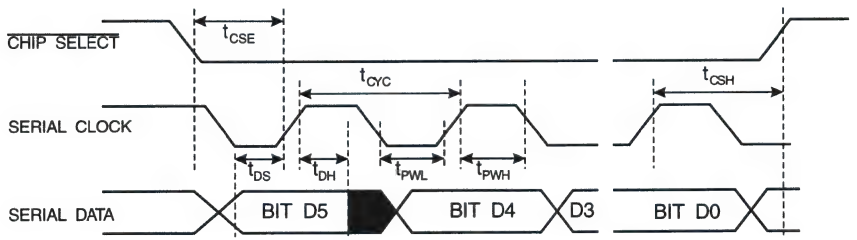
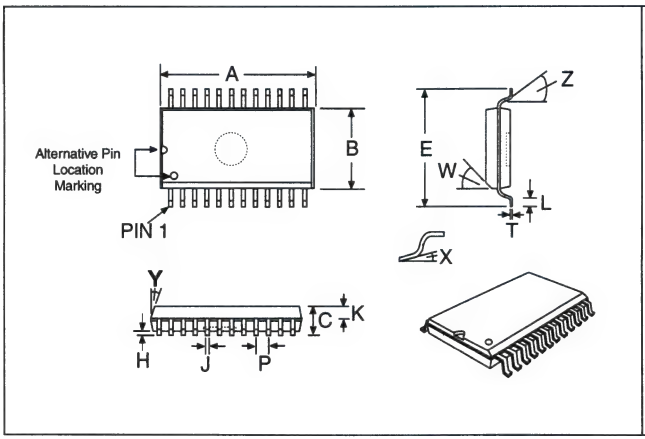


Figure 9: Data Load Timing for the Controlled Sensitivity Mode

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.3 Packages

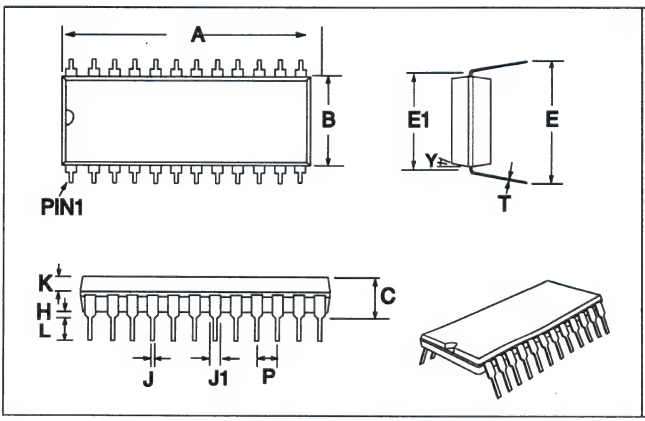


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin SOIC Mechanical Outline: order as part no. MX641DW



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 24-pin PDIP Mechanical Outline: order as part no. MX641P

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480115.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

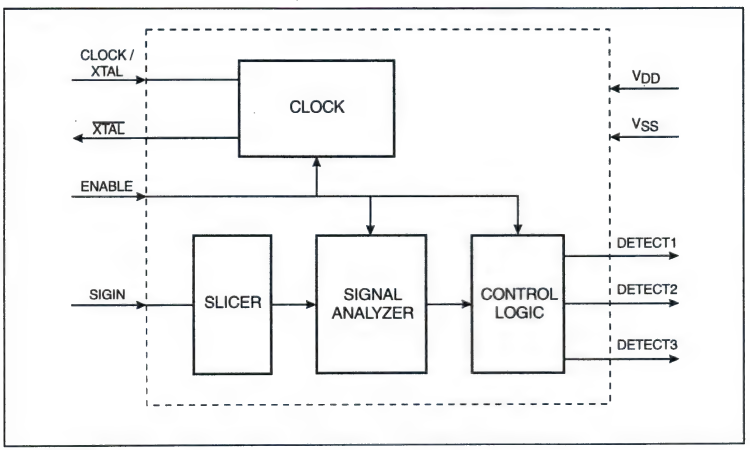
MX643

Call Progress Tone Detector with Special Information Tones (SIT)

Document #20480148.001 May 1996

Preliminary Information

- **International Special Information Tone Identification**
- **Worldwide Tone Compatibility**
- **Single and Dual Tone Detected**
- **U.S. Busy-Detect Output**
- **Voice-Detect Output**
- **Wide Dynamic Range > 40dBm**
- **- 40°C to 85°C Operating Temp**
- **Low Supply Current (0.3mA/0.5mA)**
- **Low Supply Voltage (3.3V/5.0V)**
- **Standard 3.58MHz Clock Input**
- **Standard 8-pin DIP Package**



AVAILABLE PACKAGES

MX643P
8-pin PDIP

MX643DW
16-pin SOIC

The MX643 is a low power, low cost device that uses signal processing techniques to detect audible tone signals such as; Dial, Ring, Busy, Unobtainable, and other conditions found when placing a call throughout the world's telecom systems. The detection of these Call Progress stages is essential to the proper operation and application of automatic calling products.

The MX643 offers identification of International Special Information Tones (SIT), reducing the time needed for cadence verification under Obtainable conditions. In addition to the SIT feature, single and dual tone decoding are added for better cross-system Call Progress monitoring. The MX643 offers these features in addition to the same performance levels and features of the MX633 Call Progress Tone Detector such as; detection and identification of U.S. Busy tones, thereby reducing the need to measure the tone cadence to identify U.S. Busy. The decoding and indicating of speech, or other Non-Call Progress signals, thus reducing voice-falsing of Call Progress tones and adding Voice-Answer as a connect prompt.

Available in the industry standard 8-pin DIP, the MX643 is also available in a 16-pin SOIC making it pin compatible with the MX633DW (16-pin SOIC).

© 1996 MX•COM, INC.

Tele: 800 638 5577, 910 744 5050, Fax: 910 744 5054

CONTENTS

Section **Page**

1. Block Diagram **2-119**

2. Signal List **2-120**

3. External Components **2-121**

4. General Description **2-121**
4.1 Glossary 2-121
4.2 Overall Function Description 2-122

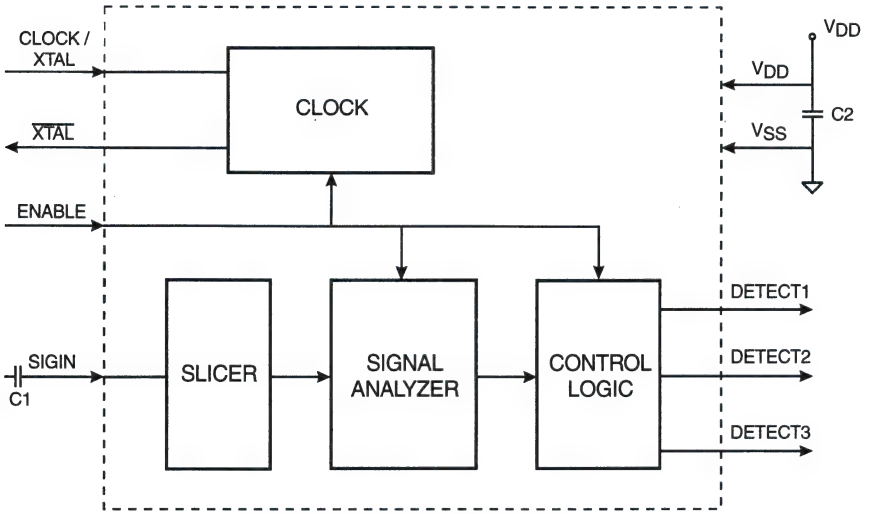
5. Block Diagram Description **2-122**
5.1 Decode Output Truth Table 2-123

6. Performance Specification **2-123**
6.1 Electrical Performance 2-123
6.2 Packaging 2-128

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050, Fax: 910 744 5054
Doc. #20480148.001

1. Block Diagram



Note: XTAL used for 16-pin SOIC (MX643DW) only.

Figure 1: Block Diagram

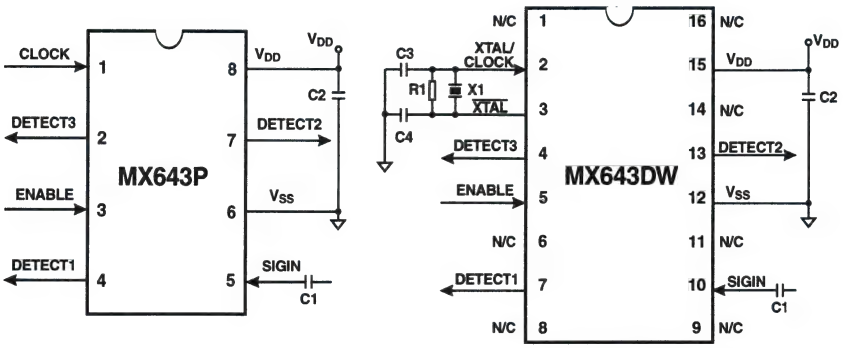
© 1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050, Fax: 910 744 5054

2. Signal List

P-Pin No.	DW-Pin No.	Signal	Type	Description
1	2	CLOCK / XTAL	input	For the MX643P this is the external clock input to the clock divider circuit. For the MX643DW this can be either an external clock input or an external crystal input.
-	3	$\overline{XTAL}$	output	Output of the on-chip oscillator. Not available on 8-pin DIP..
2	4	DETECT3	output	When a single tone is within the range of the Call Progress Band, Non Call Progress Band, or a Special Information Tone, is detected, this output goes to a logic 1.
3	5	ENABLE	input	A logic 1 applied to this input enables the decoder and detection outputs. A logic 0 applied to this input disables the decoder and forces DETECT1, DETECT2 and DETECT3 to a logic 0.
4	7	DETECT1	output	When a call progress signal is detected, this output goes to a logic 1.
5	10	SIGIN	input	Signal input. Signals to this pin should be ac coupled. The dc bias of this pin is set internally.
6	12	V_{SS}	power	Negative supply. (ground).
7	13	DETECT2	output	This output is used in conjunction with DETECT1. When DETECT1 is at a logic 1, this output goes to a logic 1 if a Call Progress High Band signal is detected. When DETECT1 is at a logic 0, this output goes to a logic 1 if a Non Call Progress signal is detected.
8	15	V_{DD}	power	Positive supply. This pin should be decoupled to V_{SS} by a capacitor.
	1, 6, 8, 9, 11, 14, 16	N/C		Internal connection. Do not make a connection to these pins.

© 1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050, Fax: 910 744 5054

3. External Components



C1	1.0nF	±20
C2	1.0µF	±20
For details of CLOCK frequency refer to Sec.6.1		

R1	1MΩ	±10
C1	560pF at 3.3V_{DD} 1.0nF at 5.0V_{DD}	±20
C2	1.0µF	±20
C3	33pF	±20
C4	33pF	±20
X1	3.579545MHz	refer to Sec. 6.1

Figure 2: Recommended External Components for Typical Applications

4. General Description

4.1 Glossary

The following glossary and Decode Truth table (found in section 5.1), describe the MX643 decoding features and functions.

Call Progress Tones: The single and dual frequency tones in the range of 350Hz to 620Hz specified widely for Call Progress signaling.

Call Progress Band: The nominal range is 340Hz to 650Hz within which the MX643 will detect Call Progress tones. The detection algorithm requires that the tones have characteristics typical of Call Progress Tones.

Call Progress Low Band: The nominal range is 340Hz to 490Hz. The MX643 will detect single or dual tones falling entirely within this range, as Call Progress Low Band tones.

Call Progress High Band: The nominal range is 600Hz to 650Hz. Single tones in this range, or dual tones having a material frequency component within this range (e.g. 480 + 620Hz), are detected as Call Progress High Band tones.

Special Information Tone: The nominal range is 950Hz or 1400Hz or 1800Hz, with a tolerance of ±50Hz.

Non Call Progress Signal: A signal falling within the nominal range (a) 200Hz to 800Hz, but NOT within the Call Progress Band, or (b) within the nominal range 200Hz to 800Hz, but NOT meeting the DETECTION REQUIREMENTS when the signal falls in the Call Progress Band.

Subject to the duration and other characteristics of such signals, the MX643 will usually interpret these as a Non Call Progress Signal (e.g. speech or other signal activity).

Minimum Input Signal: The minimum signal level for the specified tone decoding performance. The lower level at which absence of an input signal will be registered is not specified.

No Signal: A signal falling outside the nominal range of 120Hz to 900Hz or Special Information Tone or the absence of an input signal. Either will be detected as a No Signal condition.

© 1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050, Fax: 910 744 5054

Nominal: Subject to dynamic tolerances within the signal analysis process. Absolute values are not material or adverse to performance.

4.2 Overall Function Description

The MX643 Call Progress Tone Detector uses different tone detection methods from those commonly found with other Call Progress Tone Detectors.

Many traditional devices use a bandpass filter followed by an energy detector. The filter is usually designed to pass input signals with a frequency between about 300Hz and 700Hz. Each signal amplitude in this range is then checked against a level threshold. Any signal of acceptable level in this frequency band is classed as a Call Progress tone, including speech and noise. False outputs caused by speech are commonly indicated by such products and background noise may lead to a stuck detect output.

In contrast, the MX643 uses a stochastic signal processing technique. This technique is based on analysis of both the frequency and time domains, with signal amplitude forming a minor part in the decision process. This analysis includes, checks on whether the signal has a profile which matches international standards for Call Progress Tones, Special Information Tones, or a profile more likely to match that of speech, noise or other Non-Call Progress signals. Checks are also performed to see if the signal is a single tone, and whether the tones which include frequencies corresponding with the 'U.S. Busy' signals have been detected.

5. Block Diagram Description

(Reference Figure 1)

Slicer

The input signal to the slicer is amplified by a self-biased inverting amplifier. The dc bias of this input is internally set at $V_{DD}/2$.

Signal Analyzer

The frequency range, quality, and consistency of the input signal is analyzed by this function block. To be classified as a Call Progress signal the input signal frequencies should lie between 340Hz and 650Hz. To be classified as a Special Information Tone, the input signal frequency should lie between 900Hz and 1000Hz or 1350Hz and 1450Hz or 1750Hz and 1850Hz. The signal to noise ratio must be 16dB or greater. The signal must be consistent over a period of about 145 ms. These decode criteria are continuously monitored and the assessment is updated every 7 ms, reference Figure 3.

The Signal Analyzer samples the call progress signal at 9.3kHz. Care should be taken to avoid high frequency signals (≥8.4kHz) aliasing into the call progress band.

Control Logic

This block categorizes the nature of the signal into various decoded output states and controls the three output pins. See the Decode Output Truth Table in section 5.1

Clock

An external clock source is to be connected to the CLOCK input pin when using the 8-pin device. If using the on-chip oscillator (16-pin device only) you will need to use the external components shown in Figure 2. If using an external clock source then $\overline{\text{XTAL}}$ should be left unconnected.

© 1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050, Fax: 910 744 5054

5.1 Decode Output Truth Table

DETECT3	DETECT2	DETECT1	CONDITIONS
0	0	0	No Signal
1	0	0	Special Information Tone: Will detect 950, 1400 and 1800Hz tones
0	0	1	Call Progress Low Band: Will detect 350+440, 400+450 and 440+480Hz tones, for example
1	0	1	Call Progress Low Band: Will detect single 400, 425, 440, and 450Hz tones, for example
0	1	1	Call Progress High Band: Will detect 480+620Hz tones, for example
1	1	1	Call Progress High Band: Will detect single 600 and 620Hz tones, for example
0	1	0	Non Call Progress signal, e.g. Voice Activity
1	1	0	Will detect a single tone lying outside the Call Progress Band and within the Non Call Progress signal range

Decode Output Truth Table Notes:

DETECT1 responds to the complete range of call progress signals from 340Hz to 650Hz
DETECT2 responds to higher frequency call progress and voice or similar activity
DETECT3 responds to and indicates the presence of a single tone

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings
Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
P/DW Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits
Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Xtal Frequency		3.57	3.59	MHz

© 1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050, Fax: 910 744 5054
Doc. #20480148.001

Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz, S/N = 16 dB, Noise Bandwidth = 5 kHz,
V_{DD} = 3.3V to 5.0V, T_{AMB} = - 40°C to 85°C. 0dB = 775mV_{RMS}.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
Supply Current					
I_{DD} (ENABLE = 1) (V_{DD} = 5.0V)	1		0.5	1.0	mA
I_{DD} (ENABLE = 1) (V_{DD} = 3.3V)	1		0.3	0.7	mA
Enable Input					
Input Logic 1 Level	2	80%			V_{DD}
Input Logic 0 Level	2			20%	V_{DD}
Input Leakage Current (V_{IN} = 0 to V_{DD})	2	−5.0		5.0	µA
Input Capacitance	2		10.0		pF
Detect Output					
Output Logic 1 Level (I_{OH} = 120µA)	3	90%			V_{DD}
Output Logic 0 Level (I_{OL} = 360µA)	3			10%	V_{DD}
AC Parameters					
SIGIN pin					
Input Impedance (at 100Hz)	4		350		kΩ
Input Signal Level	5	-40			dB
Input Signal Dynamic Range	5	40			dB
Signal to Noise Ratio		16			dB
Clock Input					
'High' Pulse Width	6	40			ns
'Low' Pulse Width	6	40			ns
Input Impedance (at 100Hz)		10			MΩ
Gain (input = 1mV_{RMS} at 100Hz)		20			dB

Operating Characteristics Notes:

1. Not including any current drawn from the device pins by external circuitry.
2. ENABLE pin.
3. DETECT1, DETECT2 and DETECT3 pins.
4. Small signal impedance.
5. The input level is not critical as the detector uses a stochastic algorithm.
6. Timing for an external input to the CLOCK pin.

© 1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050, Fax: 910 744 5054

Timing Characteristics

For the following conditions unless otherwise specified:

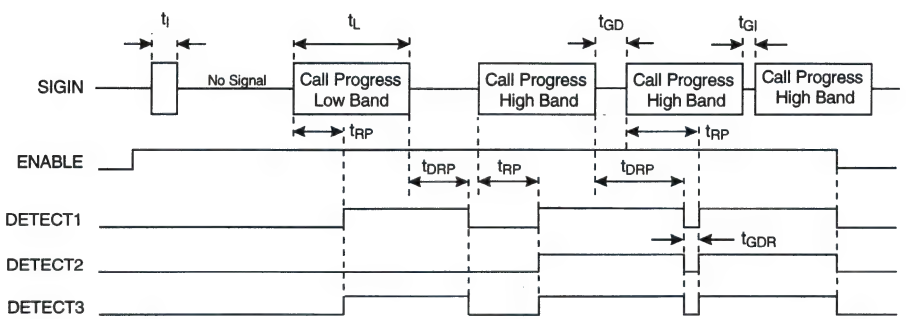
Xtal Frequency = 3.579545MHz, V_{DD} = 3.3V to 5.0V, T_{AMB} = - 40°C to 85°C, S/N = 20dB.

Timing (ref. Figures 3, 4, 5 and 6)		Notes	Min.	Typ.	Max.	Units
t_I	Burst Length Ignored	1			70	ms
t_L	Burst Length Detected	1	145			ms
t_{GI}	Call Progress Tone Gap Length Ignored	1, 2			20	ms
t_{GD}	Call Progress Tone Gap Length Detected	1, 2	40			ms
t_{RP}	Call Progress Tone Response Time	1			145	ms
t_{DRP}	Call Progress Tone De-response Time	1			145	ms
t_{GDR}	Gap Detected Recorded	1, 3	6			ms
t_{NG}	Non Call Progress Signal Gap Length Ignored	4			80	ms
t_{NRP}	Non Call Progress Signal Response Time		145			ms
t_{DNRP}	Non Call Progress signal De-response Time				80	ms
t_{CH}	State Change		0			ms
t_V	DETECT1, DETECT2, and DETECT3 Response Time	5			145	ms

Timing Notes:

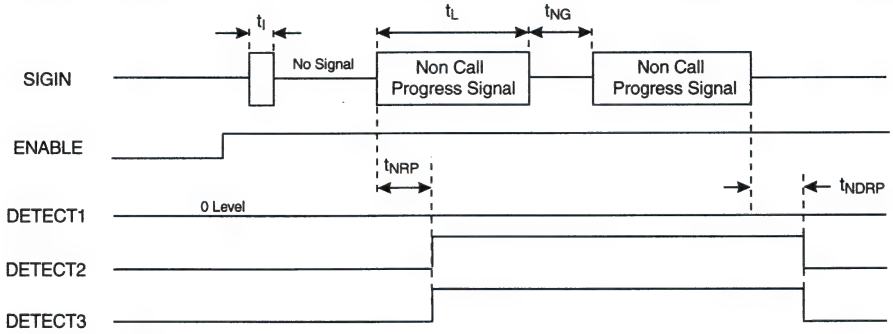
1. Timings also apply to Special Information Tone.
2. Only applies to bursts of the same frequency.
3. To acknowledge a short tone gap ≥ 40 ms, No Signal is indicated for a minimum of 6ms.
4. If the gap > 90 ms, a No Signal state will be decoded.
5. Time between a stable XTAL/CLK and a valid DETECT1, DETECT2, and DETECT3 state when ENABLE is logic high..

Timing Diagrams



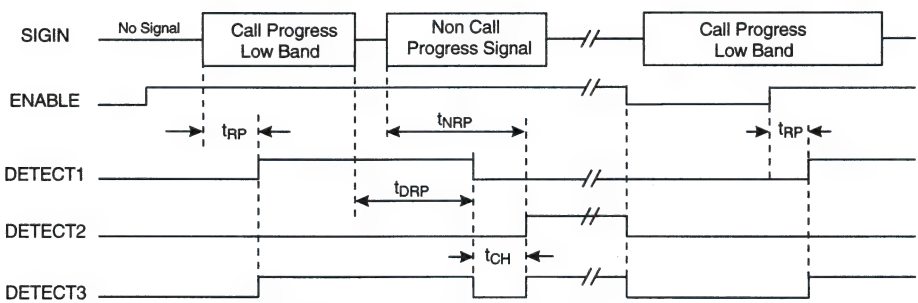
Note: DETECT3 is logic high only when the Call Progress Signal, or the Non Call Progress Signal is a single frequency tone.

Figure 3: Timing Diagram: Call Progress Tone(s)



Note: DETECT3 is logic high only when the Call Progress Signal, or the Non Call Progress Signal is a single frequency tone.

Figure 4: Timing Diagram: Non Call Progress Signal



Note: DETECT3 logic high only when the Call Progress signal, or the Non Call Progress signal is a single frequency tone.

Figure 5: Timing Diagram: Call Progress Tone(s) to Non Call Progress Signal

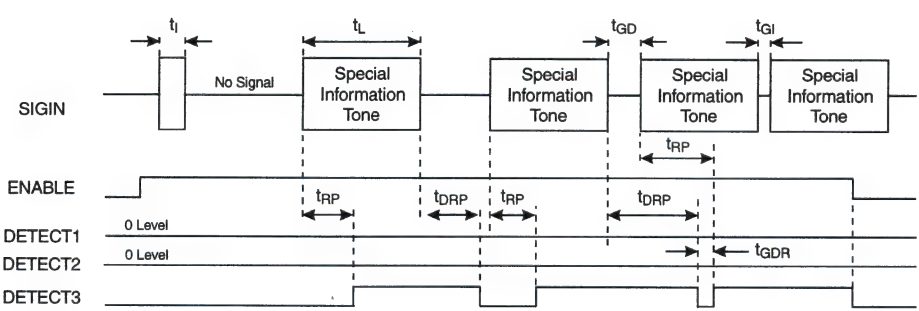


Figure 6: Timing Diagram: Special Information Tones

© 1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050, Fax: 910 744 5054

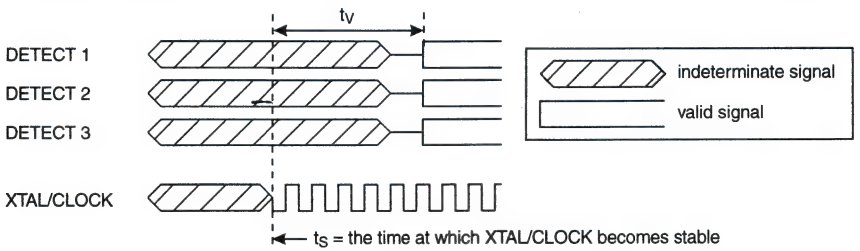


Figure 7: Timing Diagram: DETECT1, DETECT2, and DETECT3 Response time when ENABLE is high

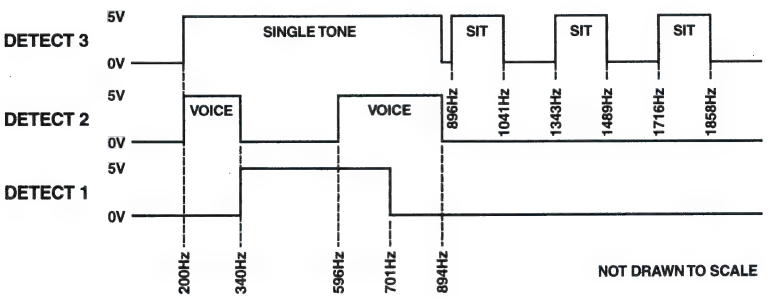
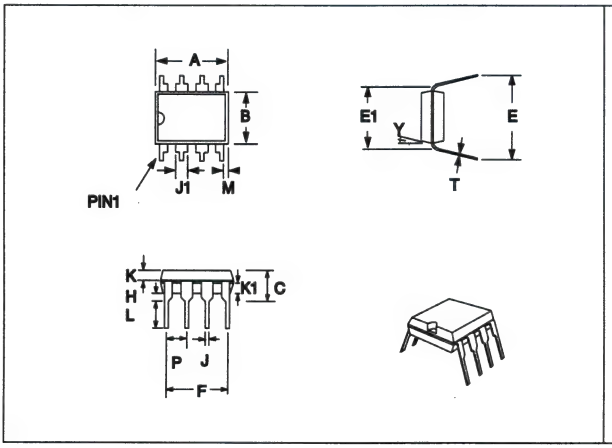


Figure 8: MX643 Frequency Sweep Results

6.2 Packaging

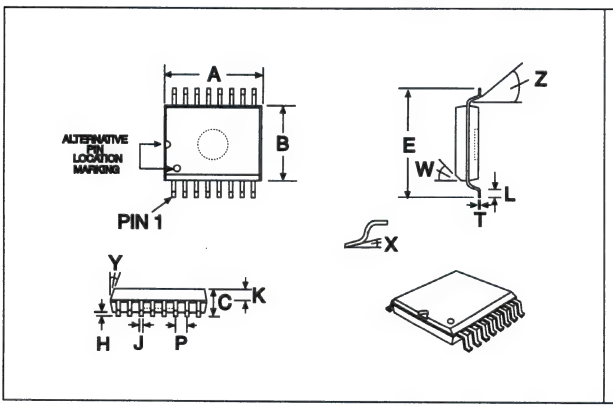


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.346 (8.790)		0.400 (10.16)
B	0.240 (6.10)		0.260 (6.60)
C	0.145 (3.68)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.87).
E1	0.290 (7.37)		0.325 (8.22)
F		0.30 (7.62)	
H	0.015 (0.38)		0.040 (1.01)
J	0.015 (0.38)		0.023 (0.58)
J1	0.045 (1.14)		0.065 (1.65)
K		0.060 (1.52)	
K1		0.060 (1.52)	
L	0.121 (3.07)		0.150 (3.81)
M	0.020 (0.51)		0.033 (0.84)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 8-pin PDIP Mechanical Outline: *Order as part no. MX643P*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 16-pin SOIC Mechanical Outline: *Order as part no. MX643DW*

© 1996 MX•COM, INC.
Tele: 800 638 5577, 910 744 5050, Fax: 910 744 5054

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX651

Telephone Subscriber Pulse Metering & Anti Fraud Tone Processor

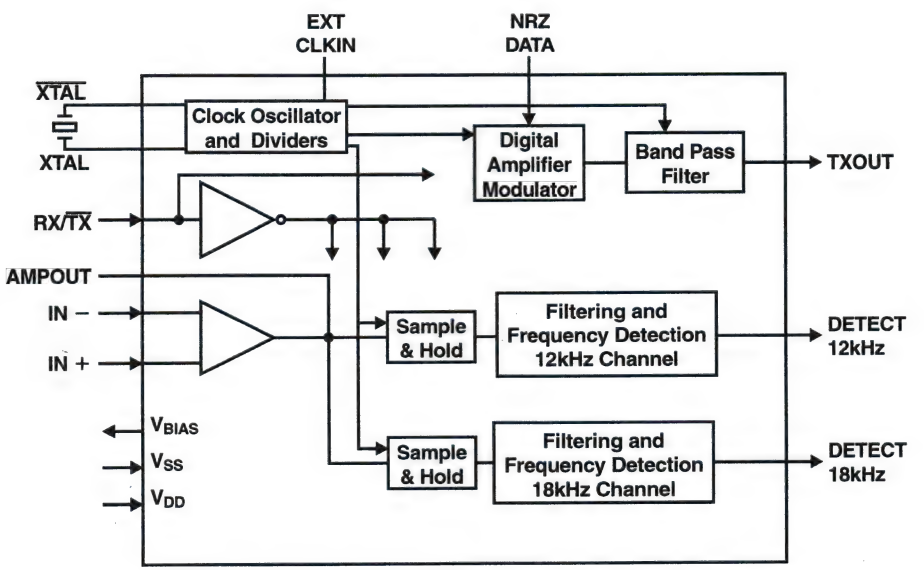
PRELIMINARY INFORMATION

Features

- **Rapid 18kHz tone encoder-decoder can transfer NRZ data**
  - **Tx up to 166bps**
  - **Rx up to 62bps**
- **12kHz Subscriber Pulse Metering Detector**

Applications

- **Meets European 12kHz SPM Frequency Specifications**
- **Payphone Applications**
- **Card Operated Telephone Installations**
- **Component Adjustable Input Sensitivity**
- **Low Power 3.3V/5.0V Operation**



The MX651 is a low power integrated circuit which combines 12kHz Subscriber Pulse Metering (SPM) detection with 18kHz tone processing for anti-fraud purposes within a telephone system. Suitable for battery or line powered systems, the MX651 is protected from crosstalk and false decoding by employing high accuracy switched capacitor filters. By using simple logic or µProcessor control the MX651 will:

- Decode 12kHz SPM pulses (in the presence of high level voice and 18kHz signaling) and provide a logic output.
- Transmit an NRZ amplitude modulated 18kHz security tone to line.
- Decode an incoming modulated 18kHz security tone (in the presence of high level voice and 12 kHz SPM tones) and provide a logic output.

The MX651 is available in a 16-pin SOIC (MX651DW) and a 16-pin PDIP (MX651P) package.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

CONTENTS

Section ..... **Page**

1. Block Diagram **2-131**

2. Signal List **2-132**

3. External Components **2-133**

4. General Description **2-134**

4.1 Overall Function 2-134

4.1.1 SPM (12kHz) Detector 2-134

4.1.2 Security Tone (18kHz) Detector (Rx Mode Only) 2-134

4.1.3 Security Tone Transmission (Tx Mode Only) 2-134

4.2 Description of Blocks (Reference Figure 1) 2-134

4.2.1 Input Amplifier 2-134

4.2.2 Sample and Hold (12kHz Channel) 2-134

4.2.3 Filtering and Frequency Detection (12kHz Channel) 2-134

4.2.4 Sample and Hold (18kHz Channel) 2-134

4.2.5 Filtering and Frequency Detection (18kHz Channel) 2-134

4.2.6 Clock Oscillator and Dividers 2-135

4.2.7 (Gate ON-OFF) (Tx Only) 2-135

4.2.8 Band Pass Filter (Tx Only) 2-135

5. Application **2-135**

5.1 Device Sensitivity versus V_{DD} - Input Amplifier Gain 2-135

5.2 Alias Responses - False Decodes 2-135

5.2.1 12kHz Channel 2-135

5.2.2 18kHz Channel 2-136

6. Performance Specifications **2-136**

6.1 Electrical Performance 2-136

6.2 System Timing 2-139

6.2.1 Timing Diagrams 2-139

6.3 Packaging 2-140

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Block Diagram

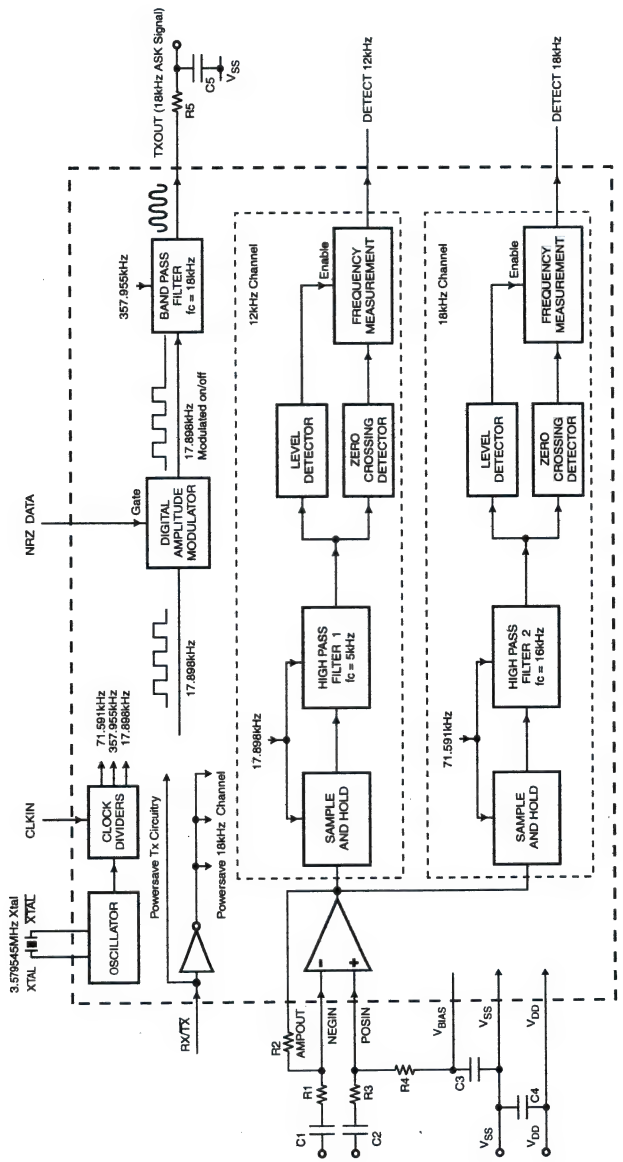


Figure 1: Block Diagram

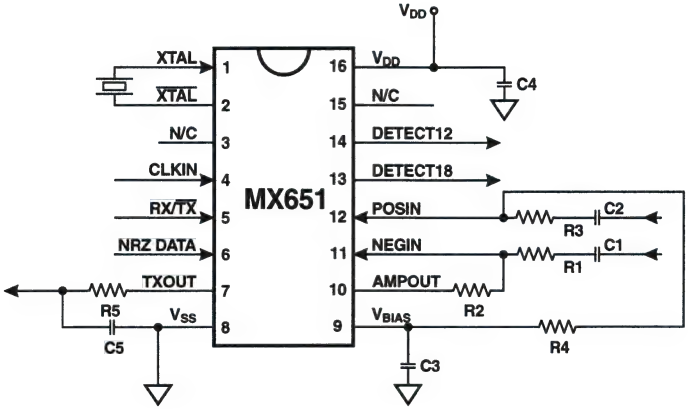
© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Signal List

Pin No.	Signal	Type	Description
1	XTAL	input	Input to the on-chip oscillator inverter.
2	$\overline{XTAL}$	output	Inverted output of the on-chip oscillator.
4	CLKIN	input	A logic input which may be used when an external clock signal is available in place of a crystal. The external 3.579545MHz signal is applied to this pin and XTAL is tied to V_{DD}. When not used, this pin should be tied to V_{DD}.
5	RX/$\overline{TX}$	input	A logic input which controls the operating mode of the device. In Rx, the device detects the presence of 12kHz and 18kHz tones. In Tx, the18kHz detect function is disabled and 18kHz is transmitted from the TXOUT pin modulated ON -OFF by the NRZ Data pin.
6	NRZ DATA	input	A logic input used in Tx mode to ASK modulate the TXOUT pin. A logic high corresponds to no tone and logic low corresponds to 18kHz.
7	TXOUT	output	The Tx mode output. It is ASK modulated by the NRZ data input pin. It transmits 18kHz or no tone depending upon the state of the NRZ data input pin. This pin goes to a high impedance state when in Rx mode.
8	V_{SS}	power	Negative supply.
9	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$ It also forms the analog ground for the input differential amplifier. This pin must be bypassed by a capacitor mounted close to the device pins (see Figure 1).
10	AMPOUT	output	Output of the input amplifier. External components are used in conjunction with the amplifier to couple the line signal into the device. Both inputs are available to allow a differential configuration because a two wire input is assumed.
11	NEGIN	input	Inverting input to the input amplifier.
12	POSIN	input	Non-inverting input to the input amplifier.
13	DETECT 18kHz	output	Logic output of the 18kHz channel. Logic 0 when a 18kHz tone (within specified frequency and amplitude limits) has been detected for a minimum length of time.
14	DETECT 12kHz	output	Logic output of the 12kHz channel. Logic 0 when a 12kHz tone (within specified frequency and amplitude limits) has been detected for a minimum length of time.
16	V_{DD}	power	Positive Supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor (see Figure 1).
3, 15	N/C		No internal connection: leave open circuit.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

External Components



R1, R3	See Note 1	1.1MΩ @ 3.3V 1.0MΩ @ 5.0V	±1% ±1%
R2, R4	See Note 1	270kΩ @ 3.3V 330kΩ @ 5.0V	±1% ±1%
C1, C2	See Note 1	33pF @ 3.3V 68pF @ 5.0V	±10% ±10%
C3, C4		0.1µF	±20%
R5		51kΩ	±1%
C5		100pF	±10%
XTAL	See Note 2	3.579545MHz	

Figure 2: Recommended External Components

External Components Notes

1. The device sensitivity is proportional to the power supply (V_{DD}) voltage. The input gain must compensate for this and also prevent input circuitry saturation. It is recommended that amplifier components (R1 to R4, C1 and C2) be used to set the gain between -10dB (if V_{DD} is 5.0V) and -13dB (if V_{DD} is 3.3V).
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak-to-peak. Tuning fork type crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

General Description

Overall Function

The MX651 is a dual channel tone detector for use in European, French, and other payphone systems where 12kHz SPM and 18kHz security tones are used.

SPM (12kHz) Detector

The SPM detector channel responds to a low level (50mV) 12kHz tone in the presence of a large security tone (16kHz - 20kHz) and speech.

The device responds after a period of continuous valid tone and so recognizes a valid SPM toneburst (minimum transmission duration, 40 - 50ms).

This function is permanently enabled.

Security Tone (18kHz) Detector (Rx Mode Only)

This demodulates the 18kHz ASK signal in the presence of the SPM signaling.

Security Tone Transmission (Tx Mode Only)

An 18kHz tone modulated ON - OFF by the NRZ data pin. A logic 0 gates the signal ON so that 18kHz is transmitted. A logic 1 gates the signal OFF so that no tone appears at the TXOUT pin.

Description of Blocks (Reference Figure 1)

Input Amplifier

This Input Amplifier is connected as a differential amplifier and is used to couple the signal into the device. It also attenuates the combined speech, SPM tone and security tone to prevent its output saturating. The signal gain should be -10dB at 5.0V supply and -13dB at 3.3V. (See Figure 2 for recommended component values).

Sample and Hold (12kHz Channel)

This samples the input signal at 17.898kHz and creates images of the incoming frequencies. The 12kHz SPM is translated to 5.898kHz and the security tone is translated to between 978Hz and 1182Hz. This simplifies the subsequent signal processing.

Filtering and Frequency Detection (12kHz Channel)

The output of the sample and hold circuit is passed to filter HPF1. This is a switched capacitor high pass filter which amplifies the frequency shifted SPM tone (about 5.9kHz) but rejects the frequency shifted security tone (about 1kHz). The filter also rejects any speech signals present. The filter output is passed to the level detect and frequency measurement circuitry which determines the presence or absence of a valid SPM signal on the line. A valid signal sends the "DETECT 12kHz" pin to logic low.

Sample and Hold (18kHz Channel)

This samples the input signal at 71.592kHz. It is synchronized with the following high pass filter, which is a switched capacitor circuit with the same sampling rate. The sample and hold circuit stores the value of the input waveform value between sampling instants so that it is a suitable input for the filter.

Without the sample and hold circuit, speech or SPM tone components which are large compared with the security tone would interfere with the level discrimination at the filter output.

Filtering and Frequency Detection (18kHz Channel)

The output of the sample and hold circuit is passed to filter HPF2. This is a switched capacitor high pass filter which amplifies the security tone (about 16.92kHz - 19.08kHz) but rejects the SPM tone.

The filter output signal is passed to the level detect and frequency measurement circuitry which determines the presence or absence of a valid security tone on the line. A valid signal sends the "DETECT 18kHz" pin to logic 0.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Clock Oscillator and Dividers

These circuits generate the internal clocks by division of the oscillator reference frequency. The crystal is connected as shown in Figure 2 without any need for other external components. When a crystal is used, the CLKIN pin should be left open circuit.

Alternatively, when a frequency of 3.579545MHz is externally available, the use of a crystal is unnecessary. The external frequency is applied to the CLKIN pin. In this case, the XTAL pin should be tied to V_{DD}.

In Tx, the dividers also generate a pulse train, frequency 18kHz, which is passed to the Tx circuitry (Gate ON - OFF and Band Pass Filter) for digital modulation and filtering.

(Gate ON-OFF) (Tx Only)

This circuit is a digital block. It performs ON - OFF modulation of the 18kHz pulse train generated from the crystal frequency by the digital dividers. It is controlled by the NRZ DATA pin and is used to encode NRZ data packets as pulsed 18kHz (ASK data). The modulated digital signal is passed to the Tx filter for wave shaping.

Band Pass Filter (Tx Only)

This is a 4th order band pass filter with center frequency 18kHz. It shapes the modulated digital pulse train from the previous block into a low distortion pulsed sinusoidal waveform. The resulting signal is the system acknowledgment security tone. It is transmitted by the subscriber equipment, via the telephone link, to the local exchange.

Application

Device Sensitivity versus V_{DD} - Input Amplifier Gain

The device sensitivity is proportional to V_{DD} because internal voltage references are derived from the power supply. Accordingly, input amplifier signal gain should be adjusted via external components. Figure 2 shows components recommended for 5.0V and 3.3V operation.

Alias Responses - False Decodes

The MX651 is designed to work in telephone systems where certain ranges of input frequencies are expected and other ranges are not. The 12kHz SPM channel works in the presence of speech and a tone in the range 16kHz - 20kHz. The security tone detector functions in the presence of an interfering tone in the range 11kHz - 13kHz. A significant tone at other frequencies may interfere with correct decoding of valid transmissions and should be avoided.

A small range of input frequencies could cause false decoding when no valid tone has been received. This is because of the frequency shifting property of the SPM channel and the sampled data filters in both channels.

The tone detectors in both the 12kHz and 18kHz channels will respond to 'other than normal' tones. Accordingly, such tones should be avoided.

12kHz Channel

The 12kHz tone detector response frequencies are described by the following two equations:

sign

$$f_{12kHz\ plus} = [(n \times 17.898kHz) + 5.893kHz] \pm 0.185kHz$$

$$f_{12kHz\ minus} = [(n \times 17.898kHz) - 5.893kHz] \pm 0.185kHz$$

n	nominal plus detect frequency (kHz)	nominal minus detect frequency (kHz)
0	5.893	N/A
1	23.791	12.005
2	41.689	29.903
...	...	...

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Note: A valid SPM input, in the range 11.82kHz - 12.18KHz, is met when; n = 1 and the nominal minus sign (-) detect frequency is calculated. The other inputs represent false decodes. The response time and level sensitivity for a false decode is the same as that for a valid decode, e.g. 42ms - 45ms of 5708Hz at 50mV could cause a false decode at the "DETECT 12kHz" pin.

18kHz Channel

The 18kHz tone detector response frequencies are described by the following two equations:

sign

$f_{18kHz\ plus} = [(n \times 71.591kHz) + 18.0kHz] \pm 1.08kHz$

$f_{18kHz\ minus} = [(n \times 71.591kHz) - 18.0kHz] \pm 1.08kHz$

n	nominal plus detect frequency (kHz)	nominal minus detect frequency (kHz)
0	18	N/A
1	89.591	53.591
2	161.182	125.182
3	232.773	196.773
...	...	...

Note: A valid security tone input is met when, n = 0 and the nominal plus sign (+) detect frequency is calculated. The other inputs represent false decodes. The response time and level sensitivity for a false decode is the same as that for a valid decode, e.g. 5.8ms of 52.511kHz at 40mV could cause a false response at "DETECT18kHz" pin.

Performance Specifications

Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device. Correct operation of the device outside these limits is not implied.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin (wrt V_{SS})	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / P Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Operating Temperature	-40	85	°C
Storage Temperature	-55	125	°C

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Operating Limits

For the following conditions unless otherwise specified.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	3.0	5.5	V
Operating Temperature	-40	85	°C
Xtal Frequency	3.579008	3.580082	MHz

Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz, Noise and Distortion Measured in 50kHz Bandwidth
V_{DD} = 3.3V to 5.5V @ T_{AMB} = 25°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD}	1		2.5	4.0	mA
I_{DD}	2		1.0	2.0	mA
Logic 1 Input Level	1, 3	3.5			V
Logic 0 Input Level	1, 3			1.5	V
Logic 1 Output Level at I_{OH} = -120µA	1	4.6			V
Logic 1 Output Level at I_{OL} = 360µA	1			0.4	V
AC Parameters					
Tx Output					
Tx Output Impedance (Tx mode)	4		1.0	2.5	kΩ
Tx Output Impedance (Rx mode)	4	300	500		kΩ
Output Frequency		17.82		18.18	kHz
Output Distortion	5			2	%
Signal Level	5, 6	3.0	3.4	3.7	V_{P-P}
Signal Level	5, 7	2.0	2.2	2.4	V_{P-P}
Response/De-response Times	8			100	µs
Rise/Fall Times	9			5	ms
Rx Input	10				
Rx Input Impedance		10.0			MΩ
Rx Input Amp Voltage Gain			500		V/V
12kHz (SPM) Channel Performance	11				
With Interfering Speech & Security Tone	12				
Input Signal Level	12			800	mV
Decode Min Signal Level	12			50	mV
No Decode Max Signal Level	12	25			mV
Response Delay	12, 13	40		50	ms
De-response Delay	12, 13	40		50	ms
Detect Bandwidth	12	11.82		12.18	kHz
Not Detect Frequencies (below 12kHz)	12			11.52	kHz
Not Detect Frequencies (above 12kHz)	12	12.48			kHz

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

	Notes	Min.	Typ.	Max.	Units
18kHz (Security Tone) Channel Performance	14				
With Interfering Speech & SPM Tone	15				
Input Signal Level	15			1.2	V
Decode Min Signal Level	15			40	mV
No Decode Max Signal Level	15	10			mV
Response/De-response Times	15, 16			8	ms
Detect Bandwidth	15	16.92		19.08	kHz
Not Detect Frequencies (below 18kHz)	15			16.25	kHz
Not Detect Frequencies (above 18kHz)	15	19.75			kHz

Operating Characteristics Notes:

1. At V_{DD} = 5.0V only, I_{DD} specification does not include any current drawn from the device pins by external circuitry.
2. At V_{DD} = 3.3V only, I_{DD} specification does not include any current drawn from the device pins by external circuitry.
3. CLKIN input signal may be sinusoidal.
4. Small signal impedance.
5. At output of smoothing network.
6. V_{DD} = 5.0V.
7. V_{DD} = 3.3V.
8. The time between a logic 1 - 0 transition at NRZ data input and the tone amplitude at TXOUT reaching 10% of its full value or between a 0 - 1 transition at NRZ data input and the tone amplitude falling to 90% of its full value.
9. The time for the 18kHz tone amplitude at TXOUT to rise from 10% to 90% or to fall from 90% to 10% of its full value.
10. Input amplifier signal gain set to -10dB for V_{DD} = 5.0V, -13dB for V_{DD} = 3.3V.
11. Maximum 10% distortion for incoming SPM tone, not including interfering speech or security tone (16kHz - 20kHz). Minimum SNR 22dB for incoming SPM tone before the input capacitor.
12. Signal levels at the amplifier input, i.e. before the input capacitor. 12kHz channel performance specified in the presence of the following interfering signals:
    (a) A 1.2V continuous tone in the frequency range 16kHz - 20kHz
    (b) An ordinary speech signal containing frequencies in the range 300Hz - 3400Hz of maximum instantaneous amplitude 8.0V_{P-P}
13. The device responds after 40-50ms of continuous valid tone and de-responds after: a 40-50ms period of no-tone, tones less than 25mV or an out of band tone.
14. Maximum 10% distortion for incoming security tone, not including interfering SPM tone (11kHz - 13kHz). Minimum 20dB SNR for incoming security tone.
15. Signal level specified at the amplifier input, i.e. before the input capacitor. Performance specified in the presence of an interfering 800mV continuous tone in the frequency range 11kHz - 13kHz.
16. The device responds after 8ms of continuous valid tone and de-responds after any of: an 8ms period of no-tone, tone of 10mV or less, or an out of band tone.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

System Timing

		Notes	Min	Max	Unit
Rx					
12KHz	Response Delay		40	50	ms
	De-response Delay		40	50	ms
18KHz	Response Time			8	ms
	De-response Time			8	ms
Tx					
	Transmit 0 Time	Note 1, 2		5.1	ms
	Transmit 1 Time	Note 1, 2		5.1	ms

Note:

1. Tx Transmit Times include both Response/De-response Times and Rise/Fall Times.
2. The Tx Transmit 0 and Transmit 1 Time must exceed 5.1ms.

Timing Diagrams

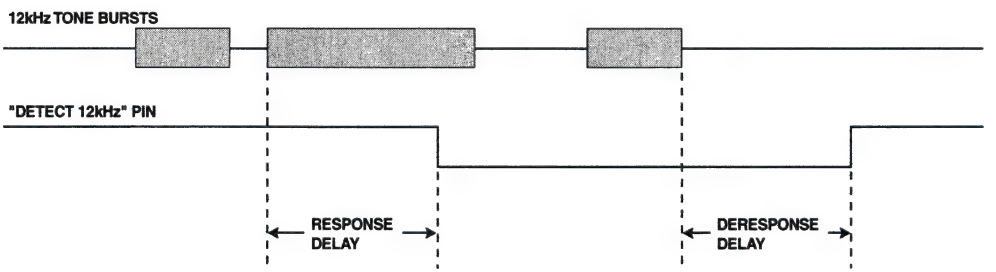


Figure 3: SPM (12kHz) channel. Toneburst and tonegaps < the response and de-response delays are ignored

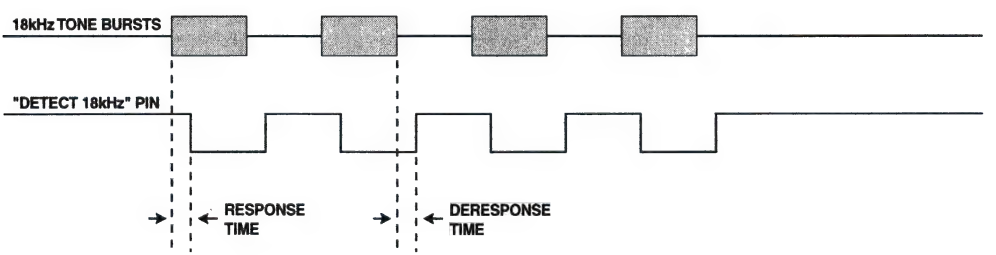


Figure 4: Security tone (18kHz) channel. The response and de-response times are short to enable the device to recognize short ON-OFF bursts (20ms each)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

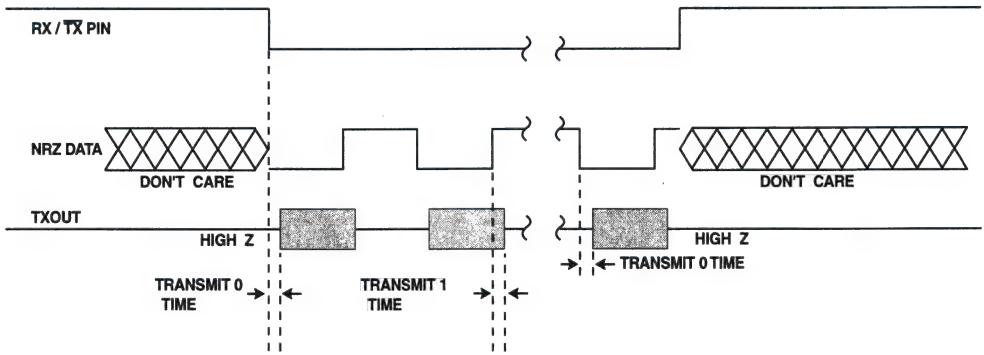
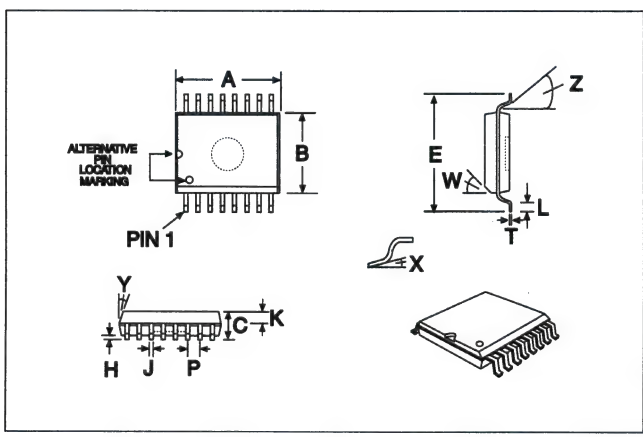


Figure 5: Transmit Mode. TXOUT is modulated by the NRZ DATA pin. An 18kHz toneburst represents logic 0 and "no tone" represents logic 1. Data packets with symbol periods ≥ 6ms can be transmitted.

Packaging



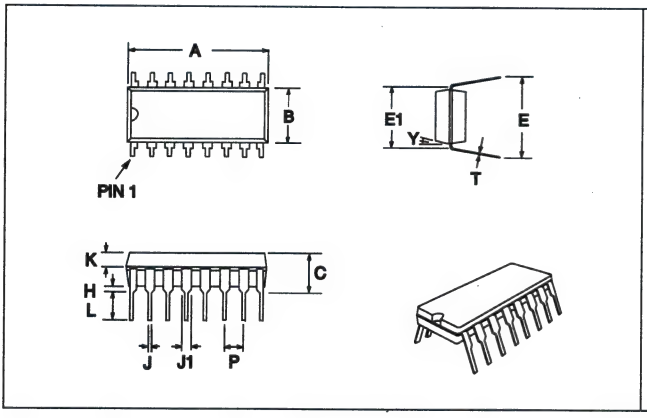
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: SOIC Mechanical Outline: *Order as part no. MX651DW*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: PDIP Mechanical Outline: *Order as part no. MX651P*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480137.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX663 Call Progress Decoder

ADVANCE INFORMATION

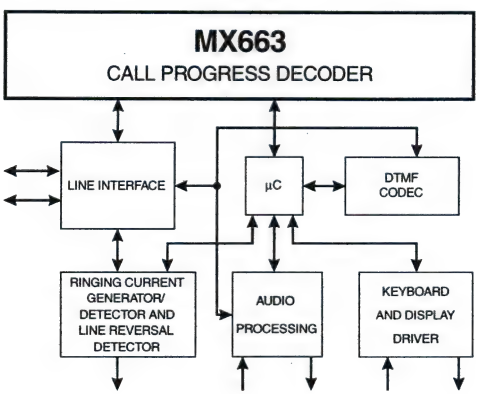
SHIPPING MAY 1997

Features

- **Worldwide Call Progress Tone Decoding:**
  - **Single and Dual Tones**
  - **Fax and Modem**
  - **Answer/Originate Tones**
  - **SIT (Special Information Tones)**
  - **Fast 'US Busy' Tone Detector**
- **Adjustable Detection Threshold**
- **Voice Detector**
- **Low Power 3.3V/5.0V Operation**

Applications

- **Call Progress Monitoring**
  - **Automatic Call Placement**
- **Machine Dialing**
- **Fax Tone Detection for Line Switching**



The MX663 decodes the standard audible tone signals provided by telecom systems worldwide to indicate Dial, Ringing, Busy, Unobtainable and other stages of a call attempt. It provides the key features needed for intelligent, full-function, call progress monitoring by applications involving machine dialing or automatic call placement. The MX663 also incorporates the following features:

- Single and dual tone decoding for better cross-system Call Progress monitoring.
- "US Busy" tone detector, saving time needed for "cadence verification" under Busy and Unobtainable conditions. This incorporates a separate 620Hz detector for improved response.
- A detector to indicate speech and non-call progress signals; this reduces voice falsing of call progress tones and adds Voice-Answer detection as a "connected" prompt.
- A fax and modem tone decoder.
- A separate, adjustable threshold, signal-level detector which reduces noise falsing.

The MX663 uses digital signal processing techniques to provide these advantages. It is a low cost, low power product with superior performance. The MX663 may be used with a 3.0 to 5.5 volt supply and is available in the following packages: 16-pin SOIC (MX663DW) or 16-pin PDIP (MX663P).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

CONTENTS

Section **Page**

1. Block Diagram **2-145**

2. Signal List **2-146**

3. External Components **2-147**

4. General Description **2-148**

4.1 Overall Function Description 2-148

4.2 Glossary 2-148

4.3 Block Diagram Description 2-148

4.3.1 SIGIN 2-148

4.3.2 Call Progress Detector: Signal Analyzer 2-149

4.3.3 620Hz Detector 2-149

4.3.4 Control and Output Logic 2-149

4.3.5 Level Detector and OPAMP 2-149

4.3.6 Xtal/Clock Oscillator 2-149

4.3.7 Decode Output Truth Table 2-150

5. Application **2-150**

5.1 General 2-150

6. Performance Specification **2-153**

6.1 Electrical Performance 2-153

6.1.1 Absolute Maximum Ratings 2-153

6.1.2 Operating Limits 2-153

6.1.3 Operating Characteristics 2-154

6.2 Timing 2-155

6.3 Packaging 2-158

MX COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1. Block Diagram

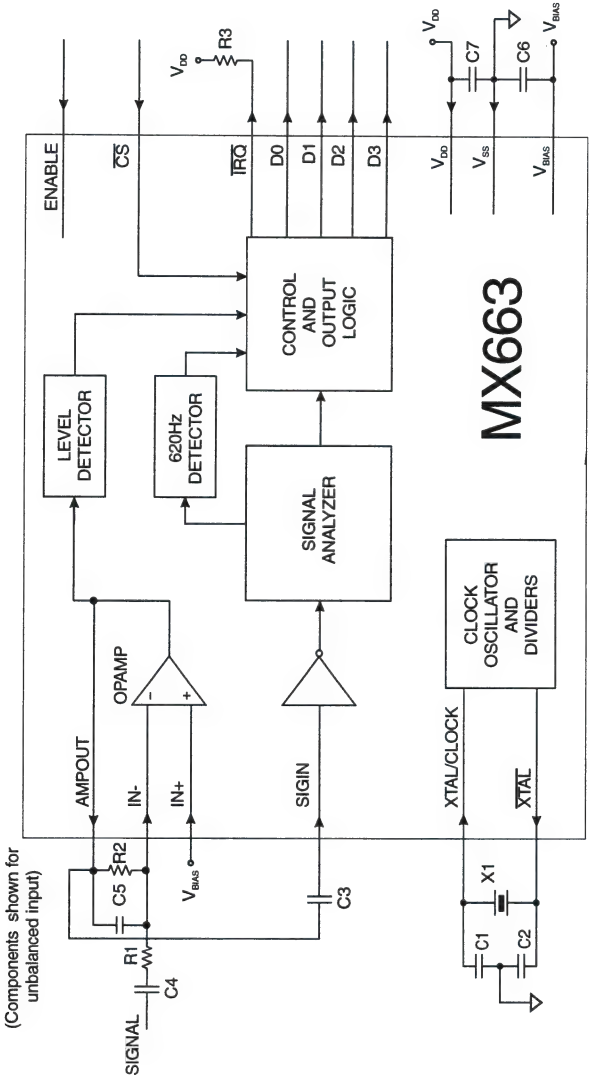


Figure 1: Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. Signal List

Pin No.	Signal	Type	Description
1	$\overline{XTAL}$	output	Inverted output of the on-chip oscillator.
2	XTAL/CLOCK	input	Input to the on-chip oscillator, for external Xtal circuit or clock.
3 4 5 6	D3 D2 D1 D0	output	D3, D2, D1 and D0 is a 4-bit parallel data word output to the µC. The transmission of data is under the control of the $\overline{CS}$ input. These 3-state outputs are held at high impedance when $\overline{CS}$ is at "1". See Figure 8 If $\overline{CS}$ is permanently at "0", D3, D2, D1 and D0 are permanently active. See Figure 4 and Figure 7.
7	$\overline{CS}$	input	The chip select pin activates the Data Bus "D0: 3" when held low. A µC can provide this input to allow the MX663 to reside on a shared Data Bus. Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See Figure 8
8	$\overline{IRQ}$	output	This output indicates an interrupt condition to the µC by going to a logic "0". This is a "wire-ORable" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pullup resistor is required. If $\overline{CS}$ is permanently at "0", the interrupt condition is a logic "0" pulse. See Figure 4 and Figure 7.
9	ENABLE	input	A low level input selects the powersave mode, all circuits are reset and disabled. D0 - D3 outputs become high impedance. A high level input enables all circuits.
10	V_{SS}	Power	Negative supply (ground).
11	SIGIN	input	Signal input. The signal to this pin should be ac coupled. The dc bias of this pin is set internally.
12	V_{BIAS}	output	Internally generated bias voltage, held at $V_{DD}/2$ when the device is not in powersave mode, it should be bypassed to V_{SS} by a capacitor mounted close to the device pins. In powersave mode this pin is pulled towards V_{SS}.
13	IN+	input	Non-inverting input to the on-chip amplifier.
14	IN-	input	Inverting input to the on-chip amplifier.
15	AMPOUT	output	Output of the on-chip amplifier, this is internally connected to the input of the Level Detector.
16	V_{DD}	Power	The positive supply rail. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

Table 1: Signal List

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components

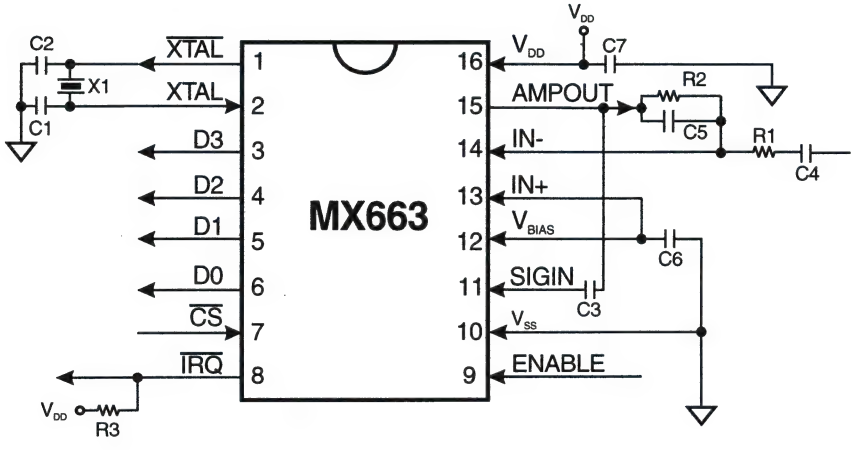


Figure 2: Recommended External Components

R1	Note 3	100kΩ	±10%
R2	Note 3	510kΩ	±10%
R3		20kΩ	±10%
C1		33pF	±20%
C2		33pF	±20%
C3		0.1µF	±20%

C4	Note 3	0.1µF	±20%
C5	Note 3	100pF	±20%
C6		0.1µF	±20%
C7		1µF	±20%
X1	Note 1, 2	3.579545MHz	±100ppm

Table 2: Recommended External Components

Notes

1. A standard Color Burst Crystal Frequency is recommended.
2. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
3. Reference section 4.3.5.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4. General Description

4.1 Overall Function Description

The MX663 consists of a Call Progress Tone Detector, a 620Hz Detector and a Level Detector.

The MX663 Call Progress Tone Detector uses different tone detection methods from those commonly found with other products.

Many traditional devices use a bandpass filter followed by an energy detector. The filter is usually designed to pass input signals with a frequency between about 300Hz and 700Hz, and the amplitudes of signals in this range are then checked against a level threshold. Any signal of acceptable level in this frequency band is classed as a Call Progress tone, including signals due to speech and noise. False outputs caused by speech are a common feature with these products, and background noise may lead to a stuck "detect" output.

The MX663, by contrast, uses a stochastic signal processing technique based on analysis in both the frequency and time domain, with signal amplitude forming a small part in the decision process. This analysis includes checks on whether the signal has a "profile" which matches international standards for Call Progress tones, or a profile more likely to match that of speech, noise or other non-call-progress signals. It also adds checks on whether tones which include frequencies corresponding with the "US Busy" signals, Special Information Tones and Fax/Modem Tones have been detected.

4.2 Glossary

Call Progress Tones: The single and dual frequency tones in the range 350Hz to 620Hz specified widely for call progress signaling.

Call Progress Band: The nominal range 340Hz to 700Hz within which the MX663 will detect Call Progress tones. The detection algorithm requires that the tones have the characteristics typical of Call Progress Tones.

620Hz Detection: The nominal range 590Hz to 650Hz. Single tones in this range, or dual tones having a material frequency component within this range (e.g. 480 + 620Hz) will be detected.

Non Call Progress Signal: A signal falling within the nominal range (a) 200Hz to 895Hz, but NOT within the Call Progress Band, or (b) within the nominal range 200Hz to 895Hz, but NOT meeting the DETECTION REQUIREMENTS when the signal falls in the Call Progress Band.

Subject to the duration and other characteristics of such signals, the MX663 will usually interpret these as a Non Call Progress Signal (e.g. speech or other signal activity).

Special Information Tone: The nominal frequencies 950Hz or 1400Hz or 1800Hz.

Fax/Modem Low Tone: The nominal frequency 1250Hz.

Fax/Modem High Tone: The nominal frequency 2150Hz.

Minimum Input Signal: The minimum signal level for the specified tone decoding performance. The lower level at which absence of an input signal will be registered is not specified. However, a separate signal level detector makes amplitude information available.

No Signal: A signal falling outside the nominal range 180Hz to 2280Hz or the absence of an input signal. Either will be detected as a No Signal condition.

Nominal: Subject to dynamic tolerances within the signal analysis process. Absolute values are not material or adverse to performance.

4.3 Block Diagram Description (Reference Figure 1)

4.3.1 SIGIN

The input signal is amplified by a self-biased inverting amplifier. The dc bias of this input is internally set at. Accordingly, the input signal should be capacitively coupled to SIGIN.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.3.2 Call Progress Detector: Signal Analyzer

The analyzer samples the call progress signal at 9.322kHz. An external Anti-Alias Filter can be configured using the on-chip opamp. The frequency range, quality and consistency of the input signal is analyzed by this functional block. To be classified as a call progress signal the input signal frequencies should lie between 340Hz and 700Hz, the signal to noise ratio must be 16dB or greater and the signal must be consistent over a period of at least 145ms. These decode criteria are continuously monitored and the assessment is updated every 7ms. See section 4.3.5.

Because the analyzer time samples the input signal (SIGIN), signals above the operating band (2300Hz) can alias, appear inband, and therefore be detected. Accordingly, applying signals above (2300Hz) should be avoided. Such signals may be inadvertently generated by other sources such as digital clocks, switching power supply, crosstalk, etc.

4.3.3 620Hz Detector

The detector is designed to aid detection of "US Busy" tone. The bandwidth of the 620Hz Detector is 60Hz and the signal must be consistent over a period of at least 145ms for detection to occur. This assessment is updated every 55ms.

4.3.4 Control and Output Logic

This block categorizes the nature of the signal into various decoded output states and controls the four outputs. See the Truth Table in section 4.3.7.

4.3.5 Level Detector and OPAMP

The OPAMP is configured as an amplifier with external components R1, R2, C4 and C5. The level detector operates by measuring the level of the amplified input signal and comparing it with a preset threshold which is defined inside the MX663 as shown in the gain calculations below.

The detector output goes to the Control and Output Logic block. The data output is gated with the level detector's output. The data output is valid only if the level detector output is true. The level detector output can be forced true by connecting IN+ to V_{BIAS} and IN- to V_{SS} through a 100kΩ resistor. An interrupt is produced if the output data changes state.

Gain Calculations:

1. Set gain so an input signal level is amplified above the threshold level of $250mV_{P-P}$.

$$\text{Gain} > \frac{250mV_{P-P}}{V_{IN}}$$

where V_{IN} is the input signal level at C4 in mV_{P-P}.

In simplified form to assist with component value selection:

1. DC Gain = -R2/R1
2. C5 and R2 form a low-pass filter to attenuate out of band signals applied to SIGIN. The low pass filter's band edge is determined by the following: The recommended R2 and C5's component values are selected so than f(-3dB) = 3120Hz .

$$f(-3dB) = \frac{1}{2 \cdot \pi \cdot R2 \cdot C5}$$

3. C4 is a DC blocking capacitor, large enough to avoid affecting the AC gain in the frequency band of interest.
4. The following formula defines the ac gain as a function of frequency, R1, R2 and C5 component values.

AC gain, Av(f)

$$|Av(f)| = \frac{R1}{R2 \cdot \sqrt{1 + (2 \cdot \pi \cdot f \cdot R2 \cdot C5)^2}}$$

4.3.6 Xtal/Clock Oscillator

If the on-chip Xtal oscillator is to be used, then external components X1, C1 and C2 are required. If an external clock source is to be used, then it should be connected to the XTAL/CLOCK input pin and the $\overline{XTAL}$ pin should be left unconnected.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.3.7 Decode Output Truth Table

D3	D2	D1	D0	Conditions
0	0	0	0	No Signal
0	0	0	1	Call Progress Dual Tones: Will detect 350+440, 400+450, 440+480 Hz tones
0	0	1	0	Non Call Progress Signal, e.g. Voice Activity
0	0	1	1	Call Progress Dual Tone including 620Hz Detection: Will detect 480+620 Hz tones
0	1	0	0	Special Information Tone: Will detect 950, 1400 and 1800 Hz tones
0	1	0	1	Call Progress Single Tone: Will detect 400, 425, 440 and 450 Hz tones
0	1	1	0	Will detect a single tone lying outside the Call Progress Band and within the Non Call Progress signal range
0	1	1	1	Call Progress Single Tone including 620Hz Detection: Will detect 600 and 620 Hz tones
1	0	0	0	Fax/modem High Tone: Will detect 2100 and 2200 Hz tones
1	0	0	1	Reserved for future use
1	0	1	0	Reserved for future use
1	0	1	1	Reserved for future use
1	1	0	0	Fax/modem Low Tone: Will detect 1200 and 1300 Hz tones
1	1	0	1	Reserved for future use
1	1	1	0	Reserved for future use
1	1	1	1	Reserved for future use

Table 3: Decode Truth Table

5. Application

5.1 General

Apply a reset after power-up by taking the ENABLE pin low. This places the device in a powersave mode and resets the internal circuits. It also places the data word output (D0-D3) in a high impedance state, regardless of the level on the $\overline{CS}$ pin.

From this mode the device can be returned to normal operation without any additional settling time, when using the component values recommended in Figure 2. The tone response times remain the same and are given in section 6.1.

An interrupt is produced when the decode state is changed. This interrupt is reset by $\overline{CS}$ going to logic "0". When $\overline{CS}$ is permanently at "0", the interrupt condition is a 5 µs logic "0" pulse on the $\overline{IRQ}$ pin. When $\overline{CS}$ is set to logic "1", the data word output (D0-D3) goes into a high impedance state.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.2 Signal Category Reference

Signal Category	Sub-Category	Output Code $D_{3:0}$
No Signal		0 0 0 0
Voice and Non-Call Progress Signal	Not Single Tone Single Tone outside of CP band	0 X ~~1~~ 0 0 0 1 0 0 1 1 0
Call Progress Signal	Dual Tone without 620Hz Dual Tone with 620Hz Single Tone not 620Hz Single Tone 620Hz	0 X X 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 1
Special Information Tone (SIT Tone)	N/A	0 1 0 0
FAX/MODEM	Low High	1 1 0 0 1 0 0 0
Unused Codes	Reserved for future use	1 0 0 1, 1 0 1 0, 1 0 1 1, 1 1 0 1, 1 1 1 0, 1 1 1 1

Table 4: Signal Category

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.3 Typical Response

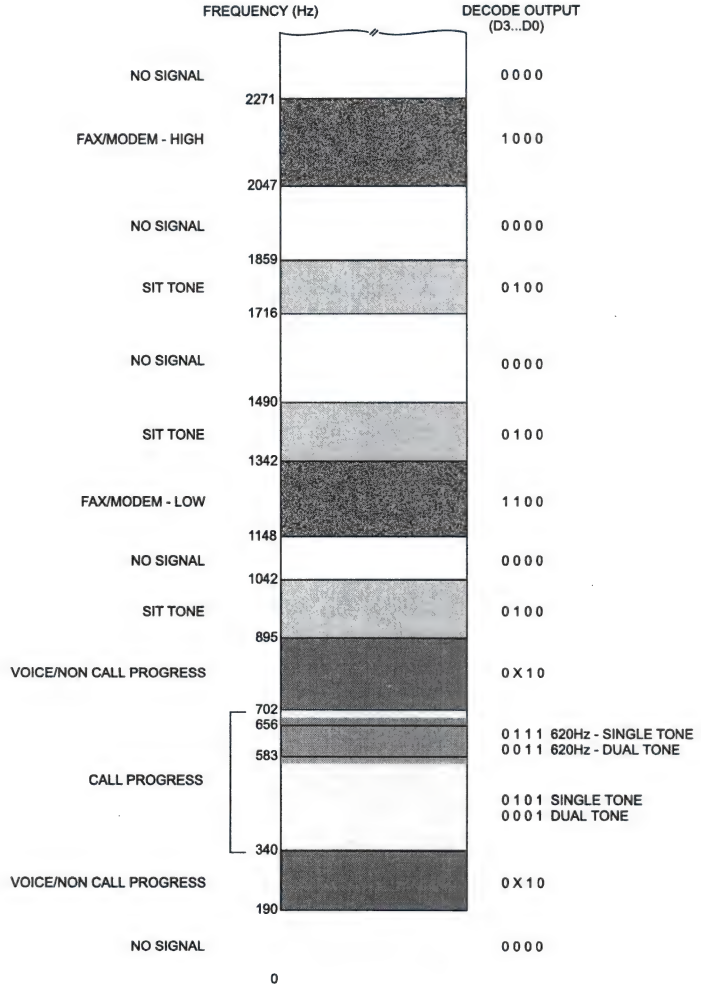


Figure 3: Typical Response Chart

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
P / DW Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency		3.57	3.59	MHz

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 3.579545MHz (Color Burst Crystal)
V_{DD} = 3.3V to 5.0V, T_{AMB} = 25°C.
0dB = 775 mV_{RMS}, S/N = 20dB, Noise Bandwidth = 5kHz Band Limited Gaussian

		Notes	Min.	Typ.	Max.	Units
DC Parameters						
I_{DD}						
all powersaved		1, 2		30		µA
V_{DD} = 3.3V		1		0.5	1	mA
V_{DD} = 5.0V		1		1.0	2	mA
Logic Interface						
Input Logic '1'			70%			V_{DD}
Input Logic '0'					30%	V_{DD}
Input Leakage Current	Logic '1' or '0'		-1.0		1.0	µA
Input Capacitance					7.5	pF
Output Logic '1'	I_{OH} = 120µA		90%			V_{DD}
Output Logic '0'	I_{OL} = 360µA				10%	V_{DD}
'Off' State Leakage Current		3			10.0	µA
AC Parameters						
SIGIN Pin						
Input Impedance		4		0.35		MΩ
Minimum Input Signal Level				-40.0		dB
Input Signal Dynamic Range			40.0			dB
Level Detector						
Signal Level Detection Threshold	measured at AMPOUT pin	5		-19.0		dB
OPAMP						
Input Impedance		6	10.0			MΩ
Voltage gain				500		V/V
Xtal/Clock Input						
Pulse Width	'High' or 'Low'	7	40.0			ns
Input Impedance	at 100Hz		10.0			MΩ
Gain	input = 1 mV_{RMS} at 1kHz		20.0			dB

Notes:

1. Not including any current drawn from the device pins by external circuitry.
2. Enable input at V_{SS}, $\overline{CS}$ input at V_{DD}.
3. $\overline{IRQ}$ pin, D0 to D3 pins.
4. Small signal impedance over the frequency range 100Hz to 2300Hz and at 5.0V.
5. Input signal level is multiplied by the voltage gain (-R2/R1). The overall signal at AMPOUT should be larger than 250mV_{P-P}, for V_{DD} = 5.0V. This threshold is proportional to V_{DD}.
6. Open loop, small signal low frequency measurements.
7. Timing for an external input to the XTAL/CLOCK pin.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

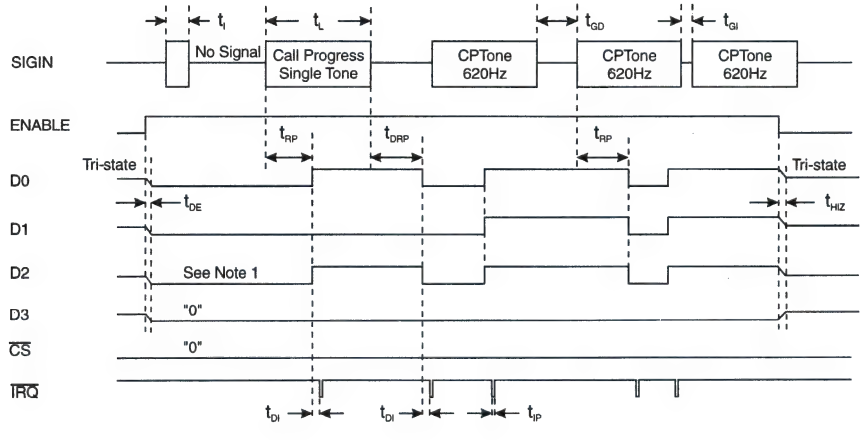
6.2 Timing

For the following conditions unless otherwise specified:
Xtal Frequency = 3.579545MHz, V_{DD} = 3.3V to 5.0V, T_{AMB} = 25°C.

	Parameter	Notes	Min.	Typ.	Max.	Units
t_{RP}	Call Progress Tone Response Time	1			145	ms
t_{DRP}	Call Progress Tone De-response Time	1			145	ms
t_{NRP}	Non Call Progress Signal Response Time		145			ms
t_{NDRP}	Non Call Progress Signal De-response Time			80		ms
t_I	Burst Length Ignored	1			70	ms
t_L	Burst Length Detected	1	145			ms
t_{GI}	Call Progress Tone Gap Length Ignored	1, 2, 3			20	ms
t_{GD}	Call Progress Tone Gap Length Detected	1, 2	40			ms
t_{NG}	Non Call Progress Signal Gap Length Ignored	4		80		ms
t_{DI}	Data available to Interrupt pulse				430	µs
t_{DE}	"$\overline{CS}$ -Low " to Data Valid				0.2	µs
t_{HIZ}	"$\overline{CS}$ -High" to Output Tri-state				1.0	µs
t_{IR}	Interrupt Reset Time				0.2	µs
t_{IP}	Interrupt Low Pulse		4.0	5.0	6.0	µs

Notes:

1. Timing also applies to Special Information Tones and Fax/modem Tones.
2. Only applies to burst of the same frequency.
3. For Special Information Tones and Fax/Modem tones, t_{GI} is 15ms maximum.
4. If the gap > 90ms, a NO Signal state will be detected.

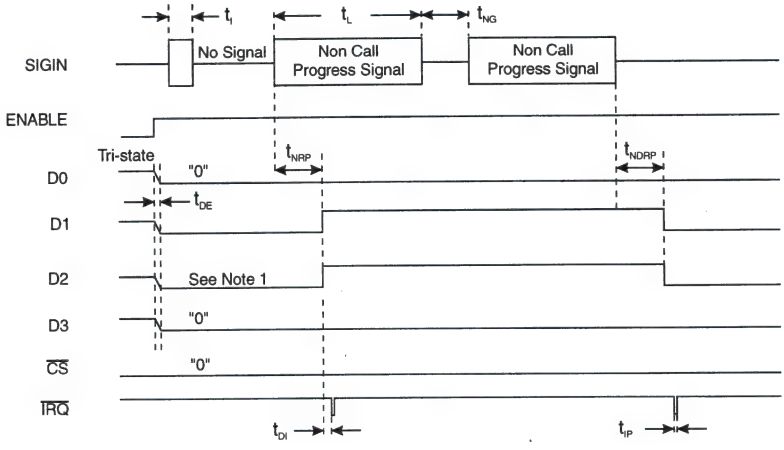


Note

1. D2 is '1' only when the Call Progress signal, or a Non Call Progress signal, is a single frequency tone.

Figure 4: Timing Diagram: Call Progress Tone(s)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



Note:

1. D2 is '1' only when the Call Progress signal, or a Non Call Progress signal, is a single frequency tone.

Figure 5: Timing Diagram: Non Call Progress Signal

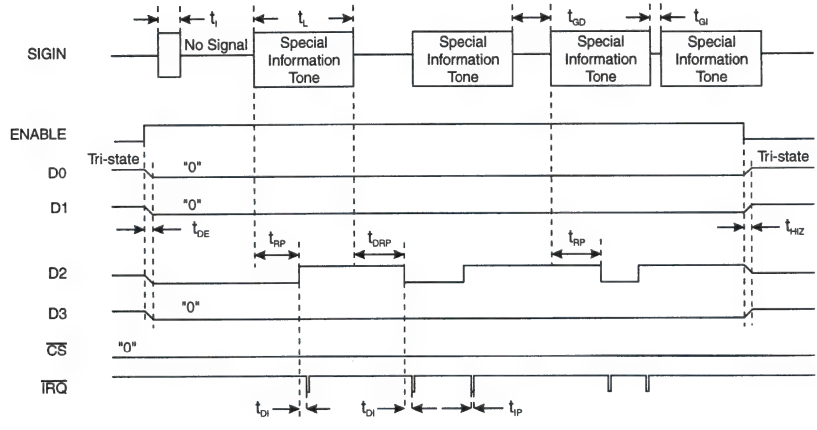


Figure 6: Timing Diagram: Special Information Tones

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

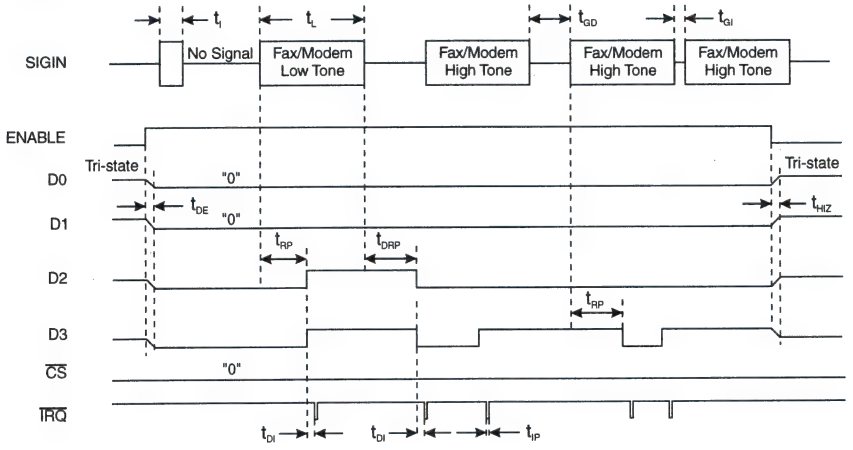


Figure 7: Timing Diagram: Fax/Modem Tones

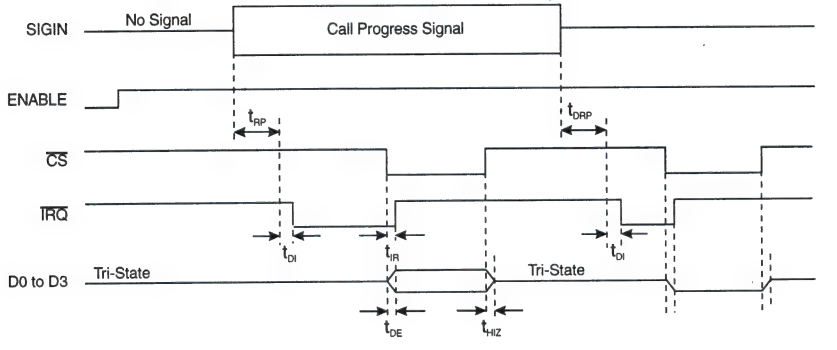
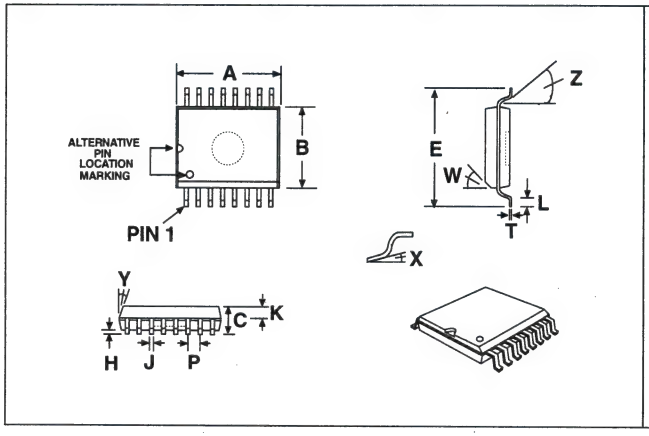


Figure 8: Bus Timing

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.3 Packaging

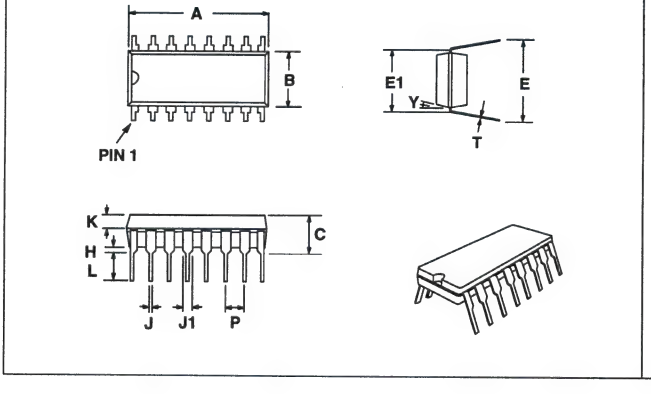


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 16-pin SOIC Mechanical Outline: *Order as part no. MX663DW*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 16-pin PDIP Mechanical Outline: *Order as part no. MX663P*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480165.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Technical Specifications

Section 3: Sub-Audio Tone Signaling & Detection IC's

Device	Description	Page
MX165C	Low Voltage CTCSS Encoder/Decoder with Tx/Rx Filters	3
MX315A	CTCSS Encoder	19
MX375	*Pvt*SQUELCH™ CTCSS Encoder/Decoder	29
MX465	Low Voltage CTCSS Encoder/Decoder with Tx/Rx Filters	45
MX805A	Sub-Audio Signaling Processor	61
MX818	CTCSS Signaling Processor	79
MX828	CTCSS/DCS/SelCall Processor	107

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX165C

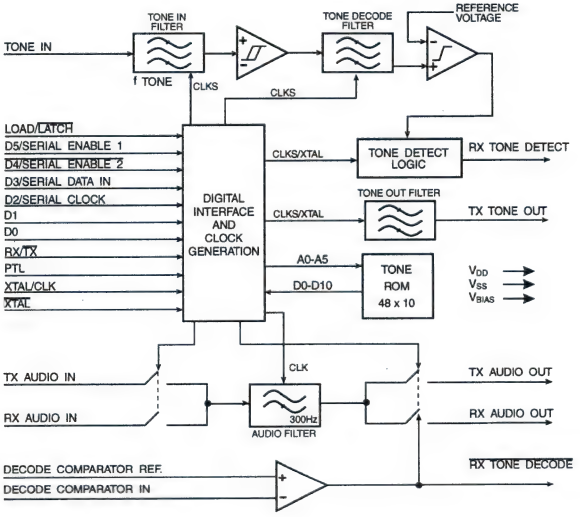
Low Voltage CTCSS Encoder/Decoder with TX/RX Filters

Features

- Meets TIA/EIA-603 Standards
- 47 CTCSS Tones + Notone
- TX/RX Speech Filters
- Improved Sinad
- Serial or Parallel Programming
- Easy µP Interface
- Scanning on any Channel
- Standard 1MHz Xtal (See MX465 for 4MHz)
- Low Voltage 3.3V to 5.0V

Applications

- Mobile Radio Channel Sharing
- Scan Trunking
- Wireless Intercom Traffic Control
- Hookswitch Supervision
- Repeater Control



The MX165C CTCSS Encoder/Decoder is a low voltage, CMOS device that meets TIA/EIA-603 Standards. The MX165C will encode and decode the tones 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz in addition to the 39 standard CTCSS tones, for a total of 47 CTCSS tones + Notone. With the incorporation of the on-chip TX and RX speech filter, the MX165C enhances voice/tone multiplexing by attenuating TX and RX speech 36dB at frequencies below 250Hz while passing signals > 300Hz with only 1dB of ripple. This not only minimizes CTCSS talk-off in the TX mode but also improves Hum and Noise performance in the RX mode.

Available in the following package styles: 24-pin TSSOP (MX165CTN), 24-pin SOIC (MX165CDW), 24-pin PLCC (MX165CLH), and 24-pin PDIP (MX165CP), the MX165C requires a single 3.3V to 5.0V supply and a 1MHz clock or crystal.

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480102.008

CONTENTS

Section **Page**

1. Block Diagram **3-5**

2. Signal List **3-6**

3. External Components **3-8**

4. General Description **3-9**

4.1 Description 3-9
4.2 I/O Conditions 3-9
4.3 Filter Response 3-10
4.4 Serial and Parallel Mode Timing 3-10
4.5 CTCSS Programming 3-12

5. Performance Specification **3-13**

5.1 Electrical Performance 3-13
5.1.1 Absolute Maximum Ratings 3-13
5.1.2 Operating Limits 3-13
5.2 Packaging 3-16

MX•COM, Inc. Reserves the right to change specifications at any time and without notice

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Block Diagram

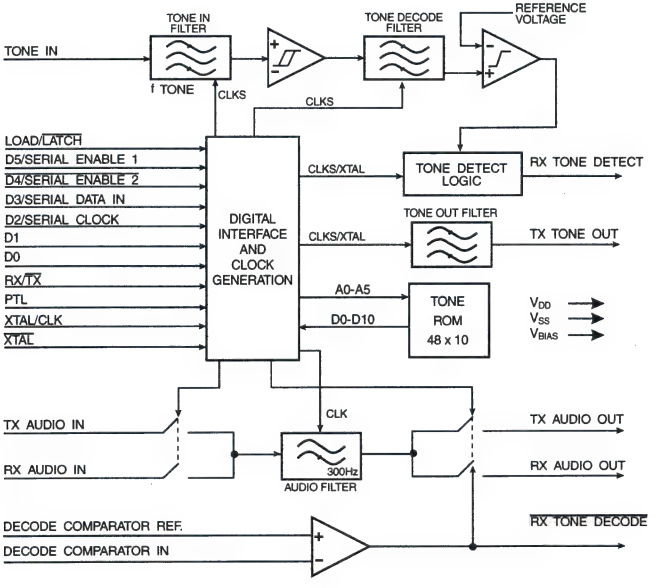


Figure 1 : Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Signal List

Pin No.	Signal	Type	Description
1	V_{DD}	power	Positive supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
2	XTAL/CLOCK	input	Input to the on-chip inverter used with a 1MHz Xtal or external clock source.
3	$\overline{XTAL}$	output	Output of the on-chip inverter (clock output).
4	LOAD/$\overline{LATCH}$	input	Controls 8 on-chip latches. It is used to latch RX / $\overline{TX}$, PTL, and D0-D5. A logic 1 applied to this input places the 8 latches in the 'transparent' mode. A logic 0 applied to this input places the 8 latches in the 'latched' mode. In Parallel Mode, data is loaded and latched by a logic 1-0 transition (see Figure 4). In Serial Mode, data is loaded and latched by a 0-1-0 strobe pulse on this pin (see Figure 5). Internally pulled to V_{DD}
5	D5 / SERIAL ENABLE 1	input	Data input D5 (Parallel Mode). A logic 1 applied to this input together with a logic 0 applied to D4/$\overline{SERIAL\ ENABLE\ 2}$ will place the device in Serial Mode (see Figure 5). Internally pulled to V_{DD}.
6	D4 / $\overline{SERIAL\ ENABLE\ 2}$	input	Data input D4 (Parallel Mode). A logic 0 applied to this input together with a logic 1 applied to D5 / SERIAL ENABLE 1 will place the device in Serial Mode (see Figure 5). Internally pulled to V_{DD}.
7	D3 / SERIAL DATA IN	input	Data input D3 (Parallel Mode). In Serial Mode this pin becomes the serial data input for D5-D0, RX / $\overline{TX}$ and PTL (see Figure 5). D5 is clocked first and PTL last. Internally pulled to V_{DD}.
8	D2 / SERIAL CLOCK	input	Data input D2 (Parallel Mode). In Serial Mode this pin becomes the SERIAL CLOCK input. Data is clocked on the positive going edge (see Figure 5). Internally pulled to V_{DD}.
9	D1	input	Data input D1 (Parallel Mode). Internally pulled to V_{DD}.
10	D0	input	Data input D0 (Parallel Mode). Internally pulled to V_{DD}.
11	V_{SS}	power	Negative supply.
12	DECODE COMPARATOR REF.	input	Internally biased to $V_{DD}/3$ or 2 $V_{DD}/3$ via 1M resistors depending on the logic state of the $\overline{RX\ TONE\ DECODE}$ pin. $\overline{RX\ TONE\ DECODE}$ = 1 will bias this input 2 $V_{DD}/3$; a logic 0 will bias this input $V_{DD}/3$. This input provides the DECODE COMPARATOR REFERENCE voltage, and the switching of bias voltages provides hysteresis to reduce 'chatter' under marginal conditions.
13	$\overline{RX\ TONE\ DECODE}$	output	Gated output of the decode comparator. This output is used to gate the RX Audio path. A logic 0 on this pin indicates a successful decode and the DECODE COMPARATOR IN pin is more positive than the DECODE COMPARATOR REF. input (see Table 3).
14	DECODE COMPARATOR IN	input	Inverting input of the DECODE COMPARATOR. This pin is normally connected to the integrated output of the RX TONE DETECT line.
15	RX TONE DETECT	output	In RX mode this output will go to logic 1 during a successful decode. It must be externally integrated to control response and deresponse times (see Table 3).
16	TX TONE OUT	output	The CTCSS sinewave output appears on this pin under control of the RX / $\overline{TX}$ pin. When not transmitting a tone, TX TONE OUT may be biased to $V_{DD}/2$. (see Table 3).
17	RX / $\overline{TX}$	input	RX or TX modes selected in Parallel Mode (see Figure 4). In Serial Mode this function is serially loaded. This pin is internally pulled to V_{DD} via a 1MΩ resistor.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Pin No.	Signal	Type	Description
18	PTL	input	In RX mode this pin operates as a 'Push To Listen' function by enabling the RX audio path, thus overriding the tone squelch function (Parallel Mode). In Serial Mode this function is loaded serially. Internal pull-up to V_{DD}
19	RX AUDIO OUT	output	High pass filtered RX AUDIO OUT. This pin outputs audio when $\overline{\text{RX TONE DECODE}}$ = logic 0, PTL = logic 1, or when Notone is programmed (see Table 4). In TX mode this pin is biased to $V_{DD}/2$.
20	TX AUDIO OUT	output	High pass filtered TX AUDIO OUT pin. In TX mode this pin outputs audio present at the TX AUDIO IN pin. In RX mode this pin is biased to $V_{DD}/2$
21	V_{BIAS}	output	Output of an internally generated V_{DD} /2 bias level that would normally be externally bypassed to V_{SS} via capacitor C6.
22	TX AUDIO IN	input	In TX mode TX AUDIO IN may be prefiltered, using the TX Audio path, thus helping to avoid talk-off due to intermodulation of speech frequencies with the transmitted CTCSS tone. Internally biased to $V_{DD}/2$.
23	RX AUDIO IN	input	Input to the audio high pass filter in RX mode. Internally biased to $V_{DD}/2$.
24	TONE INPUT	input	Input to the CTCSS tone detector. Internally biased to $V_{DD}/2$.

Table 1: Signal List

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

External Components

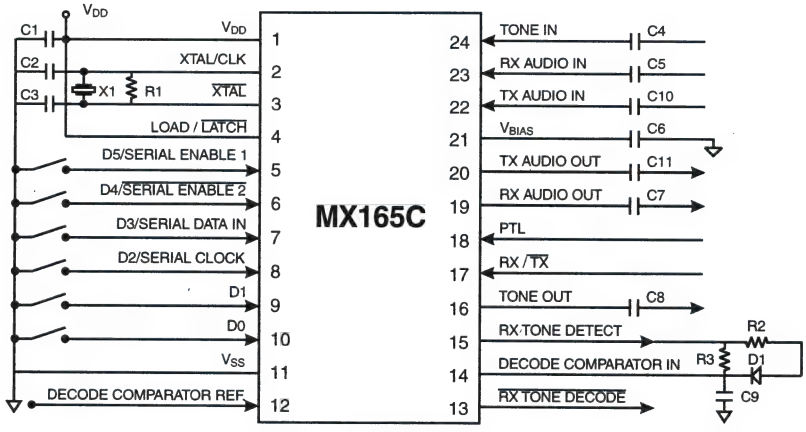


Figure 2 : Recommended External Components for Typical Application

R1	Note 1	4.7MΩ	±10%
R2		560kΩ	±10%
R3		820kΩ	±10%
C1		0.1µF	±20%
C2	Note 1	18pF	±20%
C3	Note 1	33pF	±20%
C4	Note 2	0.1µF	±20%
C5	Note 2	0.1µF	±20%

C6		0.47µF	±20%
C7	Note 2	0.1µF	±20%
C8	Note 2	0.1µF	±20%
C9	Note 2	0.1µF	±20%
C10	Note 2	0.1µF	±20%
C11	Note 2	0.1µF	±20%
D1		small signal	
X1	Note 1	1MHz	100ppm max.

Table 2: External Components

External Components Notes:

1. The values specified for R1, C2, and C3 have been found to be satisfactory when used with a crystal (X1) whose equivalent series resistance is ≤ 1000Ω. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. The 0.1µF value for the DC Blocking capacitors, C4, C5, C7, C8, C9, C10, and C11 is not a requirement. For the capacitors C4, C5, and C10, the input impedance is internal to the device and specified typical as 550kΩ. For the remaining capacitors external circuits will be important in determining the input impedance.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

General Description

Description

Voice on shared radio channels are multiplexed with a subaudible CTCSS (Continuous Tone Controlled Subaudible Squelch) tone as a means of directing messages among user groups sharing the same RF frequencies. CTCSS modulates the transmitter with a discrete tone, from 39 standard CTCSS tones in the range (67.0Hz to 250.0Hz) according to TIA/EIA-603. There are an additional eight CTCSS tones not specified in TIA/EIA-603 that the MX165C will encode and decode. They are : 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz, for a total of 47 CTCSS tones plus Notone.

The MX165C also incorporates TX/RX on chip speech filters. In early CTCSS designs, TX speech was not filtered from the CTCSS tone, rather the filtering was dependent upon the host transmitter's pre-emphasis network. At only 6dB/octave, the attenuation of speech components at higher CTCSS tones was only a few dB which resulted in talk-off (low frequency voice components unsquelching the receiver audio).

I/O Conditions

D0-D5	Tone	No Tone	Tone	Tone	Tone	No Tone
Input Pins Condition						
RX / $\overline{TX}$	0	0	1	1	1	1
PTL	0	X	0	1	X	X
Decode Comparator In	X	X	0	0	1	X
Output Pins Condition						
RX TONE DETECT	0	0	0	0	1	X
$\overline{RX\ TONE\ DECODE}$	1	1	1	1	0	0
Result / Function						
Tone Transmitter Enabled	Yes	No (Bias)	No (Bias)	No (Bias)	No (Bias)	No (Bias)
TX Audio Path Enabled	Yes	Yes	No	No	No	No
Tone Decode Enabled	No	No	Yes	Yes	Yes	Yes
RX Audio Path Enabled	No (Bias)	No (Bias)	No (Bias)	Yes	Yes	Yes
Notes	1	2	3	4	5	6

Notes:

1. Normal tone transmit condition.
2. Notone programmed in TX mode, tone transmit output set to $V_{DD}/2$. TX audio path enabled.
3. Normal decode standby.
4. Normal decode standby with PTL used to enable audio.
5. Normal decode of correct CTCSS tone condition, PTL has no effect.
6. Notone programmed in RX mode, tone transmit output (Bias). RX audio path enabled.
7. X = don't care

Table 3: Combinations of Input / Output conditions

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Filter Response

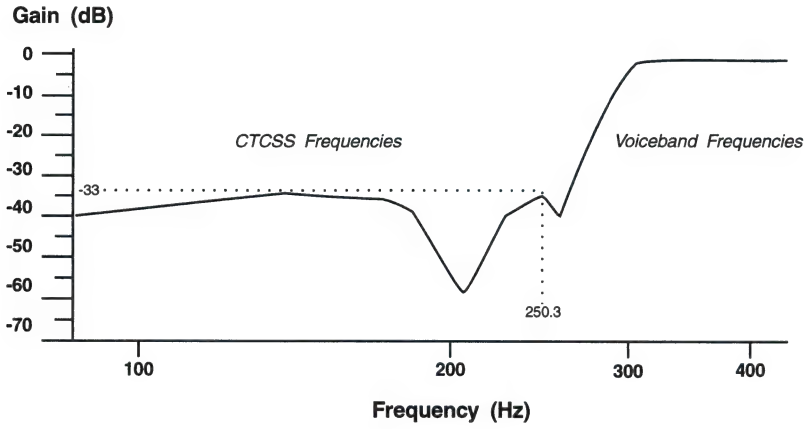


Figure 3 : Voiceband Filter Response

Serial and Parallel Mode Timing

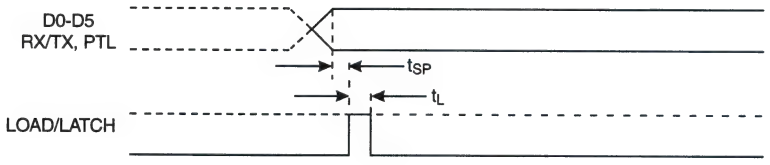
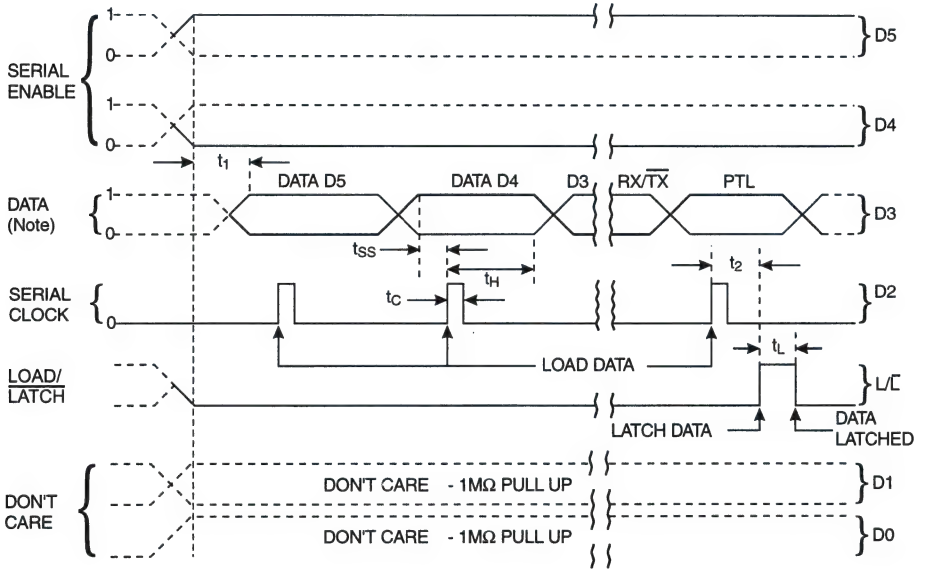


Figure 4 : Parallel Mode

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



Note : Serial bit 1 through bit 8 = D5, D4, D3, D2, D1, D0, RX/TX and PTL respectively. Load bit 1 first, bit 8 last

Figure 5 : Serial Mode

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

CTCSS Programming

	Tone			Programming Inputs						
	Nominal Frequency (Hz)	MX165C Frequency (Hz)	Δf_0 (%)	D5	D4	D3	D2	D1	D0	Hex
	67.0	66.98	-0.029	1	1	1	1	1	1	3F
	69.3	69.32	0.024	1	1	1	0	0	1	39
	71.9	71.901	0.001	0	1	1	1	1	1	1F
	74.4	74.431	0.042	1	1	1	1	1	0	3E
	77.0	76.965	-0.046	0	0	1	1	1	1	0F
	79.7	79.677	-0.029	1	1	1	1	0	1	3D
	82.5	82.483	-0.021	0	1	1	1	1	0	1E
	85.4	85.383	-0.020	1	1	1	1	0	0	3C
	88.5	88.494	-0.007	0	0	1	1	1	0	0E
	91.5	91.456	-0.048	1	1	1	0	1	1	3B
	94.8	94.76	-0.042	0	1	1	1	0	1	1D
	97.4	97.435	-0.036	1	1	1	0	1	0	3A
	100.0	99.96	-0.040	0	0	1	1	0	1	0D
	103.5	103.429	-0.069	0	1	1	1	0	0	1C
	107.2	107.147	-0.05	0	0	1	1	0	0	0C
	110.9	110.954	0.049	0	1	1	0	1	1	1B
	114.8	114.84	0.035	0	0	1	0	1	1	0B
	118.8	118.793	-0.006	0	1	1	0	1	0	1A
	123.0	123.028	0.023	0	0	1	0	1	0	0A
	127.3	127.328	0.022	0	1	1	0	0	1	19
	131.8	131.674	-0.095	0	0	1	0	0	1	09
	136.5	136.612	0.082	0	1	1	0	0	0	18
	141.3	141.323	0.016	0	0	1	0	0	0	08
	146.2	146.044	-0.107	0	1	0	1	1	1	17
	151.4	151.441	0.027	0	0	0	1	1	1	07
	156.7	156.875	0.112	0	1	0	1	1	0	16
•	159.8	159.936	0.085	1	1	0	0	0	1	31
	162.2	162.311	0.069	0	0	0	1	1	0	06
	167.9	167.708	-0.114	0	1	0	1	0	1	15
	173.8	173.936	0.078	0	0	0	1	0	1	05
	179.9	179.654	-0.137	0	1	0	1	0	0	14
•	183.5	183.680	0.098	1	1	0	0	1	0	32
	186.2	186.289	0.048	0	0	0	1	0	0	04
•	189.9	190.069	0.089	1	1	0	0	1	1	33
	192.8	192.864	0.033	0	1	0	0	1	1	13
•	196.6	196.329	-0.138	1	1	0	1	0	0	34
•	199.5	199.312	-0.094	1	1	0	1	0	1	35
	203.5	203.645	0.071	0	0	0	0	1	1	03
•	206.5	206.207	-0.142	1	1	0	1	1	0	36
	210.7	210.848	0.070	0	1	0	0	1	0	12
	218.1	217.853	-0.113	0	0	0	0	1	0	02
	225.7	225.339	-0.160	0	1	0	0	0	1	11

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

	Tone			Programming Inputs						
	Nominal Frequency (Hz)	MX165C Frequency (Hz)	Δ f_0 (%)	D5	D4	D3	D2	D1	D0	Hex
•	229.1	229.279	0.078	1	1	0	1	1	1	37
	233.6	233.359	-0.103	0	0	0	0	0	1	01
	241.8	241.970	0.070	0	1	0	0	0	0	10
	250.3	250.282	-0.007	0	0	0	0	0	0	00
•	254.1	254.162	0.024	1	1	1	0	0	0	38
	Notone		N/A	1	1	0	0	0	0	30
	Serial input mode		N/A	1	0	Data	Clock	X	X	2X

• Not specified in the TIA/EIA tone set

Table 4: CTCSS Tones

Performance Specification

Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device. Operation of the device outside the operating limits is not implied.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
any other pins	-20	20	mA
TN / DW / LH / DIP Package			
Total Allowable Power Dissipation at T_{AMB} =25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating temperature	- 40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	2.7	5.5	V
Xtal Frequency	1.0	1.0	MHz
Operating Temperature	-40	85	°C

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Operating Characteristics

For the following conditions unless otherwise specified

V_{DD} = 3.3V / 5.0V at T_{AMB} = 25°C, V_{SS} = 0V,
Xtal Frequency = 1.0 MHz, 100ppm max.
(Over the life of the Xtal the operating range may vary from 100ppm up to 1000ppm)
0dB ref. = 750mV_{RMS} (proportional to V_{DD}; see note 17)

Composite Signal:
1kHz test tone = 300mV_{RMS}, f_0 CTCSS tone = 30 mV_{RMS}, 75mV_{RMS} Noise (band limited to 6kHz Gaussian)

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply voltage		2.7	3.3/5.0	5.5	V
Supply current					
V_{DD} = 5.0V			3.2	4.2	mA
V_{DD} = 3.3V			1.1	1.6	mA
Rx Monitor			2.0		mA
Analog input impedance	18	480	550		kΩ
Analog output impedance	18		400	1000	Ω
Digital Input impedance	1,18	25	40		kΩ
Input logic 1	1	70%V_{DD}			V
Input logic 0	1			30%V_{DD}	V
Output Logic 1 source = 0.1mA	2	80%V_{DD}			V
Output Logic 0 sink = 0.1mA	2			20%V_{DD}	V
Dynamic Values					
Speech filter					
Total harmonic distortion	5,8,19		0.7	1.5	%
Output noise level (input ac short circuit, audio switch enabled)	8,18		0.5	1.0	mV_{RMS}
Sinad	8,9	40	50		dB
Spurious emissions	18			- 48	dB
Cutoff frequency			300		Hz
Bandpass ripple	8		1	1.8	dB
Stopband attenuation <250Hz	7,8,19	33	36		dB
Passband gain 1kHz		- 0.5	0	0.5	dB
TX/RX isolation	5		60		dB
Encoder					
Tone output level	12	-1.0	0	1.0	dB
Tone Frequency Accuracy (f error)		- 0.3		0.3	%f_0
Risetime to 90% nominal output					
f_0>100Hz	4,10		15	75	ms
f_0<100Hz	4,10		45	120	ms
Total Harmonic Distortion	19		1.5	2	%

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

	Notes	Min.	Typ.	Max.	Units
Decoder					
Pure tone decode threshold	19		7	15	mV_{RMS}
Composite signal decode threshold	3			30	mV_{RMS}
Decode input signal level	16	-20		3.5	dB
Pure tone decode response time	13,14	95	115	140	ms
Pure tone decode deresponse time	13,15	95	130	170	ms
Decode response time	3,6,10			250	ms
Deresponse time	3,10		180	250	ms
Decode selectivity:					
Upper decode band edge	3,11,19,20	$1.005f_0$	$1.015f_0$	$0.995f_{0+1}$	Hz
Lower decode band edge	3,11,19,20	$1.005f_{0-1}$	$0.985f_0$	$0.995f_0$	Hz
Serial / Parallel Inputs					
Parallel Set Up Time (t_{SP})		400			ns
Load / Latch Pulse Width (t_L)		400			ns
Serial Clock Pulse Width (t_C)		400			ns
Serial Data Set-Up Time (t_{SS})		400			ns
Serial Data Hold Time (t_H)		400			ns
Serial Enable Time (t_1)		400			ns
Serial Load / Latch Set-Up Time (t_2)		400			ns
Serial Clock Frequency			1		MHz

Operating Characteristics Notes:

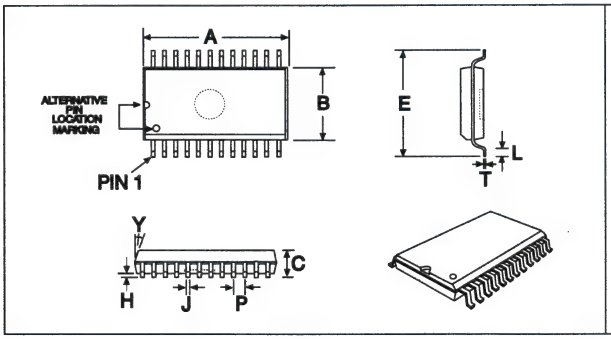
1. Refers to RX/TX, PTL, Decode Comparator Input, D0-D5.
2. All logic outputs.
3. Composite signal test condition.
4. Any programming tone and R_L = 10kΩ, C_L = 15pF.
5. With an input level of 0dB @1kHz
6. f_0>100Hz (for 100 Hz> f_0>67Hz: t=100/ f_0Hz x 250ms)
7. See Figure 3.
8. Measured in a 30kHz bandwidth.
9. With an input level of -3.5dB @1kHz
10. Per TIA/EIA-603.
11. Per TIA/EIA-603, device will not decode adjacent TIA/EIA-603 Tones.
12. Tone output level is proportional to V_{DD}.
13. f_0=156.7Hz @ -20dB.
14. Typically 12.5 Tone Cycles + 40ms.
15. Typically 7 Tone Cycles + 90ms.
16. Max composite signal is 3.5dB with:
    Noise (band limited 6kHz Gaussian) = -12dB ref. to 1kHz test tone
    f_0 CTCSS tone = -20dB ref. to 1kHz test tone
17. For maximum dynamic range, set audio level to 0dB, V_{DD} x150mV_{RMS}, using minimum V_{DD} under which system is intended to work. (e.g. for a 2.7V system, use 0dB equal to 405mV_{RMS}).
18. By characterization only.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

19. Batch sampled only
20. For example, if: f_0 = 100.0Hz (f_{0-1} = 97.4Hz f_{0+1} = 103.5Hz)

Decode Selectivity	Min	Typ	Max	Unit
Upper Decode Band Edge	100.5	101.5	102.98	Hz
Lower Decode Band Edge	97.89	98.5	99.5	Hz

Packaging

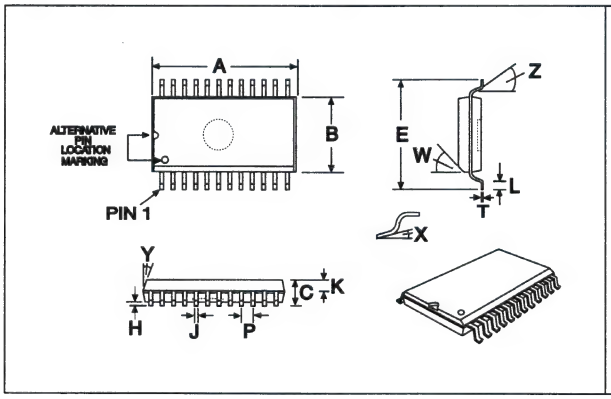


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin TSSOP Mechanical Outline: Order as part no. MX165CTN



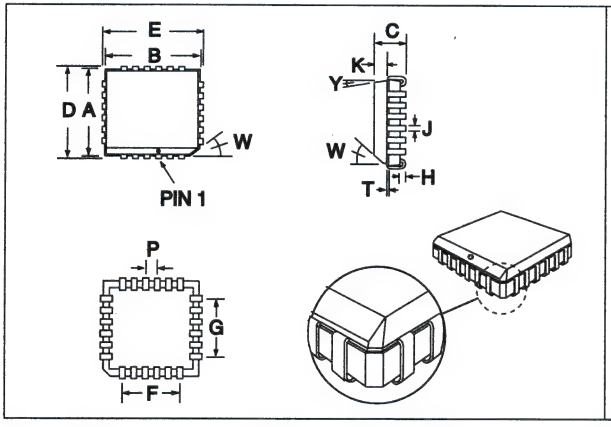
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 24-pin SOIC Mechanical Outline: Order as part no. MX165CDW

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

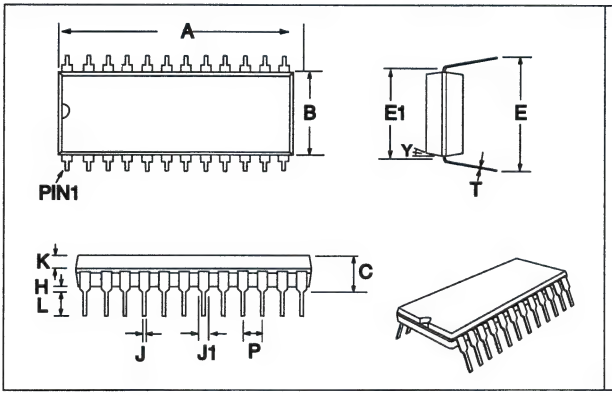


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin PLCC Mechanical Outline: Order as part no. MX165CLH



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 24-pin PDIP Mechanical Outline: Order as part no. MX165CP

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480102.008
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX315A

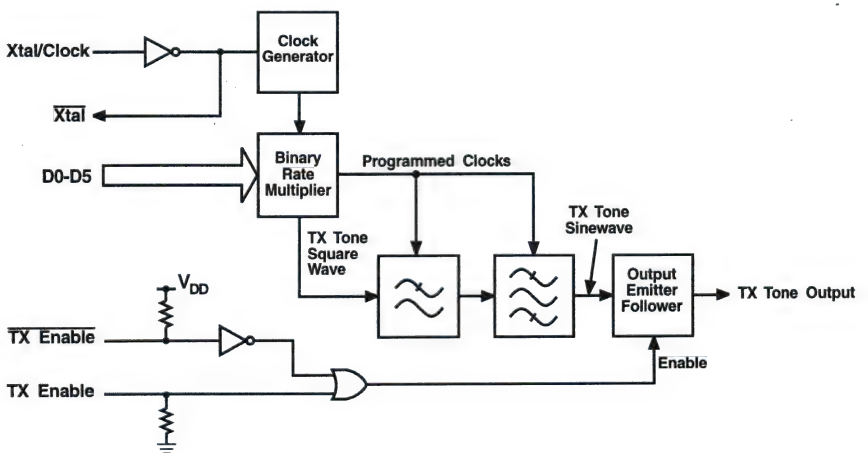
CTCSS Encoder

Features

- Field Programmable Tone Encoder
- 40 CTCSS Frequencies
- Crystal-Controlled Frequency Stability
- Low Distortion Sinewave Output
- Few External Components Required
- CMOS Low Power Requirements

Applications

- Mobile Radio Base Stations & Repeater Stations
- Mobile Radios
- Hand-Held Radios
- Industrial Controls
- Intercom Systems
- Door-Entry Systems



The MX315A is a monolithic CMOS tone encoder for sub-audible tone squelch systems, which provides three additional frequencies over the earlier MX315A. These frequencies are 69.3, 97.4 and 206.5Hz. The tone frequencies are derived from an input reference frequency. An on-chip inverter is provided to drive an external crystal circuit.

Tone selection is achieved through six programming inputs and two control inputs (which allow either a logic "1" or "0" to enable the device). A low distortion sinewave is generated at the TX Tone Output when the MX315A is enabled. The emitter follower output stage can source 1mW directly into a 600Ω load (0dBm).

The MX315A is available in the following package styles: 16-pin SOIC (MX315ADW), 14-pin PDIP (MX315AP) and 14-pin CDIP (MX315AJ).

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480054.005
All Trademarks and service marks are held by there respective companies.

CONTENTS

Section **Page**

1. Block Diagram **3-21**

2. Signal List **3-22**

3. External Components **3-23**

4. Application **3-24**

4.1 Interfacing and Electromagnetic Capability 3-24

4.2 CTCSS Programming 3-25

5. Performance Specification **3-26**

5.1 Electrical Performance 3-26

5.2 Packaging 3-27

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All Trademarks and service marks are held by there respective companies.
Doc. # 20480054.005

1. Block Diagram

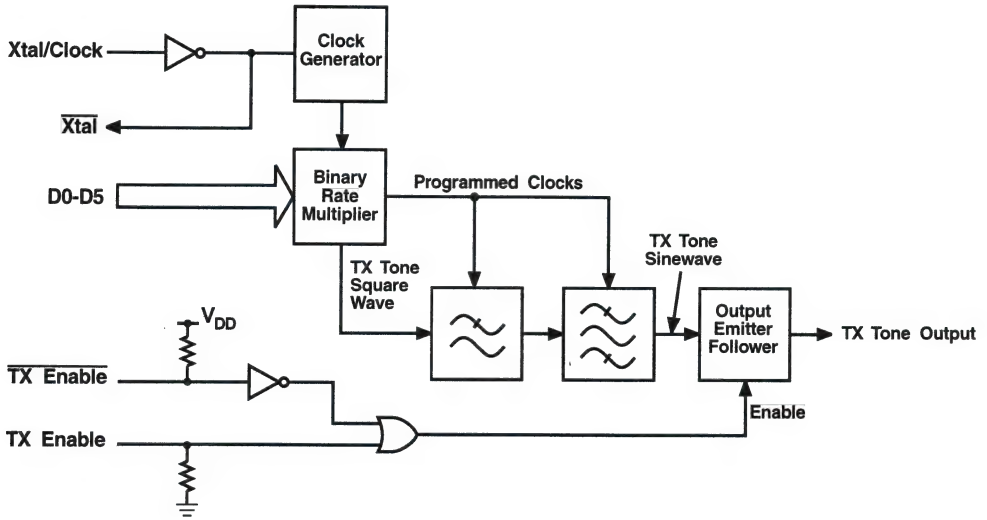


Figure 1: Device Block Diagram

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All Trademarks and service marks are held by there respective companies.
Doc. # 20480054.005

2. Signal List

Pin No.		Name	Description
J,P	DW		
1	1	D3	D0-D5 are tone select inputs with internal pull-up resistors. The logic combination at these inputs determines the encoded CTCSS tone. See Table 1. The input sequence is not latched and may be changed at any time. A logic "1" will be programmed if the input is open circuit, allowing the use of SPST switches.
2	2	D2	
3	3	D1	
4	4	D0	
5	5	D4	
6	6	D5	
7	7	V_{SS}	Negative Supply Voltage.
8	8	Xtal/Clock In	This is the input to the CMOS inverter. It can be used in conjunction with the Xtal output to form the active element in a crystal oscillator circuit. Alternatively, a logic level 1MHz frequency can be injected at this pin. However, the supply voltage should never be applied without the input clock signal.
9	9	$\overline{\text{Xtal}}$ Output	This is the output of the CMOS inverter. When used as a crystal oscillator, track lengths and loading of this pin should be minimized.
10	10	Internal Connection	Do not use
	11	N/C	
	12	N/C	
11	13	TX Tone Output	This is the tone output pin. It includes a low impedance emitter follower stage for sourcing sinusoidal tone. The tone is generated about a DC level of approximately 1/2 V_{DD}. The pin is high impedance when not encoding.
12	14	$\overline{\text{TX Enable}}$ Input	This logic input has an internal pull-up resistor. A logic "0" at this pin enables the MX315A.
13	15	TX Enable Input	This logic input has an internal pull-down resistor. A logic "1" at this pin enables the MX315A.
14	16	V_{DD}	Positive Supply Voltage.

Table 1: Signal List

© 1996 MX•COM, INC. Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480054.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All Trademarks and service marks are held by there respective companies.

3. External Components

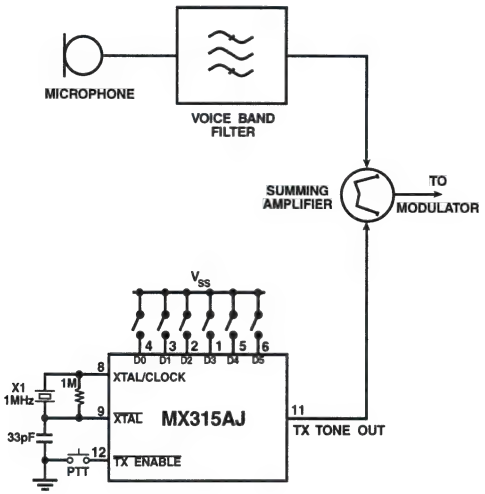


Figure 2: External Components

R1	Note 1	1M	±20%
C1		33pF	±20%
X1	Note 2, 3	1MHz	±0.19%

Table 2: Recommended External Components

Notes:

1. The 1MΩ resistor is used to bias the internal CMOS inverter into its linear mode. A tolerance of ±20% is acceptable.
2. "X1" is a parallel resonant crystal. A reference frequency of 1 MHz ±0.19% is required to maintain a tone accuracy within 0.5%.
3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All Trademarks and service marks are held by there respective companies.
Doc. # 20480054.005

4. Application

The MX315A is dedicated to Continuous Tone-controlled Squelch Systems (CTCSS) in radio applications. However, it can be used wherever encoding of low-frequency tones is required, such as intercoms, door-entry systems and various industrial applications.

The performance of a CTCSS system can be degraded if speech frequencies in the signaling spectrum are not removed prior to transmission. This can be accomplished by filtering the microphone signals to attenuate frequencies below 250 Hz. Figure 2 illustrates the addition of TX Tone Output to the filtered microphone signals prior to modulation. Figure 3 illustrates the TX Tone Output sequence and a typical spectral analysis.

Where two or more circuits are required to use a single oscillator (i.e. repeater applications), the signal at $\overline{Xtal}$ can be used to drive one additional Xtal/Clock input. Any further circuits can be driven from the buffered $\overline{Xtal}$ output of the second device.

The program code can be set on the D0-D5 inputs by hardwired logic levels or SPST switches to V_{SS}, as illustrated in Figure 2 (allowing the internal pull-up resistors to program a logic "1").

The MX315A provides both a $\overline{TX\ Enable}$ input and a TX Enable input. Either input can be used to enable the tone output, with the unused pin left open circuit (internal resistors establish a valid logic level and prevent damage). Any configuration of PTT switch or TX signal can therefore be interfaced.

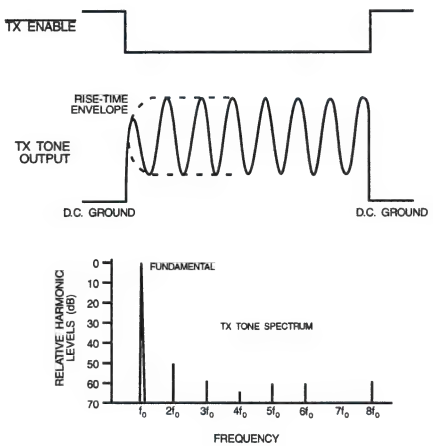


Figure 3: Tone Encoding Sequence and Spectral Response

4.1 Interfacing and Electromagnetic Capability

The MX315A requires a clock of 1MHz, which is internally converted to logic level square waves. Consideration should therefore be given to possible interference problems with RF or IF circuitry caused by 1MHz or its harmonics.

A decoupling capacitor can be used to reduce ripple on the power supply. This will reduce the level of superimposed noise on the supply caused by internal switching transients (particularly at 1MHz and f_0).

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All Trademarks and service marks are held by there respective companies.
Doc. # 20480054.005

4.2 CTCSS Programming

Tone			Programming Inputs						
Nominal Frequency (Hz)	MX315A Freq. (Hz)	Δfo (%)	D5	D4	D3	D2	D1	D0	Hex
67.0	67.06	+.10	1	1	1	1	1	1	3F
69.3	69.37	+.10	1	1	1	0	0	1	39
71.9	71.84	-.08	0	1	1	1	1	1	1F
74.4	74.33	-.10	1	1	1	1	1	0	3E
77.0	76.99	-.02	0	0	1	1	1	1	0F
79.7	79.65	-.06	1	1	1	1	0	1	3D
82.5	82.50	0.0	0	1	1	1	1	0	1E
85.4	85.34	-0.7	1	1	1	1	0	0	3C
88.5	88.62	+.14	0	0	1	1	1	0	0E
91.5	91.38	-.13	1	1	1	0	1	1	3B
94.8	94.88	+.08	0	1	1	1	0	1	1D
97.4	97.46	+.06	1	1	1	0	1	0	3A
100.0	99.87	-.13	0	0	1	1	0	1	0D
103.5	103.39	-.11	0	1	1	1	0	0	1C
107.2	107.17	-.03	0	0	1	1	0	0	0C
110.9	110.85	-.04	0	1	1	0	1	1	1B
114.8	114.80	0.0	0	0	1	0	1	1	0B
118.8	118.60	-.17	0	1	1	0	1	0	1A
123.0	123.12	+.10	0	0	1	0	1	0	0A
127.3	127.50	+.16	0	1	1	0	0	1	19
131.8	131.67	-.10	0	0	1	0	0	1	09
136.5	136.69	+.14	0	1	1	0	0	0	18
141.3	141.48	+.13	0	0	1	0	0	0	08
146.2	145.96	-.16	0	1	0	1	1	1	17
151.4	151.45	+.03	0	0	0	1	1	1	07
156.7	156.59	-.07	0	1	0	1	1	0	16
162.2	162.10	-.06	0	0	0	1	1	0	06
167.9	168.01	+.07	0	1	0	1	0	1	15
173.8	173.43	-.21	0	0	0	1	0	1	05
179.9	180.21	+.17	0	1	0	1	0	0	14
186.2	186.46	+.14	0	0	0	1	0	0	04
192.8	193.16	+.19	0	1	0	0	1	1	13
203.5	202.88	-.31	0	0	0	0	1	1	03
206.5	206.78	+.14	1	1	1	0	0	0	38
210.7	210.84	+.07	0	1	0	0	1	0	12
218.1	217.96	-.07	0	0	0	0	1	0	02
225.7	225.58	-.05	0	1	0	0	0	1	11
233.6	233.75	+.07	0	0	0	0	0	1	01
241.8	242.54	+.31	0	1	0	0	0	0	10
250.3	250.06	+.10	0	0	0	0	0	0	00
Test	4032	0.0	1	1	0	0	1	1	*33

* - or any invalid address

Table 3: CTCSS Tones

© 1996 MX•COM, INC. Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480054.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All Trademarks and service marks are held by there respective companies.

5. Performance Specification

5.1 Electrical Performance

5.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply Voltage	-0.3	7.0	V
J / P /DW Packages			
Total Allowable Device Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C
Operating Temperature	-30	+85	°C
Storage Temperature	-55	+125	°C

5.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
V_{DD}		4.5	5.0	5.5	V
Operating Temperature		-30		85	°C
Clock	Note 1		1		MHz

Operating Limits Note:

1. "X1" is a parallel resonant crystal. A reference frequency of 1 MHz ±0.19% is required to maintain a tone accuracy within 0.5%.

5.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V , T_{AMB} = 25°C, Xtal Frequency = 1MHz

	Notes	Min.	Typ.	Max	Units
Supply Current (operating)			1.5	4.5	mA
Input Impedance	1		500		kΩ
Input Impedance	2		10		MΩ
Logic Input "1"		3.5			V
Logic Input "0"				1.5	V
TX Output EMF	3	550	775		mV_{RMS}
TX Risetime			1		ms
TX Tone Output Load Current				5	mA
TX Distortion	3		2	5	%
Variation in Output Level Between Tones	3		0.1		dB

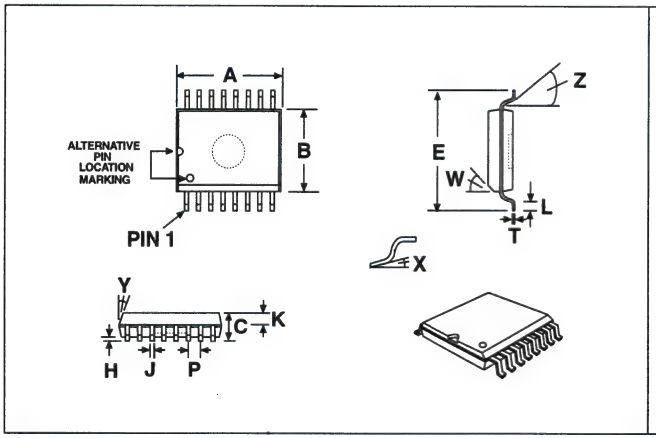
Operating Characteristics Notes:

1. Refers to D0, D1, D2, D3, D4, D5, TX Enable and $\overline{\text{TX Enable}}$ inputs
2. Refers to Xtal/Clock input

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All Trademarks and service marks are held by there respective companies.
Doc. # 20480054.005

3. Any program tone and R_L = 600Ω, C_L = 15pF. THD measurements are taken in the 0-6 kHz bandwidth.

5.2 Packaging

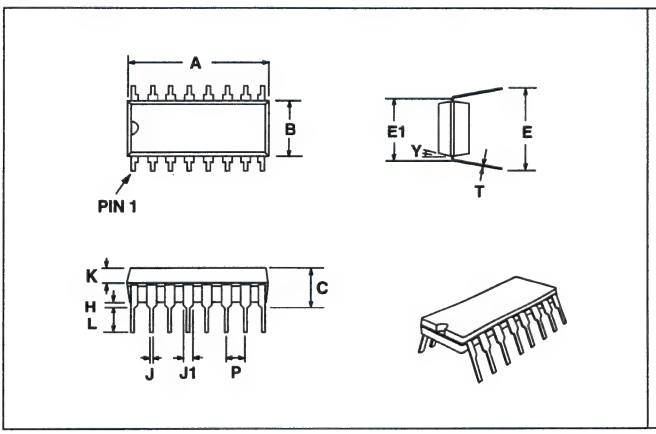


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 4: 16-pin SOIC Mechanical Outline: Order as part no. MX315ADW



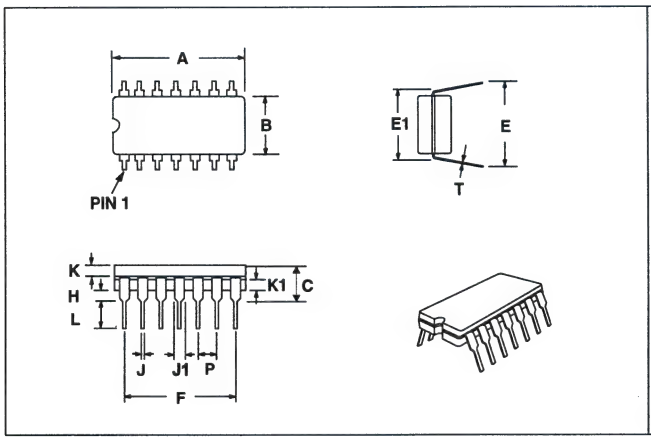
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 16-pin PDIP Mechanical Outline: Order as part no. MX315AP

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480054.005
All Trademarks and service marks are held by there respective companies.



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.754 (19.15)		0.766 (19.46)
B	0.240 (6.10)		0.288 (7.32)
C	0.165 (4.19)		0.230 (5.84)
E	0.360 (9.14)		0.420 (10.67)
E1	0.305 (7.75)		0.315 (8.00)
F		0.600 (15.24)	
H		0.015 (0.38)	
J		0.018 (0.46)	
J1		0.060 (1.52)	
K	0.053 (1.35)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.100 (2.54)	
T		0.010 (0.254)	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin CDIP Mechanical Outline: Order as part no. MX315AJ

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480054.005
All Trademarks and service marks are held by there respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX375

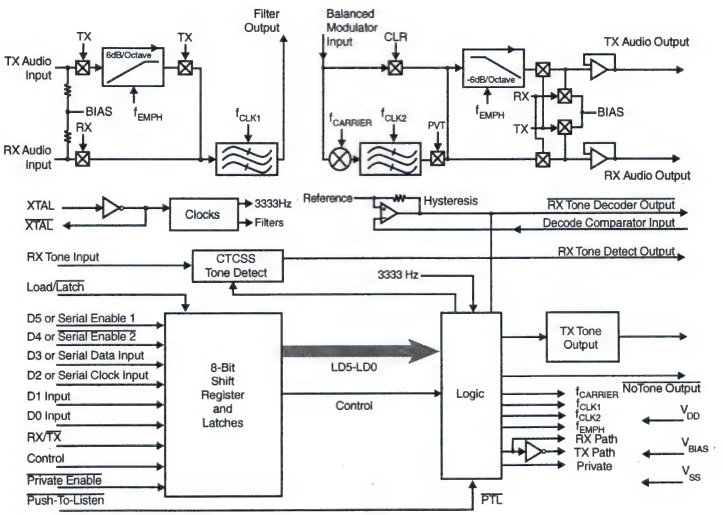
Pvt SQUELCH™ CTCSS Encoder/Decoder

Features

- PRIVATE/CLEAR CAPABILITY
- ON-CHIP TX AUDIO PRE/DEEMPHASIS
- ALTERNATIVE TO STANDARD CTCSS "PARTY LINE"
- POWERSAVE OPTION

Applications

- MOBILE RADIOS
- COMMUNITY REPEATERS
- TELEPHONE/RADIO INTERCONNECT SYSTEMS



The MX375 is a CMOS LSI microcircuit which combines CTCSS Encode/Decode operation with voice band frequency inversion. Frequency inversion is achieved by modulating the input audio with a 3333 Hz carrier frequency. Higher voice band frequencies are translated downward, and lower frequencies upward, resulting in a "mirror image" voice transmission. *Pvt*SQUELCH™ combines CTCSS with inverted speech to prevent users from understanding each other's communications unless the transmissions are accompanied by the group's assigned tone. Its net effect is to eliminate casual eavesdropping and give mobile radio users a certain degree of privacy at a minimal price. Up to 38 *Pvt*SQUELCH user groups (one per CTCSS tone) can share a single radio channel. With *Pvt*SQUELCH, competing businesses can share a radio channel without compromising communications security.

Device features: 1) serial or parallel tone programming capability (serial or parallel offered on MX375J, P & LH8), 2) the ability to operate under NOTONE conditions, 3) on-chip Tx and Rx audio filtering, 4) pin-selectable Private/Clear operation, and 5) pre/deemphasis filters in the Tx path, for optimal recovered audio quality.

A low-cost 4 MHz crystal/clock and a single 5V supply are required for operation. The MX375 is available in the following package styles: 28-pin PDIP (MX375P), 28-pin CDIP (MX375J) 28-pin PLCC (MX375LH8), and 24-pin PLCC (MX375LH).

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480026.007
All trademarks and service marks are held by their respective companies.

CONTENTS

Section **Page**

1. Block Diagram 3-31

2. Signal List 3-32

3. External Components 3-34

4. General Description 3-35

4.1.1 Pre- and De-emphasis 3-35

4.1.2 Functions and Outputs 3-35

5. Application 3-36

5.1.1 CTCSS Programming 3-36

6. Performance Specification 3-37

6.1 Electrical Performance 3-37

6.2 Timing Information 3-40

6.2.1 Serial Loading 3-40

6.2.2 Parallel Loading 3-41

6.3 Packaging 3-41

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1. Block Diagram

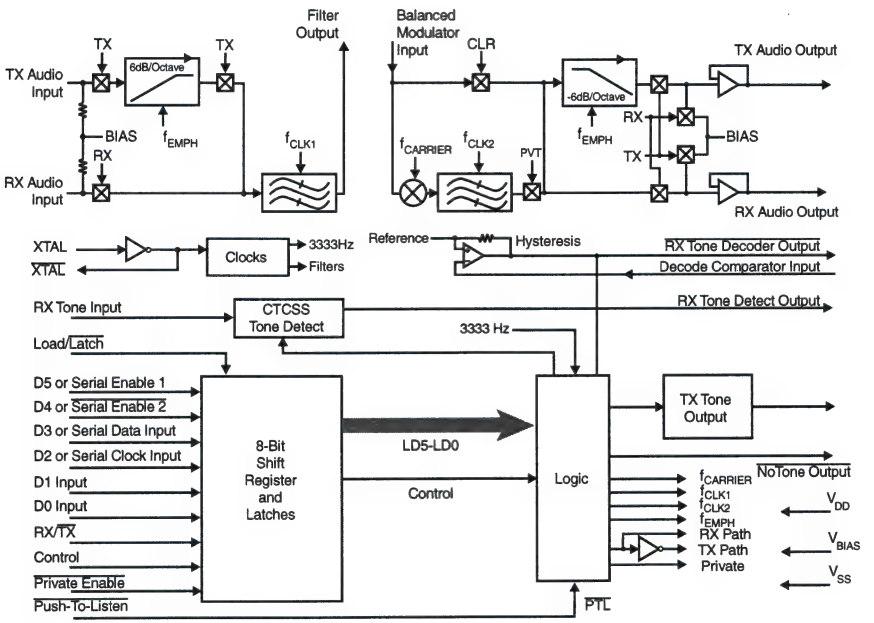


Figure 1: Device Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. Signal List

Pin No.		Name	Type	Description
LH	J,P,LH8			
1	28	V_{DD}	power	5V supply pin.
2	1	XTAL/CLOCK	input	This is the input to the clock oscillator inverter. An external 4 MHz Xtal or clock input should be applied to this pin.
3	2	$\overline{\text{XTAL}}$	output	This is the 4 MHz output of the clock oscillator inverter.
4	3	LOAD/$\overline{\text{LATCH}}$	input	This input controls the eight input latches: RX/$\overline{\text{TX}}$, $\overline{\text{PrivateEnable}}$, and D0-D5, as detailed in Table 5. Alternatively, the RX/$\overline{\text{TX}}$ and $\overline{\text{PrivateEnable}}$ inputs can be addressed separately by setting the Load/$\overline{\text{Latch}}$ and Control inputs as shown in Table 5. 1 MΩ pullup.
5-7		D4-D2	input	Programming Inputs (Serial Mode Only): These are the $\overline{\text{RX}}$/TX tone programming and function inputs which enable the serial programming mode. With Load/$\overline{\text{Latch}}$ at logic "0" serial data is loaded in the following sequence: D5, D4, D3, D2, D1, D0, RX/$\overline{\text{TX}}$, $\overline{\text{PrivateEnable}}$. When these 8 bits have been clocked in on the rising clock edge, data is latched by strobing the Load/$\overline{\text{Latch}}$ input "0 - 1 - 0" (See Figure 5). Pin 5 (D4) = $\overline{\text{Serial Enable2}}$ Pin 6 (D3) = Serial Data Input Pin 7 (D2) = Serial Clock Input
	4-9	D5-D0	input	Parallel Programming Inputs: These are the RX/$\overline{\text{TX}}$ tone programming and function inputs which select the CTCSS tone (See Table 4). *For both Serial and Parallel Modes:* In RX, a NOTONE program enables RX Audio Output and forces the RX Tone Decode Output to a logic "0". In TX, a NOTONE program generates a constant V_{BIAS}-0.7V condition at the TX Tone Output pin. Each input has a 1 MΩ pullup resistor.
8	10	$\overline{\text{RX TONE}}$ $\overline{\text{DECODE}}$	output	The gated output of the decode comparator. In RX, a logic "0" indicates a valid CTCSS tone decode condition, or the presence of NOTONE programming. A logic "0" enables the RX audio path. In TX, this output is held at logic "1".
9	11	DECODE COMPARATOR	input	The voltage level at this pin is compared internally with a fixed reference level. A greater input level compared to the reference will result in a logic "0" at the RX Tone Decode output. This input should be externally connected to the RX Tone Detect output via external integration components C10, R2, R3, and D1 (see Figure 2).
10	12	RX TONE DETECT	output	In RX, this pin outputs a logical "1" when a valid programmed CTCSS tone is received at the RX TONE INPUT. This input should be externally connected to the Decode Comparator input via external integration components C10, R2, R3, and D1 (see Figure 2).
N/A	13	NOTONE	output	This pin outputs a logic "0" when a Notone CTCSS code has been programmed in RX. It is typically used to enable carrier squelch circuits under Notone RX conditions.
11	14	V_{SS}	power	The negative supply pin (ground).
12	15	TX TONE OUTPUT	output	The buffered CTCSS sinewave tone output appears on this pin. In TX mode, the tone frequency is selected by program code (see Table 4); if NOTONE is programmed, the output is at Vbias-0.7V. In RX mode, the output goes open circuit. This is an emitter follower output with an internal 10 kΩ load.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Pin No.		Name	Type	Description
LH	J,P,LH8			
13	16	V_{BIAS}		This pin is set internally to $V_{DD}/2$. It must be externally decoupled using a capacitor (C7) to V_{SS}. See Figure 2.
14	17	FILTER OUTPUT	output	This is the output of the Input Audio Bandpass Filter. It must be A.C. coupled to the Balanced Modulator Input via capacitor C4. See Figure 2.
15	18	BALANCED MODULATOR INPUT	input	This is the input to the balanced modulator. Must be A.C. coupled to the Filter Output via capacitor C4. See Figure 2.
16	19	RX AUDIO OUTPUT	output	Outputs the received audio from a buffered output stage and is held at V_{BIAS} when in TX.
17	20	TX AUDIO OUTPUT	output	Outputs the transmitted audio in TX. In RX, this pin is held at V_{BIAS}.
18	21	RX AUDIO INPUT	input	The audio input for the RX mode. Input signals should be AC coupled via external capacitor C6. See Figure 2
19	22	TX AUDIO INPUT	input	This is the TX Audio voice input. Signals should be AC coupled via external capacitor C11. See Figure 2
20	23	$\overline{PTL}$	input	The "press to listen" function input. In RX mode, a logic "0" enables the RX Audio Output directly, overriding tone squelch but not intercepting a private conversation; in TX mode, a logic "0" reverses the phase of the TX Tone Output for "squelch tail" reduction (see Table 5).
21	24	CONTROL		This input, together with Load/$\overline{Latch}$, selects the operational mode of the RX/$\overline{TX}$ and $\overline{PrivateEnable}$ functions. See Table 5
22	25	RX/$\overline{TX}$	input	This input selects the RX or TX mode (RX = 1, TX = 0). This can be loaded in Serial or Parallel modes as described in Table 5
23	26	$\overline{PRIVATE}$ $\overline{ENABLE}$		This input selects either Private or Clear mode (Clear = 1, Private = 0), and can be loaded by Serial or Parallel modes as described in Table 5. This input has an internal 1 MΩ pullup resistor.
24	27	RX TONE INPUT	input	This is the received audio input to the on-chip CTCSS tone decoder. It should be A.C. coupled via capacitor C5.

Note: The MX375LH package is available in serial mode only.

Table 1: Signal List

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components

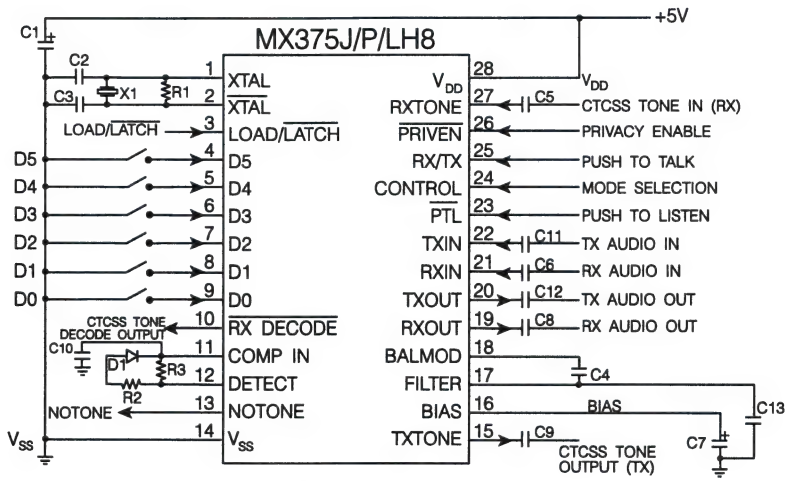


Figure 2: Recommended External Components

R1		1MΩ	±10%
R2		560kΩ	±10%
R3		820kΩ	±10%
X1	Note 1, 2	4MHz	
C1		1.0µF	±20%
C2		33pF	±20%
C3		33pF	±20%
C4		0.1µF	±20%
C5		0.1µF	±20%

C6		0.1µF	±20%
C7		1.0µF	±20%
C8		0.1µF	±20%
C9		0.1µF	±20%
C10		0.1µF	±20%
C11		0.1µF	±20%
C12		0.1µF	±20%
C13		0.001µF	±20%
D1		small signal	

Table 2: Recommended External Components

Recommended External Components Note:

1. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. XTAL - At cut, fundamental, parallel resonant 20pF load capacitance, 0.05% tolerance

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4. General Description

4.1.1 Pre- and De-emphasis

Pre- and De-emphasis (6dB/octave) filters are included on-chip in the transmit path, so that the use of this device will produce natural sounding audio (clear or private modes) when installed in modern radio communication transceivers, with or without existing audio processing circuitry. The recommended layout is shown in block form below.

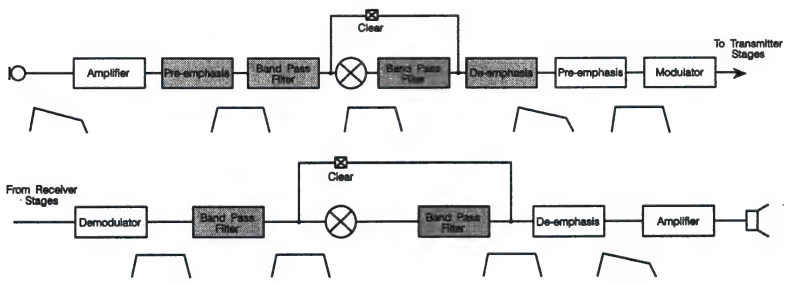


Figure 3: Transmit and Receive Paths

4.1.2 Functions and Outputs

D0-D5	Notone	RX/TX	PRIVATE ENABLE	PTL	RX TONE DETECT	RX TONE DECODER	TONE OUTPUT	TONE PHASE	TX PATH	RX PATH	PATH STATE	TONE
Tone	1	0	0	1	0	1	YES	0°	OPEN	BIAS	INV	TX, TONE
Tone	1	0	0	0	0	1	YES	180°	OPEN	BIAS	INV	TX, TONE REV
Notone	0	0	0	X	0	1	BIAS	X	OPEN	BIAS	CLR	TX, NOTONE
Tone	1	1	0	1	0	1	BIAS	X	BIAS	BIAS	X	INCOMPATIBLE
Tone	1	1	0	0	0	1	BIAS	X	BIAS	OPEN	CLR	INCOMPATIBLE
Tone	1	1	0	X	1	0	BIAS	X	BIAS	OPEN	INV	COMPATIBLE
Notone	0	1	0	X	X	0	BIAS	X	BIAS	OPEN	CLR	RX, NOTONE
Tone	1	0	1	1	0	1	YES	0°	OPEN	BIAS	CLR	TX, TONE
Tone	1	0	1	0	0	1	YES	180°	OPEN	BIAS	CLR	TX, TONE REV
Notone	0	0	1	X	0	1	BIAS	X	OPEN	BIAS	CLR	TX, NOTONE
Tone	1	1	1	1	0	1	BIAS	X	BIAS	BIAS	X	INCOMPATIBLE
Tone	1	1	1	0	0	1	BIAS	X	BIAS	OPEN	CLR	INCOMPATIBLE
Tone	1	1	1	X	1	0	BIAS	X	BIAS	OPEN	CLR	COMPATIBLE
Notone	0	1	1	X	X	0	BIAS	X	BIAS	OPEN	CLR	RX, NOTONE

Table 3: Functions and Outputs

Note:

1. Algebraic functions:
   RX Path On = RX × (PTL + RX Tone Decoder)
   Clear Path = Notone + Private Enable + (PTL × RX × RX Tone Decoder)
   Notone (D0 - D5) = 000011
   Carrier Frequency = 3333Hz During inverted Path (TX or RX)
2. The Pre- and De-emphasis circuits remain in the transmit path in both the Clear and Invert Modes.
3. Power remains applied to the CTCSS tone decoder at all times.
4. During clear operation the carrier frequency is turned off to reduce spurious emissions.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. Application

5.1.1 CTCSS Programming

Nominal Frequency(Hz)	Frequency(Hz)	Δ F_0 (%)	Program Inputs					
			D5	D4	D3	D2	D1	D0
67.0	67.05	+0.07	1	1	1	1	1	1
71.9	71.9	0	0	1	1	1	1	1
74.4	74.35	-0.07	1	1	1	1	1	0
77.0	76.96	-0.5	0	0	1	1	1	1
79.7	79.77	+0.09	1	1	1	1	0	1
82.5	82.59	+0.1	0	1	1	1	1	0
85.4	85.38	-0.2	1	1	1	1	0	0
88.5	88.61	+0.13	0	0	1	1	1	0
91.5	91.58	+0.09	1	1	1	0	1	1
94.8	94.76	-0.04	0	1	1	1	0	1
97.4	97.29	-0.11	1	1	1	0	1	0
100.0	99.96	-0.04	0	0	1	1	0	1
103.5	103.43	-0.07	0	1	1	1	0	0
107.2	107.15	-0.05	0	0	1	1	0	0
110.9	110.77	-0.12	0	1	1	0	1	1
114.8	114.64	-0.14	0	0	1	0	1	1
118.8	118.8	0	0	1	1	0	1	0
123.0	122.8	-0.17	0	0	1	0	1	0
127.3	127.08	-0.17	0	1	1	0	0	1
131.8	131.67	-0.10	0	0	1	0	0	1
136.5	136.61	+0.08	0	1	1	0	0	0
141.3	141.32	+0.02	0	0	1	0	0	0
146.2	146.37	+0.12	0	1	0	1	1	1
151.4	151.09	-0.2	0	0	0	1	1	1
156.7	156.88	+0.11	0	1	0	1	1	0
162.2	162.31	+0.07	0	0	0	1	1	0
167.9	168.14	+0.14	0	1	0	1	0	1
173.8	173.48	-0.19	0	0	0	1	0	1
179.9	180.15	+0.14	0	1	0	1	0	0
186.2	186.29	+0.05	0	0	0	1	0	0
192.8	192.86	+0.03	0	1	0	0	1	1
203.5	203.65	+0.07	0	0	0	0	1	1
210.7	210.17	-0.25	0	1	0	0	1	0
218.1	218.58	+0.22	0	0	0	0	1	0
225.7	226.12	+0.18	0	1	0	0	0	1
233.6	234.19	+0.25	0	0	0	0	0	1
241.8	241.08	-0.30	0	1	0	0	0	0
250.3	250.28	-0.01	0	0	0	0	0	0
Notone			1	1	0	0	0	0

Table 4: CTCSS Programming

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

(A) Explanation of Load/Latch function in Serial and Parallel Modes			
Load Configuration	**Load/$\overline{\text{Latch}}$**	**Result**	
Parallel	1	Transparent, the data acts directly	
Parallel	1 - 0	Latches present data in	
Parallel	0	No further changes except to allow serial mode selection	
Serial (data loading)	0	No change while serial data train is loaded	
Serial (data loaded)	0 - 1 - 0	Loaded serial data is latched	
(B) Explanation of Control Input			
Load Configuration	**Load/$\overline{\text{Latch}}$**	**Control**	**RX/$\overline{\text{TX}}$,$\overline{\text{Private Enable}}$**
Parallel	0	0	Latched
Parallel	1	0	Transparent
Parallel	X	1	Transparent
Serial	0 - 1 - 0	0	Serial Load
Serial	X	1	Transparent

Table 5: Load/$\overline{\text{Latch}}$ and Control Input Function

Notes:

1. "0 - 1 - 0" is a strobe pulse as shown in Figure 4 and Figure 5.
2. "X" denotes any logical state.

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	**Min.**	**Typ.**	**Max.**	**Units**
Supply Voltage	-0.3		7.0	V
Input Voltage at any pin	-0.3		(V_{DD} + 0.3)	V
Current				
V_{DD}	-30		30	mA
V_{SS}	-30		30	mA
Any other pin	-20		20	mA
J / P / LH / LH8 Packages				
Total Device Dissipation at T_{AMB} 25°C			800	mW
Derating above 25°C			10	mW/°C above 25°C
Operating Temperature	-40°		85°	C
Storage Temperature	-55°		125°	C

Table 6: Absolute Maximum Ratings

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal/Clock Frequency			4.0		MHz

Table 7: Operating Limits

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C, XTAL = 4.0MHz, Audio level)dB ref. = 300mV_{RMS}, Composite input signal = 0dB, 1 kHz tone in, -12dB (6kHz band limited) Gaussian white noise with a -20dB CTCSS tone.

	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
TX (Private)				15.0	mA
TX (Operating)				12.0	mA
RX (Operating)				7.0	mA
Analog Input Impedance			0.5		MΩ
Analog Output Impedance			0.5		kΩ
Tone Input Impedance			0.5		MΩ
Input Logic "1"		3.5			V
Input Logic "0"				1.5	V
Output Logic "1" (I=-0.1mA)		4.0			V
Output Logic "0" (I=-0.1mA)				1.0	V
Dynamic Values					
Decoder					
Input Signal Level	1,4	-20			dB
Response Time	1,4,6			250	ms
Deresponse Time	1,4,6			250	ms
Selectivity	4	±0.5		±3.0	%f_0
Encoder					
Tone Output Level (775mV_{RMS} ref.)		-3.0	0	3.0	dB
Tone Frequency Accuracy		-0.3		0.3	%f_0
Tone Harmonic Distortion			2.0	5.0	%
Tone Output Load Current	2			5.0	mA
Output Level Variation between Tones	9	-1.0		1.0	dB
Risetime (to 90% nominal level)					
(f_0>100 Hz)	5		15		ms
(f_0<100 Hz)	5		45		ms

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

	Notes	Min.	Typ.	Max	Units
RX Clear					
Total Harmonic Distortion	3		2	5	%
Output Noise Level	7		-43		dB
Passband Gain (300-3033Hz)	3	-1	0	1	dB
Passband Ripple (300-3033Hz)	3			3	dB
Audio Stopband Attenuation					
(f_{IN}>3333Hz)	8		-20		dB
(f_{IN}>3633Hz)	8		-45		dB
(f_{IN}<250Hz)			-42		dB
RX Invert					
Total Harmonic Distortion	3,8		4	10	%
Baseband Breakthrough	3		-40		dB
Carrier Breakthrough			-40		dB
Output Noise Level	7,8		-37		dB
Passband Ripple (300-3000Hz)	3		-	4	dB
Audio Stopband Attenuation					
(f_{IN}>3333Hz)	8		-50		dB
(f_{IN}>3633Hz)	8		-60		dB
(f_{IN}<250Hz)			-60		dB
TX Clear					
Total Harmonic Distortion	3		3	5	%
Output Noise Level	7		-43		dB
Passband Gain (300-3033Hz)	3		0		dB
Passband Ripple (300-3033Hz)	3			3	dB
Audio Stopband Attenuation					
(f_{IN}>3333Hz)	8		-20		dB
(f_{IN}>3633Hz)	8		-45		dB
(f_{IN}<250Hz)			-42		dB
TX Invert					
Total Harmonic Distortion	3,8		4	10	%
Baseband Breakthrough			-40		dB
Carrier Breakthrough			-40		dB
Output Noise Level	7,8		-37		dB
Passband Ripple (300-3033Hz)	3,8			4	dB
Audio Stopband Attenuation					
(f_{IN}>3333Hz)	8		-50		dB
(f_{IN}>3633Hz)	8		-60		dB
(f_{IN}<250Hz)	8		-60		dB

Table 8: Operating Characteristics

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Operating Characteristics Notes:

1. These values are obtained using the external integrating components given in Figure 2.
2. An emitter follower output
3. With an input signal of 1 kHz @ 0dB.
4. Under Composite Signal test conditions.
5. Any programmed tone with R_L=600 Ω, C_L=15pF, including any response to a phase reversal instruction.
6. f_0 > 100 Hz, (for 100Hz > f_0 > 67Hz: t = [100/f_0(Hz)] x 250ms).
7. Input ac short-circuit, audio path enabled.
8. Due to frequency inversion, these figures reflect the difference from the ideal response.
9. Reference 156.7 Hz (MX175 and MX275).

6.2 Timing Information

6.2.1 Serial Loading

	Min.	Typ.	Max.	Unit
Serial Mode Enable Set Up Time (t_{SMS})	250	-	-	ns
Clock "High" Pulse Width (t_{PWH})	250	-	-	ns
Clock "Low" Pulse Width (t_{PWL})	250	-	-	ns
Data Set Up Time (t_{DS})	150	-	-	ns
Data Hold Time (t_{DH})	50	-	-	ns
Load/Latch Set Up Time (t_{LL})	250	-	-	ns
Load/Latch Pulse Width (t_{LLW})	150	-	-	ns

Table 9: Serial Loading Timing Information

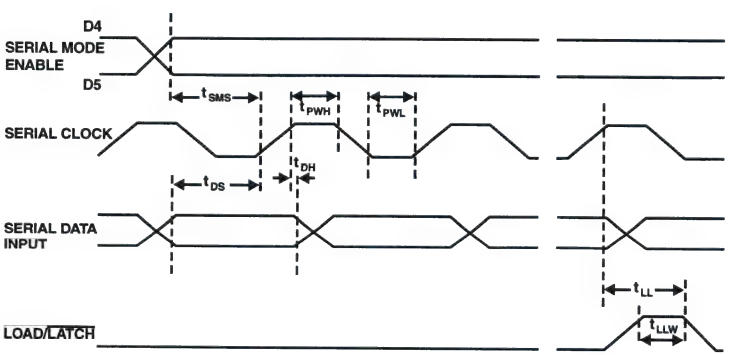


Figure 4: Serial Loading Timing

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.2.2 Parallel Loading

	Min.	Typ.	Max.	Unit
Data Valid Time (t_{VP})	200			ns
Load Time (t_L)	150			ns
Fall Time (t_F)			50	ns
Data Hold Time (t_H)	50			ns

Table 10: Parallel Loading Timing Information

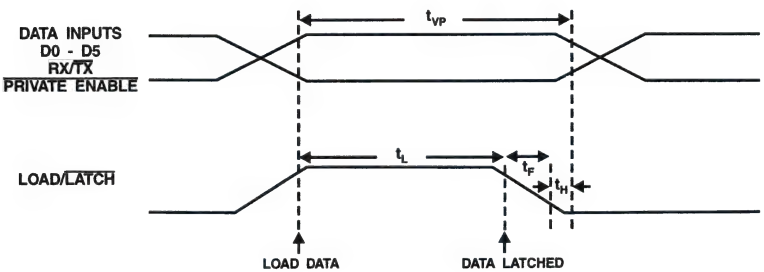
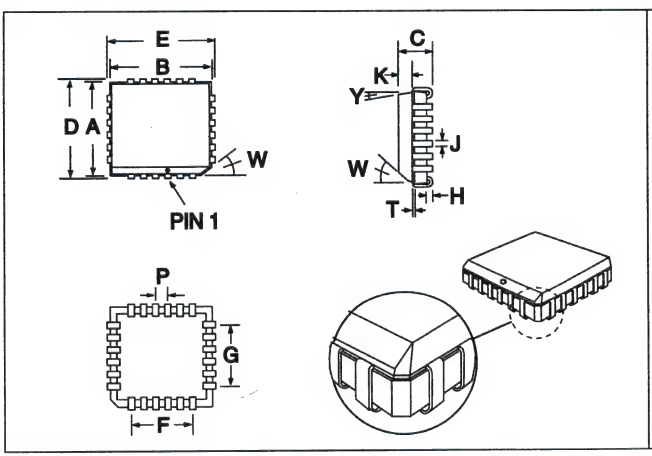


Figure 5: Parallel Load Timing

6.3 Packaging



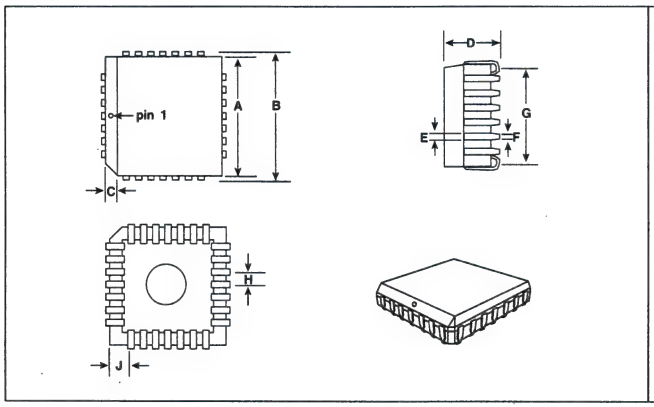
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin PLCC Mechanical Outline: *Order as part no. MX375LH*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

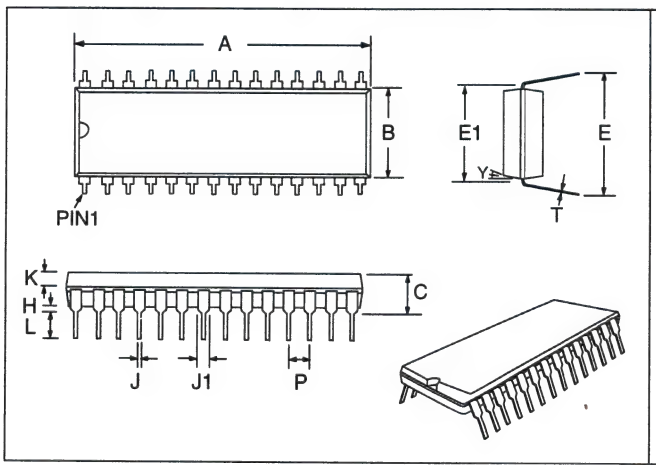


Package Tolerances

DIM.	MIN.	MAX.
A	.450 (11.43)	.453 (11.51)
B	.485 (12.32)	.495 (12.57)
C	.045x45	typical
D	.165 (4.20)	.180 (4.57)
E	.026 (0.66)	.030 (0.76)
F	.017 (0.43)	.021 (0.53)
G	.410 (10.41)	.430 (10.92)
H	.050 (1.27)	typical
J	.070 (1.78)	.085 (2.16)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 28-pin PLCC Mechanical Outline: *Order as part no. MX375LH8*



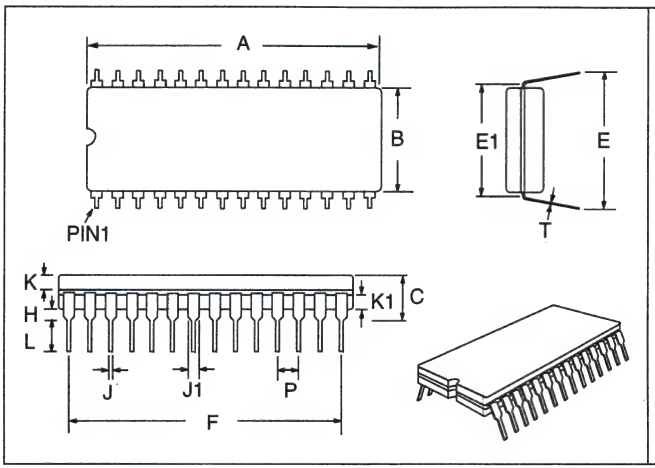
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.440 (36.44)		1.47 (37.20)
B	0.530 (13.41)		0.555 (14.04)
C	0.160 (4.05)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.013 (0.33)		0.021 (0.53)
J1		0.060 (1.52)	
K	0.066 (1.67)		0.074 (1.88)
L	0.125 (3.16)		0.160 (4.05)
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 28-pin PDIP Mechanical Outline: *Order as part no. MX375P*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.440 (36.58)		1.460 (37.08)
B	0.510 (12.94)		0.530 (13.45)
C	0.165 (4.19)		0.230 (5.84)
E	0.640 (16.26)		0.715 (18.14)
E1	0.608 (15.43)		0.618 (15.70)
F		1.300 (33.02)	
H	0.015 (0.38)		0.050 (1.27)
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0090 (0.228)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 28-pin CDIP Mechanical Outline: ***Order as part no. MX375J***

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480026.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX465

Low Voltage CTCSS Encoder/Decoder
with TX/RX Audio Filters

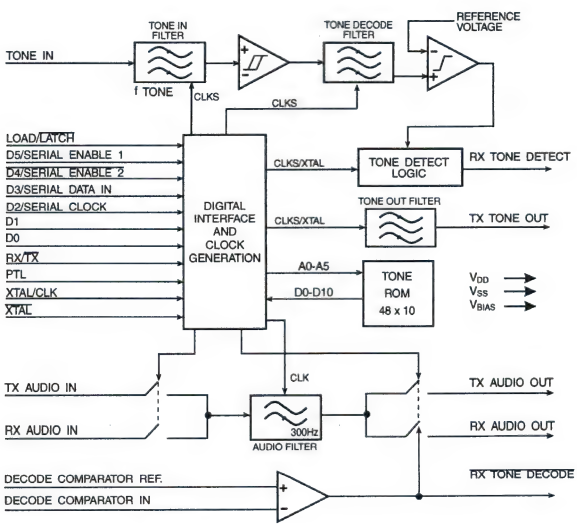
PRELIMINARY INFORMATION

Features

- **Meets TIA/EIA-603 Standards**
- **47 CTCSS Tones + Notone**
- **TX/RX Speech Filters**
- **Improved Sinad**
- **Serial or Parallel Programming**
- **Easy µP Interface**
- **Scanning on any Channel**
- **Standard 4MHz Xtal (See MX165C for 1MHz)**
- **Low Voltage 3.3V to 5.0V**

Applications

- **Mobile Radio Channel Sharing**
- **Scan Trunking**
- **Wireless Intercom Traffic Control**
- **Hookswitch Supervision**
- **Repeater Control**



The MX465 CTCSS Encoder/Decoder is a low voltage, CMOS device that meets TIA/EIA-603 Standards. The MX465 will encode and decode the tones 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz in addition to the 39 standard CTCSS tones, for a total of 47 CTCSS tones + Notone. With the incorporation of the on-chip TX and RX speech filter, the MX465 enhances voice/tone multiplexing by attenuating TX and RX speech 36dB at frequencies below 250Hz while passing signals > 300Hz with only 1dB of ripple. This not only minimizes CTCSS talk-off in the TX mode but also improves Hum and Noise performance in the RX mode.

Available in the following package styles: 24-pin TSSOP (MX465TN), 24-pin SSOP (MX465DS), 24-pin SOIC (MX465DW), 24-pin PLCC (MX465LH), 24-pin PDIP (MX465P), and 24-pin CDIP (MX465J) the MX465 requires a single 3.3V to 5.0V supply and a 4MHz clock or crystal.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. #20480143.006

CONTENTS

Section **Page**

1. Block Diagram **3-47**

2. Signal List **3-48**

3. External Components **3-50**

4. General Description **3-51**

4.1 Description 3-51
4.2 I/O Conditions 3-51
4.3 Filter Response 3-52
4.4 Serial and Parallel Mode Timing 3-52
4.5 CTCSS Programming 3-54

5. Performance Specification **3-55**

5.1 Electrical Performance 3-55
5.1.1 Absolute Maximum Ratings 3-55
5.1.2 Operating Limits 3-55
5.2 Packaging 3-58

MX•COM, Inc. Reserves the right to change specifications at any time and without notice

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. #20480143.006

Block Diagram

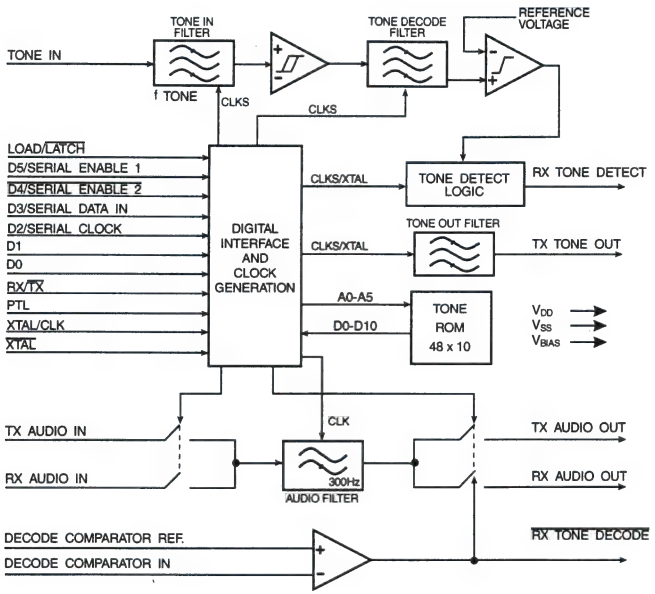


Figure 1 : Block Diagram

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Signal List

Pin No.	Signal	Type	Description
1	V_{DD}	power	Positive supply. This pin should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
2	XTAL/CLOCK	input	Input to the on-chip inverter used with a 4 MHz Xtal or external clock source.
3	$\overline{XTAL}$	output	Output of the on-chip inverter (clock output).
4	LOAD/$\overline{LATCH}$	input	Controls 8 on-chip latches. It is used to latch RX / $\overline{TX}$, PTL, and D0-D5. A logic 1 applied to this input places the 8 latches in the 'transparent' mode. A logic 0 applied to this input places the 8 latches in the 'latched' mode. In Parallel Mode, data is loaded and latched by a logic 1-0 transition (see Figure 4). In Serial Mode, data is loaded and latched by a 0-1-0 strobe pulse on this pin (see Figure 5). Internally pulled to V_{DD}
5	D5 / SERIAL ENABLE 1	input	Data input D5 (Parallel Mode). A logic 1 applied to this input together with a logic 0 applied to D4/$\overline{SERIAL\ ENABLE\ 2}$ will place the device in Serial Mode (see Figure 5). Internally pulled to V_{DD}.
6	D4 / $\overline{SERIAL\ ENABLE\ 2}$	input	Data input D4 (Parallel Mode). A logic 0 applied to this input together with a logic 1 applied to D5 / SERIAL ENABLE 1 will place the device in Serial Mode (see Figure 5). Internally pulled to V_{DD}.
7	D3 / SERIAL DATA IN	input	Data input D3 (Parallel Mode). In Serial Mode this pin becomes the serial data input for D5-D0, RX / $\overline{TX}$ and PTL (see Figure 5). D5 is clocked first and PTL last. Internally pulled to V_{DD}.
8	D2 / SERIAL CLOCK	input	Data input D2 (Parallel Mode). In Serial Mode this pin becomes the SERIAL CLOCK input. Data is clocked on the positive going edge (see Figure 5). Internally pulled to V_{DD}.
9	D1	input	Data input D1 (Parallel Mode). Internally pulled to V_{DD}.
10	D0	input	Data input D0 (Parallel Mode). Internally pulled to V_{DD}.
11	V_{SS}	power	Negative supply.
12	DECODE COMPARATOR REF.	input	Internally biased to $V_{DD}/3$ or 2 $V_{DD}/3$ via 1M resistors depending on the logic state of the $\overline{RX\ TONE\ DECODE}$ pin. $\overline{RX\ TONE\ DECODE}$ = 1 will bias this input 2 $V_{DD}/3$; a logic 0 will bias this input $V_{DD}/3$. This input provides the DECODE COMPARATOR REFERENCE voltage, and the switching of bias voltages provides hysteresis to reduce 'chatter' under marginal conditions.
13	$\overline{RX\ TONE\ DECODE}$	output	Gated output of the decode comparator. This output is used to gate the RX Audio path. A logic 0 on this pin indicates a successful decode and the DECODE COMPARATOR IN pin is more positive than the DECODE COMPARATOR REF. input (see Table 3).
14	DECODE COMPARATOR IN	input	Inverting input of the DECODE COMPARATOR. This pin is normally connected to the integrated output of the RX TONE DETECT line.
15	RX TONE DETECT	output	In RX mode this output will go to logic 1 during a successful decode. It must be externally integrated to control response and deresponse times (see Table 3).
16	TX TONE OUT	output	The CTCSS sinewave output appears on this pin under control of the RX / $\overline{TX}$ pin. When not transmitting a tone, TX TONE OUT may be biased to $V_{DD}/2$. (see Table 3).
17	RX / $\overline{TX}$	input	RX or TX modes selected in Parallel Mode (see Figure 4). In Serial Mode this function is serially loaded. This pin is internally pulled to V_{DD} via a 1MΩ resistor.
18	PTL	input	In RX mode this pin operates as a 'Push To Listen' function by enabling the RX audio path, thus overriding the tone squelch function (Parallel Mode). In Serial Mode this function is loaded serially. Internal pull-up to V_{DD}

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Pin No.	Signal	Type	Description
19	RX AUDIO OUT	output	High pass filtered RX AUDIO OUT. This pin outputs audio when RX TONE DECODE = logic 0, PTL = logic 1, or when Notone is programmed (see Table 4). In TX mode this pin is biased to $V_{DD}/2$.
20	TX AUDIO OUT	output	High pass filtered TX AUDIO OUT pin. In TX mode this pin outputs audio present at the TX AUDIO IN pin. In RX mode this pin is biased to $V_{DD}/2$
21	V_{BIAS}	output	Output of an internally generated V_{DD} /2 bias level that would normally be externally bypassed to V_{SS} via capacitor C6.
22	TX AUDIO IN	input	In TX mode TX AUDIO IN may be prefiltered, using the TX Audio path, thus helping to avoid talk-off due to intermodulation of speech frequencies with the transmitted CTCSS tone. Internally biased to $V_{DD}/2$.
23	RX AUDIO IN	input	Input to the audio high pass filter in RX mode. Internally biased to $V_{DD}/2$.
24	TONE INPUT	input	Input to the CTCSS tone detector. Internally biased to $V_{DD}/2$.

Table 1: Signal List

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. #20480143.006

External Components

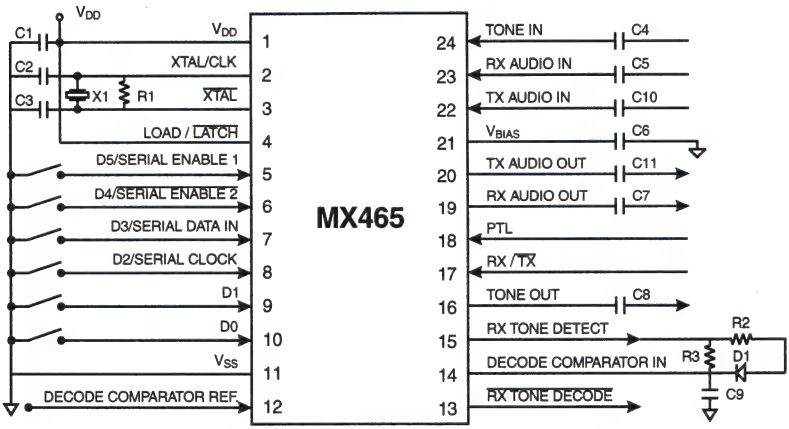


Figure 2 : Recommended External Components for Typical Application

R1	Note 1	1.0MΩ	±10%
R2		560kΩ	±10%
R3		820kΩ	±10%
C1		0.1µF	±20%
C2	Note 1	18pF	±20%
C3	Note 1	33pF	±20%
C4	Note 2	0.1µF	±20%
C5	Note 2	0.1µF	±20%

C6		0.47µF	±20%
C7	Note 2	0.1µF	±20%
C8	Note 2	0.1µF	±20%
C9	Note 2	0.1µF	±20%
C10	Note 2	0.1µF	±20%
C11	Note 2	0.1µF	±20%
D1		small signal	
X1	Note 1	4MHz	100ppm max.

Table 2: External Components

External Components Notes:

1. The values specified for R1, C2, and C3 have been found to be satisfactory when used with a crystal (X1) whose equivalent series resistance is ≤ 1000Ω. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. The 0.1µF value for the DC Blocking capacitors, C4, C5, C7, C8, C9, C10, and C11 is not a requirement. For the capacitors C4, C5, and C10, the input impedance is internal to the device and specified typical as 550kΩ. For the remaining capacitors external circuits will be important in determining the input impedance.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

General Description

Description

Voice on shared radio channels are multiplexed with a subaudible CTCSS (Continuous Tone Controlled Subaudible Squelch) tone as a means of directing messages among user groups sharing the same RF frequencies. CTCSS modulates the transmitter with a discrete tone, from 39 standard CTCSS tones in the range (67.0Hz to 250.0Hz) according to TIA/EIA-603. There are an additional eight CTCSS tones not specified in TIA/EIA-603 that the MX465 will encode and decode. They are : 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz, for a total of 47 CTCSS tones plus Notone.

The MX465 also incorporates TX/RX on chip speech filters. In early CTCSS designs, TX speech was not filtered from the CTCSS tone, rather the filtering was dependent upon the host transmitter's pre-emphasis network. At only 6dB/octave, the attenuation of speech components at higher CTCSS tones was only a few dB which resulted in talk-off (low frequency voice components unsquelching the receiver audio).

I/O Conditions

D0-D5	Tone	No Tone	Tone	Tone	Tone	No Tone
Input Pins Condition						
RX / $\overline{TX}$	0	0	1	1	1	1
PTL	0	X	0	1	X	X
Decode Comparator In	X	X	0	0	1	X
Output Pins Condition						
RX TONE DETECT	0	0	0	0	1	X
$\overline{\text{RX TONE DECODE}}$	1	1	1	1	0	0
Result / Function						
Tone Transmitter Enabled	Yes	No (Bias)	No (Bias)	No (Bias)	No (Bias)	No (Bias)
TX Audio Path Enabled	Yes	Yes	No	No	No	No
Tone Decode Enabled	No	No	Yes	Yes	Yes	Yes
RX Audio Path Enabled	No (Bias)	No (Bias)	No (Bias)	Yes	Yes	Yes
Notes	1	2	3	4	5	6

Notes:

1. Normal tone transmit condition.
2. Notone programmed in TX mode, tone transmit output set to $V_{DD}/2$. TX audio path enabled.
3. Normal decode standby.
4. Normal decode standby with PTL used to enable audio.
5. Normal decode of correct CTCSS tone condition, PTL has no effect.
6. Notone programmed in RX mode, tone transmit output (Bias). RX audio path enabled.
7. X = don't care

Table 3: Combinations of Input / Output conditions

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Filter Response

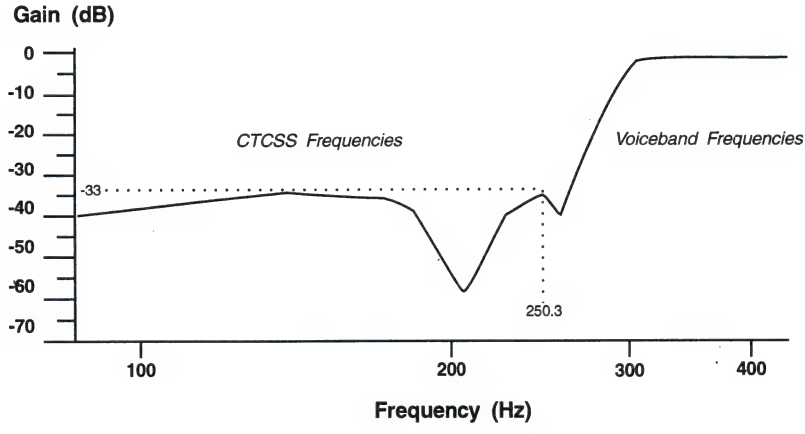


Figure 3 : Voiceband Filter Response

Serial and Parallel Mode Timing

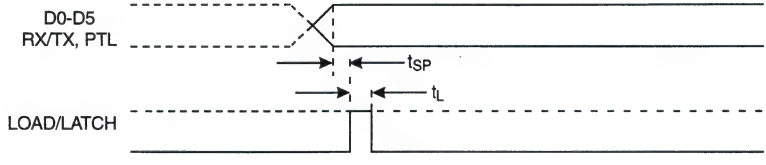
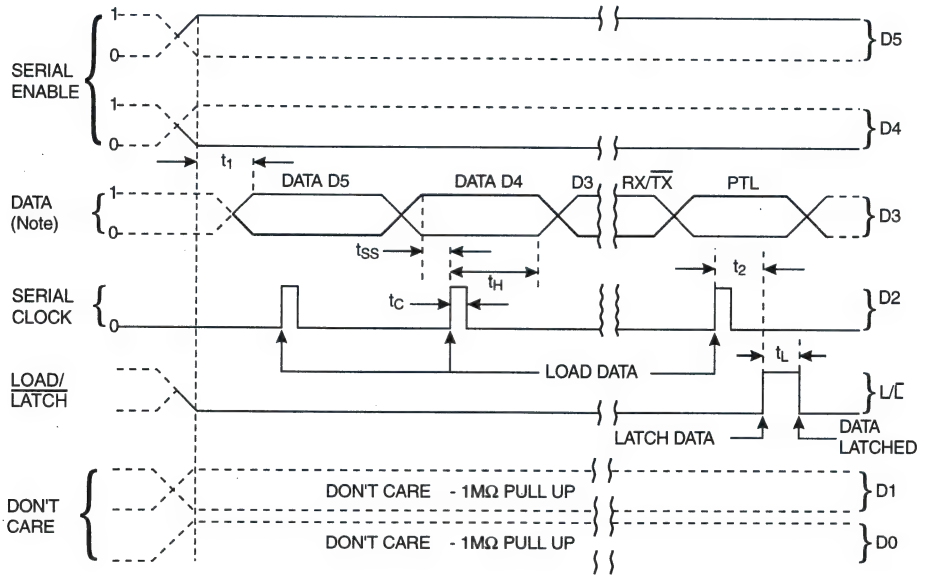


Figure 4 : Parallel Mode

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054



Note : Serial bit 1 through bit 8 = D5, D4, D3, D2, D1, D0, RX/TX and PTL respectively. Load bit 1 first, bit 8 last

Figure 5 : Serial Mode

CTCSS Programming

	Tone			Programming Inputs						
	Nominal Frequency (Hz)	MX465 Frequency (Hz)	Δf_0 (%)	D5	D4	D3	D2	D1	D0	Hex
	67.0	66.98	-0.029	1	1	1	1	1	1	3F
	69.3	69.32	0.024	1	1	1	0	0	1	39
	71.9	71.901	0.001	0	1	1	1	1	1	1F
	74.4	74.431	0.042	1	1	1	1	1	0	3E
	77.0	76.965	-0.046	0	0	1	1	1	1	0F
	79.7	79.677	-0.029	1	1	1	1	0	1	3D
	82.5	82.483	-0.021	0	1	1	1	1	0	1E
	85.4	85.383	-0.020	1	1	1	1	0	0	3C
	88.5	88.494	-0.007	0	0	1	1	1	0	0E
	91.5	91.456	-0.048	1	1	1	0	1	1	3B
	94.8	94.76	-0.042	0	1	1	1	0	1	1D
	97.4	97.435	-0.036	1	1	1	0	1	0	3A
	100.0	99.96	-0.040	0	0	1	1	0	1	0D
	103.5	103.429	-0.069	0	1	1	1	0	0	1C
	107.2	107.147	-0.05	0	0	1	1	0	0	0C
	110.9	110.954	0.049	0	1	1	0	1	1	1B
	114.8	114.84	0.035	0	0	1	0	1	1	0B
	118.8	118.793	-0.006	0	1	1	0	1	0	1A
	123.0	123.028	0.023	0	0	1	0	1	0	0A
	127.3	127.328	0.022	0	1	1	0	0	1	19
	131.8	131.674	-0.095	0	0	1	0	0	1	09
	136.5	136.612	0.082	0	1	1	0	0	0	18
	141.3	141.323	0.016	0	0	1	0	0	0	08
	146.2	146.044	-0.107	0	1	0	1	1	1	17
	151.4	151.441	0.027	0	0	0	1	1	1	07
	156.7	156.875	0.112	0	1	0	1	1	0	16
•	159.8	159.936	0.085	1	1	0	0	0	1	31
	162.2	162.311	0.069	0	0	0	1	1	0	06
	167.9	167.708	-0.114	0	1	0	1	0	1	15
	173.8	173.936	0.078	0	0	0	1	0	1	05
	179.9	179.654	-0.137	0	1	0	1	0	0	14
•	183.5	183.680	0.098	1	1	0	0	1	0	32
	186.2	186.289	0.048	0	0	0	1	0	0	04
•	189.9	190.069	0.089	1	1	0	0	1	1	33
	192.8	192.864	0.033	0	1	0	0	1	1	13
•	196.6	196.329	-0.138	1	1	0	1	0	0	34
•	199.5	199.312	-0.094	1	1	0	1	0	1	35
	203.5	203.645	0.071	0	0	0	0	1	1	03
•	206.5	206.207	-0.142	1	1	0	1	1	0	36
	210.7	210.848	0.070	0	1	0	0	1	0	12
	218.1	217.853	-0.113	0	0	0	0	1	0	02
	225.7	225.339	-0.160	0	1	0	0	0	1	11
•	229.1	229.279	0.078	1	1	0	1	1	1	37

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

	Tone			Programming Inputs						
	Nominal Frequency (Hz)	MX465 Frequency (Hz)	Δf_0 (%)	D5	D4	D3	D2	D1	D0	Hex
	233.6	233.359	-0.103	0	0	0	0	0	1	01
	241.8	241.970	0.070	0	1	0	0	0	0	10
	250.3	250.282	-0.007	0	0	0	0	0	0	00
•	254.1	254.162	0.024	1	1	1	0	0	0	38
	Notone		N/A	1	1	0	0	0	0	30
	Serial input mode		N/A	1	0	Data	Clock	X	X	2X

• Not specified in the TIA/EIA tone set

Table 4: CTCSS Tones

Performance Specification

Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device. Operation of the device outside the operating limits is not implied.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
any other pins	-20	20	mA
TN / DW / LH / DIP Package			
Total Allowable Power Dissipation at T_{AMB} =25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating temperature	- 40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} =25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating temperature	- 40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	Max.	Units
Supply (V_{DD}-V_{SS})	2.7	5.5	V
Xtal Frequency	1.0	1.0	MHz
Operating Temperature	-40	85	°C

© 1996 MX-COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.3V / 5.0V at T_{AMB} = 25°C, V_{SS} = 0V,
Xtal Frequency = 4.0 MHz, 100ppm max.
(Over the life of the XTAL the operating range may vary from 100ppm up to 1000ppm)
0dB ref. = 750mV_{RMS} (proportional to V_{DD}; see note 17)

Composite Signal:
1kHz test tone = 300mV_{RMS}, f0 CTCSS tone = 30 mV_{RMS}, 75mV_{RMS} Noise (band limited to 6kHz Gaussian)

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply voltage		2.7	3.3/5.0	5.5	V
Supply current					
V_{DD} = 5.0V			3.7	4.2	mA
V_{DD} = 3.3V			1.3	1.6	mA
Analog input impedance	18	480	550		kΩ
Analog output impedance	18		400	1000	Ω
Digital Input impedance	1,18	25	40		kΩ
Input logic 1	1	70%V_{DD}			V
Input logic 0	1			30%V_{DD}	V
Output Logic 1 source = 0.1mA	2	80%V_{DD}			V
Output Logic 0 sink = 0.1mA	2			20%V_{DD}	V
Dynamic Values					
Speech filter					
Total harmonic distortion	5,8,19		1.0	1.5	%
Output noise level (input ac short circuit, audio switch enabled)	8,18		0.5	1.0	mV_{RMS}
Sinad	8,9	40	50		dB
Spurious emissions	18			- 48	dB
Cutoff frequency			300		Hz
Bandpass ripple	8		1	1.8	dB
Stopband attenuation <250Hz	7,8,19	33	36		dB
Passband gain 1kHz		- 0.5	0	0.5	dB
TX/RX isolation	5		60		dB
Encoder					
Tone output level	12	- 1.0	0	1.0	dB
Tone Frequency Accuracy (f error)		- 0.3		0.3	%f_0
Risetime to 90% nominal output					
f_0>100Hz	4,10		15	75	ms
f_0<100Hz	4,10		45	120	ms
Total Harmonic Distortion	19		1.5	2	%

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

	Notes	Min.	Typ.	Max.	Units
Decoder					
Pure tone decode threshold	19		7	15	mV_{RMS}
Composite signal decode threshold	3			30	mV_{RMS}
Decode input signal level	16	-20		3.5	dB
Pure tone decode response time	13,14	95	115	140	ms
Pure tone decode deresponse time	13,15	95	130	170	ms
Decode response time	3,6,10			250	ms
Deresponse time	3,10		180	250	ms
Decode selectivity:					
Upper decode band edge	3,11,19,20	$1.005f_0$	$1.015f_0$	$0.995f_{0+1}$	Hz
Lower decode band edge	3,11,19,20	$1.005f_{0-1}$	$0.985f_0$	$0.995f_0$	Hz
Serial / Parallel Inputs					
Parallel Set Up Time (t_{SP})		400			ns
Load / Latch Pulse Width (t_L)		400			ns
Serial Clock Pulse Width (t_C)		400			ns
Serial Data Set-Up Time (t_{SS})		400			ns
Serial Data Hold Time (t_H)		400			ns
Serial Enable Time (t_1)		400			ns
Serial Load / Latch Set-Up Time (t_2)		400			ns
Serial Clock Frequency			1		MHz

Operating Characteristics Notes:

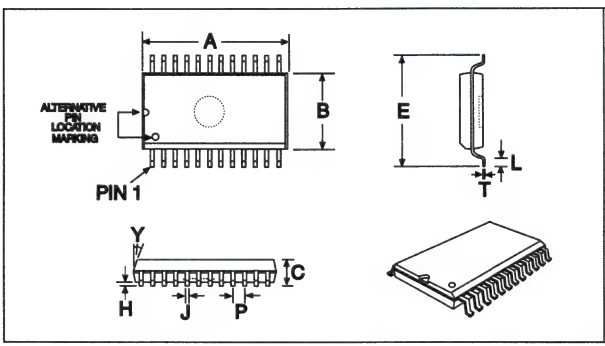
1. Refers to RX/TX, PTL, Decode Comparator Input, D0-D5.
2. All logic outputs.
3. Composite signal test condition.
4. Any programming tone and R_L = 10kΩ, C_L = 15pF.
5. With an input level of 0dB @1kHz
6. f_0>100Hz (for 100 Hz> f_0>67Hz: t=100/ f_0Hz x 250ms)
7. See Figure 3.
8. Measured in a 30kHz bandwidth.
9. With an input level of -3.5dB @1kHz
10. Per TIA/EIA-603.
11. Per TIA/EIA-603, device will not decode adjacent TIA/EIA-603 Tones.
12. Tone output level is proportional to V_{DD}.
13. f_0=156.7Hz @ -20dB.
14. Typically 12.5 Tone Cycles + 40ms.
15. Typically 7 Tone Cycles + 90ms.
16. Max composite signal is 3.5dB with:
    Noise (band limited 6kHz Gaussian) = -12dB ref to 1kHz test tone
    f_0 CTCSS tone = -20dB ref to 1kHz test tone
17. For maximum dynamic range, set audio level to 0dB, V_{DD} x150mV_{RMS}, using minimum V_{DD} under which system is intended to work. (e.g. for a 2.7V system, use 0dB equal to 405mV_{RMS}).
18. By characterization only.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

19. Batch sampled only
20. For example, if: $f_0 = 100.0Hz$ ($f_{0-1} = 97.4Hz$ $f_{0+1} = 103.5Hz$)

Decode Selectivity	Min	Typ	Max	Unit
Upper Decode Band Edge	100.5	101.5	102.98	Hz
Lower Decode Band Edge	97.89	98.5	99.5	Hz

Packaging

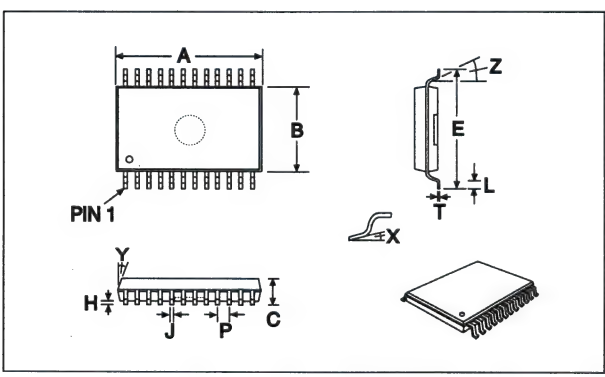


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	---------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin TSSOP Mechanical Outline: Order as part no. MX465TN



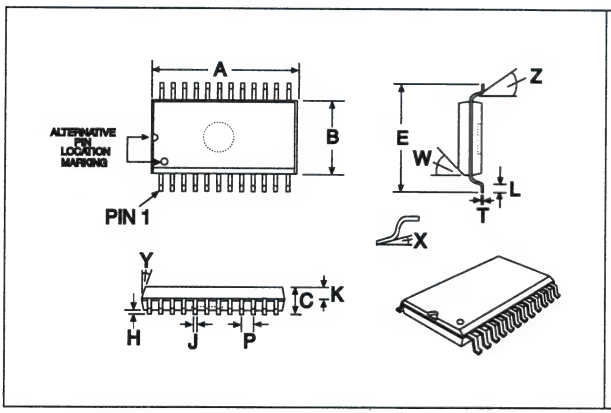
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 24-pin-SSOP Mechanical Outline: *Order as part no. MX465DS*

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

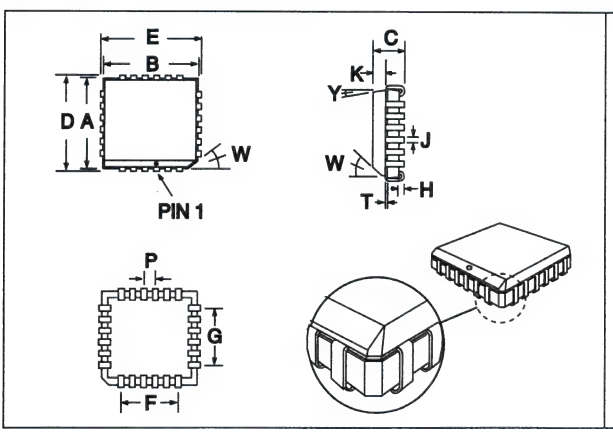


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin SOIC Mechanical Outline: *Order as part no. MX465DW*



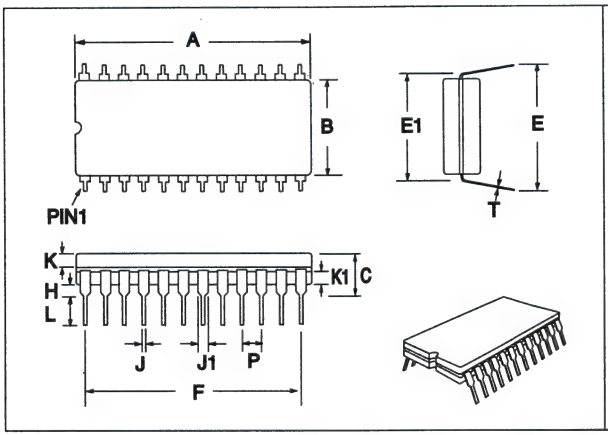
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 24-pin PLCC Mechanical Outline: *Order as part no. MX465LH*

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

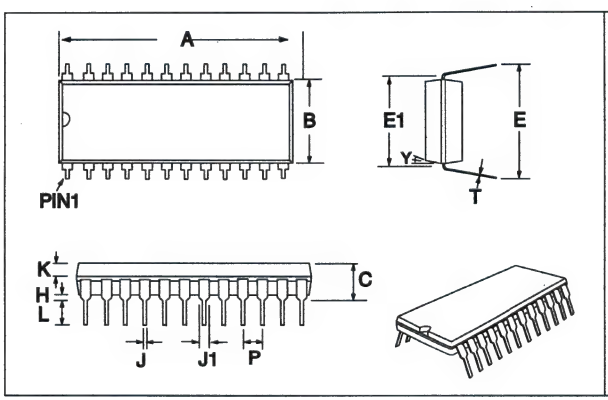


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin-CDIP Mechanical Outline: *Order as part no. MX465J*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 24-pin PDIP Mechanical Outline: *Order as part no. MX465P*

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX805A

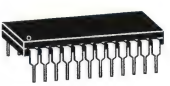
Subaudio Signaling Processor

DESCRIPTION

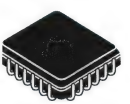
C-BUS COMPATIBLE

The MX805A, a member of the DBS800 IC family, is a subaudio frequency signaling processor that provides outband audio and digital signaling capability for LMR systems.

The MX805A is designed for the transmission and non-predictive reception of 1) Continuous Tone Controlled Subaudible Squelch (CTCSS) tones and other non-standard frequencies, and 2) Non-Return-to-Zero (NRZ) data reception and transmission to provide Digitally Coded Squelch (DCS/DPL™) and LTR™ signaling.



MX805AJ
24-pin CDIP



MX805ALH
24-pin PLCC

The MX805A contains the following:

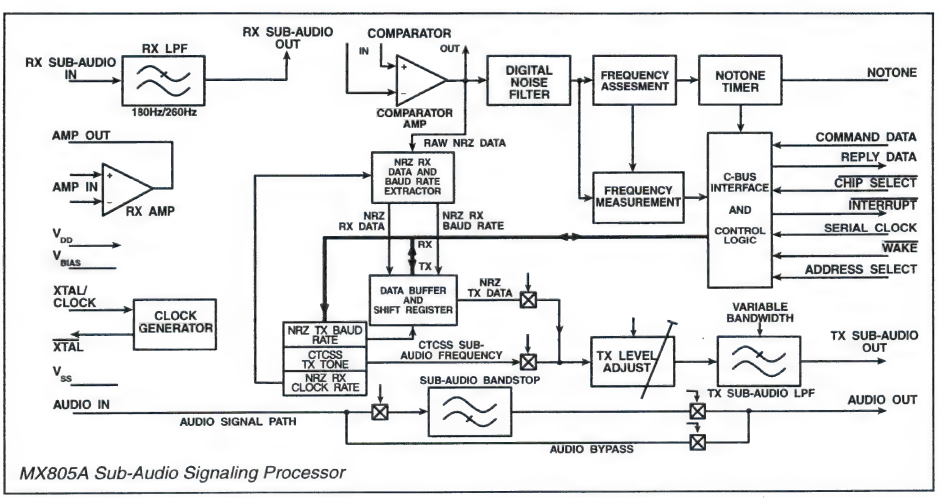
- •A non-predictive CTCSS Tone Decoder and DCS subaudio signal demodulator.
- •A CTCSS/NRZ Encoder with TX level adjustment and lowpass filter output stage with optional NRZ pre-emphasis.
- •A selectable subaudio bandstop filter.
- •A Notone (CTCSS RX) period timer.

Setting of the MX805A functions and modes is by data loaded from the microcontroller to the controlling registers within the device. Reply Data and Interrupt protocol keep the microcontroller up to date on the operational status of the circuitry.

CTCSS tone data for transmission is generated in the microcontroller, loaded to the CTCSS TX Frequency Register, encoded and output as a tone via the TX Sub-Audio LPF.

Received non-predicted CTCSS tone frequencies are measured and the resulting data, in the form of a 2-byte data word, is presented to the microcontroller for matching against a lookup table. Noise filtering is provided to improve the signal quality prior to measurement.

NRZ coded data streams for transmission, when generated within a microcontroller,



MX805A Sub-Audio Signaling Processor

DPL is a trademark of Motorola, Inc. LTR is a trademark of E.F. Johnson Co.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

DESCRIPTION...

are loaded to the NRZ TX Data Buffer and output, in 8-bit bytes, through the lowpass filter circuitry as subaudible signals. DCS turnoff tones can be added to the data signals by switching the MX805A to the CTCSS transmit mode at the appropriate time. NRZ coding is produced by the microcontroller and translated to subaudio signals by the MX805A.

Received NRZ data is filtered, detected, and placed into the NRZ RX Data Register, which is then available for transfer (one byte at a time) to the microcontroller for decoding by software. Clock extraction circuitry is provided on-chip. TX and RX baud rates are selectable.

Hardware and software are designed to allow consecutive addressing of two MX805A Sub-Audio Signaling Processors to achieve multimode duplex operation. Powersaving may be controlled by software or an input dedicated to the purpose.

The MX805A is a low-power 5 volt CMOS IC available in 24-pin CDIP and 24-lead plastic SMT packages. It is pin-compatible with the earlier MX805.

PIN FUNCTION CHART

Pin	Function
1	**$\overline{\text{Xtal}}$:** The output from the on-chip clock oscillator inverter. External components are required at this input when a Xtal input is used. See Figure 2.
2	**Xtal/Clock:** The input to the clock oscillator inverter. A Xtal or externally derived clock should be connected here.
3	**Address Select:** This input enables two MX805As to be used on the same C-BUS to provide full-duplex operation. See Tables 1 and 2.
4	**$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$):** The output of this pin indicates an interrupt condition to the microcontroller by going to a logic "0." This "wire-or-able" output allows the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin has a low impedance pulldown to logic "0" when active, and a high impedance when inactive. The system $\overline{\text{IRQ}}$ line requires 1 pullup resistor to V_{DD}. The conditions that cause interrupts are indicated in the Status Register (Table 4) and are shown below: RX CTCSS Tone Measurement Completed CTCSS NOTONE Timer Expired 1 NRZ RX Data Byte Received New NRZ Data Received Before Last Byte Read NRZ TX Buffer Ready NRZ Data Transmission Complete
5	**Serial Clock:** This is the "C-BUS" serial clock input. This clock, produced by the microcontroller, is used for transfer timing of commands and data to and from the MX805A. See timing diagrams.
6	**Command Data:** This is the C-BUS serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (bit 7) first and LSB (bit 0) last, synchronized to the Serial Clock. See timing diagrams.
7	**$\overline{\text{Chip Select}}$ ($\overline{\text{CS}}$):** This is the "C-BUS" data loading control function. This input is provided by the microcontroller. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See timing diagrams.
8	**Reply Data:** This is the C-BUS serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the $\overline{\text{Chip Select}}$ input. This 3-state output is held at high impedance when not sending data to the microcontroller. See timing diagrams.
9	**TX Sub-Audio Out:** This is the subaudio output (pure or NRZ derived). Signals are band limited. The TX Output Filter has a variable bandwidth (see Table 6). This output is at V_{BIAS} (a) when the NRZ Encoder is enabled but no data is being transmitted, (b) when the MX805A is placed in the Powersave All condition.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

PIN FUNCTION CHART

Pin	Function
10	**Audio In:** This is the input to the switched subaudio bandstop (highpass) filter. It is internally biased, and should be a.c. coupled by capacitor C_7.
11	**Audio Out**: This is the output of the audio signal path (filter or bypass). It is controlled by the Control Register. When disabled, the pin is held at V_{BIAS}.
12	**V_{SS}:** Negative supply (GND).
13	**RX Amp In (-):** This is the inverting input to the on-chip RX Input Amp (see Figures 2, 3 and 4).
14	**RX Amp In (+):** This is the non-inverting input to the on-chip RX Input Amp.
15	**RX Amp Out:** This is the output of the on-chip RX Input Op-Amp. This circuit may be used, with external components, as a signal amplifier and anti-aliasing filter prior to the RX Lowpass Filter, or for other purposes. See Figure 2 for component details.
16	**RX Sub-Audio In:** This is the received Sub-Audio (CTCSS/NRZ) input. It is internally referenced to V_{BIAS}. The signal to this pin should be a.c. coupled or biased. See Figure 2.
17	**RX Sub-Audio Out:** This is the output of the RX lowpass filter. It may be coupled into the on-chip amplifier or comparator as required.
18	**V_{BIAS}:** The internal circuitry bias line, held at »V_{DD}/2. This pin must be decoupled to V_{SS} by capacitor C_8 (see Figure 2).
19	**Comparator In (-):** This is the inverting input to the on-chip "comparator" amplifier. See Figures 2, 3 and 4.
20	**Comparator In (+):** This is the non-inverting input to the on-chip "comparator" amplifier. See Figures 2, 3 and 4.
21	**Comparator Out:** This is the output of the "comparator" amplifier. This node is also connected internally to the input of the Digital Noise Filter (See Figure 1). When both decoders (CTCSS or NRZ) are powersaved, this output is at logic "0."
22	**Notone Timing:** External RC components connected to this pin form the timing mechanism of a Notone period timer. The external network determines the "charge rate" of the timer to V_{BIAS}. The expiration of the timer will cause an interrupt. This function is only used in the CTCSS RX mode. See page 9.
23	**$\overline{\text{Wake}}$:** This "real time" input can be used to reactivate the MX805A from the "Powersave All" condition using an externally derived signal. The MX805A will be in a "Powersave All" condition when both this pin and bit 0 of the Control Register are set to a logic "1." Recovery from "Powersave All" is achieved by putting either the $\overline{\text{Wake}}$ pin or the "Powersave All" bit at logic "0." This allows MX805A activation by the microcontroller or an external signal, such as RSSI or Carrier Detect.
24	**V_{DD}:** Positive supply. A single +5 volt regulated supply is required.

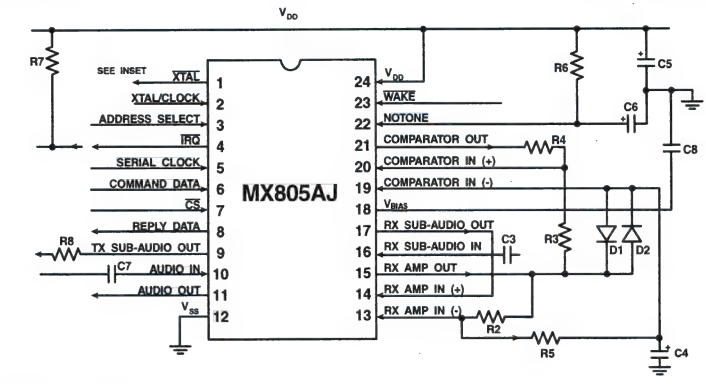
NOTES:

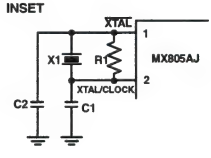
More information on external components and the DBS 800 system integration of the MX805A are contained in the DBS 800 System Support Document. Guidance on the generation and manipulation of NRZ and RX and TX data is given in the DBS 800 Application support document.

C-BUS is MX-COM's proprietary standard for the transmission of commands and data between a microcontroller and DBS 800 microcircuits. It may be used with any microcontroller, and can, if desired, take advantage of the hardware and serial I/O functions embodied into many types of microcontrollers. The C-BUS data rate is determined by the microcontroller.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Application Information





Component	Value		
R1	1.0MΩ	C1	See Note 5
R2	360kΩ	C2	See Note 5
R3	10.0kΩ	C3	1.5µF
R4	150kΩ	C4	15.0µF, 6V Tant. ±20%
R5	100kΩ	C5	1.0µF, 10V Tant. ±20%
R6	150kΩ	C6	1.0µF, 10V Tant. ±20%
R7	22.0kΩ	C7	0.1µF, 25V x 7R ±20%
R8	360kΩ	C8	1.0µF
		D1	silicon small signal
		D2	silicon small signal
Tolerance: R = ±5%		X1	4.00MHz

Figure 2 - Recommended External Components

Notes

1. Xtal/Clock circuitry components shown in INSET are recommended in accordance with MX-COM's "Standard and DBS 800 Crystal Oscillators" application note.

2. Resistor R8 is a System Component. Its value is chosen together with the MX806A Modulation Summing Amplifier to provide a subaudio signal level of -11.0dB to the system modulator.

3. Figures 3 and 4 illustrate alternative input component configurations.

4. The values of R2 and R5 are dependent on the input signal level. Values given are for the specified composite signal (reference page 14). R4 adds hysteresis to the comparator and is not always required.

5. The values used for C_1 and C_2 are determined by the frequency of X_1.

As a guide:

$C_1 = C_2 = 33pF$ for $X_1 < 5.0MHz$.

$C_1 = C_2 = 18pF$ for $X_1 > 5.0MHz$.

If the on-chip Xtal oscillator is to be used, then the external components X_1, C_1, C_2, and R_1 are required as shown in Figure 2 (inset). If an external clock source is used these components are not required; the input should be connected to the Xtal/clock pin and the $\overline{Xtal}$ pin left unconnected.

6. Resistor R7 is used as the DBS 800 system common pullup for the C-BUS Interrupt Request ($\overline{IRQ}$) line. The optimum value of this component will depend upon the circuitry connected to the $\overline{IRQ}$ line.

7. The level at this point should be approximately 900mV peak to peak.

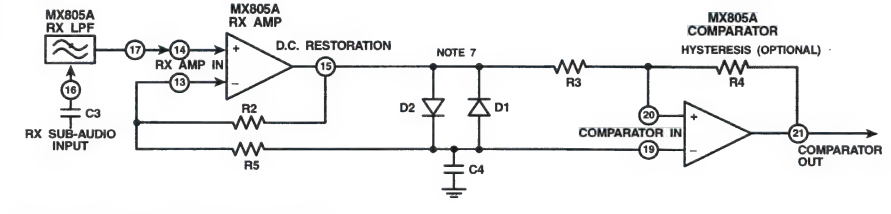


Figure 3 - MX805A Input Components

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Application Information

Figure 3 shows an input configuration that is generally for use for CTCSS signal and NRZ data reception.

Input coupling capacitor C3 is required because the RX Sub-Audio Input is held at V_{BIAS} during all powered conditions of the MX805A. Diodes D_1 and D_2 can be any silicon small-signal diode.

The output resistance (open loop) of the on-chip RX Amp is ≈6kΩ. In the configuration shown in Figure 3, the (RX Amp) RC time constant is therefore 90ms. If this period is too long for some systems, i.e. those using half-duplex, short data burst, an external amplifier should be considered in place of the on-chip RX Amp.

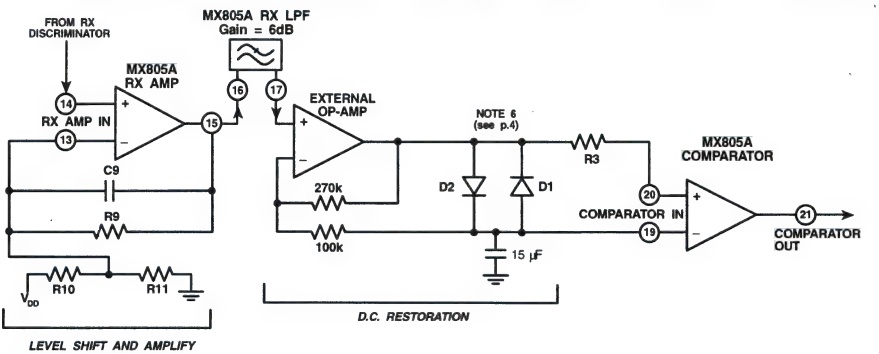


Figure 4 - MX805 Input Components using an External Op-Amp

Using An External Op-Amp

For d.c. coupling the MX805A to the receiver's discriminator output when using burst mode NRZ communication, it is recommended that an additional, external Op-Amp is employed as configured in Figure 4. This configuration will quickly compensate for sudden shifts of DC input bias.

Components R_9, R_{10}, and R_{11} should be calculated to provide an accurate potential of 2.5 Vd.c. (equal to V_{BIAS}) at pin junction 15/16 when using a discriminator input and 900 mV peak to peak at the output of the external op-amp. Note that the MX805A LPF has a 6 dB gain. If additional filtering is required, C_9 should be used; it should be calculated with R_9 to provide a lowpass cutoff frequency (f_{CO}) of 500 Hz.

Operating Modes

NRZ Encoding

The NRZ Encoder is formed by a shift register and the TX Sub-Audio Lowpass Filter. Data loaded from the Command Data line is output one 8-bit byte at a time from the NRZ TX Data Register. The output data level may be adjusted and filtered. Data may be pre-emphasized via a C-BUS command. The expected RX baud rate is programmed as the NRZ TX Baud Rate ($R_{NRZ\,TX}$). See Table 5.

CTCSS Encoding

The CTCSS Tone Encoder is comprised of a clock-divider programmed by an 11-bit binary number (Q) loaded to the CTCSS TX Frequency Register (see Table 5) via the C-BUS Command Data line.

The square-wave output of the encoder is fed through the TX Level Adjust variable gain block to the TX Sub-Audio lowpass filter, a variable bandwidth circuit controlled by 4 bits (P) of the CTCSS TX Frequency Register. The TX Sub-Audio output is a sine-wave. Standard and nonstandard subaudio tones are available. A CDCS turnoff tone may also be generated.

NRZ Decoding

Input (NRZ type) subaudio signals are filtered and the data clock extracted. Decoded data is serially loaded into a shift register buffer. This data is output one 8-bit byte at a time as Reply Data from the NRZ RX Data Register to the microcontroller. The expected RX baud rate is programmed as the NRZ RX Baud Rate ($R_{NRZ\,RX}$). See Table 5. Any codeword recognition can be carried out by software.

CTCSS Decoding

Received CTCSS signals are filtered, and coherence is increased by the digital noise filter. The quality of the signal is assessed by measurement of the cycle-to-cycle period variance and, provided it is sufficiently good, the frequency is measured over a period of 122.64 milliseconds (4.0 MHz xtal).

If the average signal quality is consistently too low, Notone is indicated; if not, the input frequency is precisely indicated in the CTCSS RX Frequency Register in a binary form.

Any single subaudio tone within the specified range may be selected, enabling a DCS turnoff tone (of 134 Hz) to be decoded while in the NRZ RX mode.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol

Control of the MX805A Sub-Audio Signaling Processor's operation is by communication between the microcontroller and the MX805A internal registers on the C-BUS, using Address/Commands (A/Cs) and appended instructions or data (see Figure 9). The use and content of these instructions is detailed in the following paragraphs and tables. The Address Select Input enables the addressing of 2 separate MX805As on the C-BUS to provide full-duplex signaling.

MX805A Internal Registers

MX805A Internal Registers are detailed as follows:

Control Register ($70_H/78_H$) -- Write only, control and configuration of the MX805.

Status Register ($71_H/79_H$) -- Read only, reporting of device functions.

CTCSS RX Frequency Register ($72_H/7A_H$) -- Read only, a 2-byte binary word indicating the frequency of the received subaudio input.

CTCSS TX Frequency/NRZ TX or RX Baud Rate Register ($73_H/7B_H$) -- Write only, a 2-byte command to set the relevant parameters.

NRZ RX Data Register ($74_H/7C_H$) -- Read only, a single byte of received NRZ data.

NRX TX Data Register ($75_H/7D_H$) -- Write only, to load a single byte of NRZ data for transmission.

Gain Set Register ($76_H/7E_H$) -- Write only, a single byte to set the gain of the TX Lowpass Filter.

Address/Commands

The first byte of a loaded data sequence is always recognized by the C-BUS as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an Address/Command byte followed by either:

(i) further instructions or data
or (ii) a Status or data Reply.

Instructions and data are loaded and transferred, via C-BUS, in accordance with the timing information in Figures 9 and 10.

Placing the Address Select input at a logic "0" will address MX805A #1, a logic "1" will address MX805 #2.

Tables 1 and 2 show the list of A/C bytes relevant to the MX805A.

Command Assignment	Address/Command (A/C) Byte + Hex.	Binary MSB LSB		Data Bytes
General Reset	01	0 0 0 0 0 0 0 1		
Write to Control Register	70	0 1 1 1 0 0 0 0	+	1 byte instruction to Control Register
Read Status Register	71	0 1 1 1 0 0 0 1	+	1 byte reply from Status Register
Read CTCSS RX Freq. Reg.	72	0 1 1 1 0 0 1 0	+	2 byte reply of CTCSS RX Data
Write to CTCSS TX Freq./ NRZ Baud Rate Reg.	73	0 1 1 1 0 0 1 1	+	2 byte instruction for TX Frequency and NRZ TX/RX baud rates
Read NRZ RX Data Reg.	74	0 1 1 1 0 1 0 0	+	1 byte binary data Reply
Write to NRZ TX Data Reg.	75	0 1 1 1 0 1 0 1	+	1 byte binary data Command
Write to Gain Set Reg.	76	0 1 1 1 0 1 1 0	+	1 byte instruction for TX Output

Table 1 - MX805A #1 C-BUS Address/Commands - (Address Select input at a logic "0")

Command Assignment	Address/Command (A/C) Byte + Hex.	Binary MSB LSB		Data Bytes
General Reset	01	0 0 0 0 0 0 0 1		
Write to Control Register	78	0 1 1 1 1 0 0 0	+	1 byte instruction to Control Register
Read Status Register	79	0 1 1 1 1 0 0 1	+	1 byte reply from Status Register
Read CTCSS RX Freq. Reg.	7A	0 1 1 1 1 0 1 0	+	2 byte reply of CTCSS RX Data
Write to CTCSS TX Freq./ NRZ Baud Rate Reg.	7B	0 1 1 1 1 0 1 1	+	2 byte instruction for TX Frequency and NRZ TX/RX baud rates
Read NRZ RX Data Reg.	7C	0 1 1 1 1 1 0 0	+	1 byte binary data Reply
Write to NRZ TX Data Reg.	7D	0 1 1 1 1 1 0 1	+	1 byte binary data Command
Write to Gain Set Reg.	7E	0 1 1 1 1 1 1 0	+	1 byte instruction for TX Output

Table 2 - MX805A #2 C-BUS Address/Commands - (Address Select input at a logic "1")

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol...

"Write to Control Register" -- A/C 70_H (78_H), followed by 1 byte of Command Data

Table 3 below shows the configurations available to the MX805A. Bits 5, 6 and 7 are used together to Enable and Powersave circuit sections as required.

Setting			Control Bits	
MSB			*Transmitted First*	
7	*6*	*5*	**Enabled**	**Powersaved**
0	0	0	CTCSS Decoder	NRZ Decoder and Both Encoders
0	0	1	NRZ Decoder	CTCSS Decoder and Both Encoders
0	1	0	CTCSS Encoder	All Decoders
0	1	1	NRZ Encoder	All Decoders
1	0	0	CTCSS Encoder and Decoder	NRZ Encoder and Decoder
1	0	1	NRZ Encoder and CTCSS Decoder	No circuits
1	1	0	NRZ Decoder and CTCSS Decoder	All Encoders
1	1	1	NRZ Decoder	All Encoders except TX Sub-Audio LPF and CTCSS Decoder
		4		
		1	Enable Audio Output -- Used with Bit 3	
		0	Disable Audio Output -- Output to V_{BIAS}	
		3		
		1	Enable Sub-Audio Bandstop Filter (Audio Signal Path)	
		0	Bypass Sub-Audio Bandstop Filter	
		2		
		1	Enable All MX805A Interrupts	
		0	Disable All MX805A Interrupts	
		1		
		1	Set RX Lowpass Filter Bandwidth to 180Hz -- For low CTCSS tones or NRZ data	
		0	Set RX Lowpass Filter Bandwidth to 260Hz	
		0		
		1	All Encoders and Decoders Powersaved	
		0	All Encoders and Decoders Enabled unless individually Powersaved	

Table 3 - Control Register

General Reset

Upon power-up the bits in the MX805A registers will be random (either "0" or "1"). A General Reset Command 01_H) will be required to reset all ICs on the C-BUS. It has the following effect on the MX805A:

Control Register	Set as 00_H
Status Register	Set as 00_H
Notone Timer	Discharged

Warning: The following MX805A register configurations are not affected by a General Reset Command:

CTCSS RX Frequency
CTCSS TX Frequency/NRZ Baud Rate Register
NRZ RX Data Register
NRZ TX Data Register
Gain Set Register

Note that setting the Control Register in this way will set the MX805A to the CTCSS decode mode and overwrite a "Powersave All" instruction. It should also be considered that a General Reset command will reset ALL DBS 800 ICs operating on the C-BUS.

Glossary of Abbreviations

Below is a list of abbreviations used in this Data Bulletin.

DCS	Continuous Digitally Coded Squelch
CTCSS	Continuous Tone Controlled Sub-Audible Squelch
DPL™	Digital Private Line
LTR™	Logic Trunked Radio
NRZ	Non-Return-to Zero
f_{CO}	Filter Cutoff frequency
$f_{CTCSS\ IN}$	Subaudio RX frequency
$f_{CTCSS\ OUT}$	Subaudio TX frequency
f_{TONE}	Tone frequency
f_{XTAL}	Xtal/Clock frequency
$R_{NRZ\ RX}$	NRZ RX baud rate
$R_{NRZ\ TX}$	NRZ TX baud rate
S_{INPUT}	Audio input signal

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol...

"Read Status Register" -- A/C 71_H (79_H), followed by 1 byte of Reply Data

The Status Register indicates the operational condition of the MX805A. Bits 0 to 5 are set individually to indicate specific actions within the device. When a Status bit is set to a logic 1, an Interrupt Request (IRQ) output is generated. A read of the Status Register will reset the Interrupt and ascertain the state of this register. Table 4 shows the conditions indicated by the Status bits.

Setting	Set By	Logic	Cleared By	Logic
MSB 7, 6	Received First Not used	"0"	Not used	"0"
5	NRZ data transmission complete. No new data is loaded.	1	1. Write to NRZ TX Data Reg., or 2. General Reset, or 3. NRZ Encoder Powersave	0
4	NRZ TX Data Buffer ready for next data byte.	1	1. Write to NRZ TX Data Reg., or 2. General Reset, or 3. NRZ TX Powersave	0
3	New NRZ RX data received before last byte was read.	1	1. Read NRZ RX Data Reg., or 2. General Reset, or 3. NRZ Decoder Powersave	0
2	1 byte of NRZ RX data received.	1	1. Read NRZ RX Data Reg., or 2. General Reset, or 3. NRZ Decoder Powersave	0
1	Notone Timer period expired.	1	1. Read Status Register, or 2. General Reset, or 3. CTCSS Decoder Powersave	0
0	RX Tone Measurement Complete	1	1. Read Status Register, or 2. General Reset, or 3. CTCSS Decoder Powersave	0

Table 4 - Status Register

"Read CTCSS RX Frequency Register" -- A/C 72_H ($7A_H$), followed by 2 bytes of Reply Data

Measurement of CTCSS RX Frequency ($f_{CTCSS\ IN}$)

The input subaudio signal ($f_{CTCSS\ IN}$) is filtered, doubled and measured in the Frequency Counter over the "measurement period" (122.64ms) (4.0 MHz Xtal).

The measuring function counts the number of complete input cycles occurring within the measurement period and then the number of measuring-clock cycles necessary to make up the period.

When the measurement period of a successful decode is complete, the RX Tone Measurement bit in the Status Register and the Interrupt bit are set.

The CTCSS RX Frequency Register will now indicate the subaudio signal frequency ($f_{CTCSS\ IN}$) in the form of 2 data bytes (1 and 0) as illustrated in Figure 6.

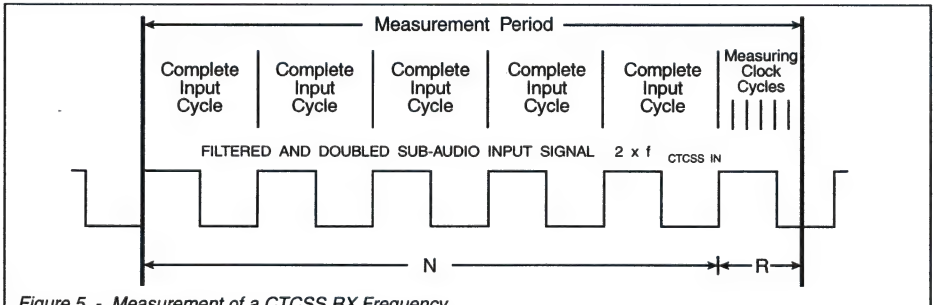


Figure 5 - Measurement of a CTCSS RX Frequency

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol...

"Read CTCSS RX Frequency Register"...

The Integer (N) -- Byte 1
A binary number representing twice the number of complete input subaudio cycle periods counted during the measurement period of 122.64ms (4.0 MHz Xtal).

The Remainder (R) -- Byte 0
A binary number representing the remainder part, R, of 2 x the Sub-Audio Input Frequency. R = number of specified measuring-clock cycles required to complete the specified measurement period (See N). The clock cycle frequency is 4166.6Hz (4.0 MHz Xtal).

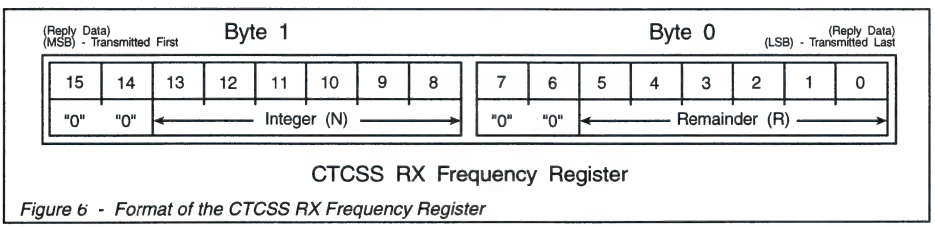

(Reply Data) (MSB) - Transmitted First
Byte 1
Byte 0
(Reply Data) (LSB) - Transmitted Last
15 14 13 12 11 10 9 8
7 6 5 4 3 2 1 0
"0" "0" Integer (N)
"0" "0" Remainder (R)
CTCSS RX Frequency Register

Figure 6 - Format of the CTCSS RX Frequency Register

CTCSS RX Frequency Register

Figure 6 above shows the format of the CTCSS RX Frequency Register.

Bits 8 (LSB) to 13 (MSB) are used to represent the Integer (N). From Byte 1, valid values of $N = 16 \leq N \leq 61$. i.e. values of N less than 16 and greater than 61 are not within the specified frequency band.

Bits 0 (LSB) to 5 (MSB) are used to represent the Remainder (R). From Byte 0, valid values of $R \leq 31$.

This register is not affected by the General Reset command (01_H) and may adopt any random configuration at Power-Up.

CTCSS RX Frequency Measurement Formulas

To assist in the production of "lookup" tables and limit-values in the microcontroller, and to provide guidance upon the determination of N and R from a measured CTCSS frequency, the following formulas show the derivation of the CTCSS RX Frequency ($f_{CTCSS\ IN}$) from the measured data bytes (N and R).

$f_{CTCSS\ IN}$
In the measurement period of 122.64ms there are N cycles at $2 \times f_{CTCSS\ IN}$ and R clock cycles at 4166.6Hz, for any input frequency.

So,

$$f_{CTCSS\ IN} = \frac{N \times f_{XTAL}}{1920 \times (511-R)} \text{ Hz} \quad [1]$$

$$N = \text{INT}\left[\frac{1920 \times 511 \times f_{CTCSS\ IN}}{f_{XTAL}}\right] \quad [2]$$

$$R = \text{INT}\left[511 - \left[\frac{N \times f_{XTAL}}{1920 \times f_{CTCSS\ IN}}\right] + 0.5\right] \quad [3]$$

Calculate N first

Examples (f_{XTAL} = 4.00MHz): $f_{CTCSS\ IN}$ = 100Hz N = 24 R = 11; $f_{CTCSS\ IN}$ = 250Hz N = 61 R = 3

Notone Timing

The input subaudio signal is monitored by the Frequency Assessment circuitry. Before any Notone action is enabled, the MX805A must have achieved at least one successful "Tone Measurement Complete" action.

If there is no signal or the signal is of a consistently poor quality, the Notone Timer will start to charge via the timing components. When the timing period has expired (at $V_{DD}/2$), an Interrupt and a Status bit (Notone Timer Expired) are generated. This is a one-shot function which is reset by a "Tone Measurement Complete" interrupt.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol...

"Write to CTCSS TX Frequency/NRZ Baud Rate Register" -- A/C 73_H ($7B_H$), followed by 2 bytes of Command Data

The information loaded to this register will set either the:

(a) CTCSS TX Tone Frequency $f_{CTCSS\ OUT}$
(b) NRZ TX Baud Rate $R_{NRZ\ TX}$
(c) NRZ RX Baud Rate $R_{NRZ\ RX}$

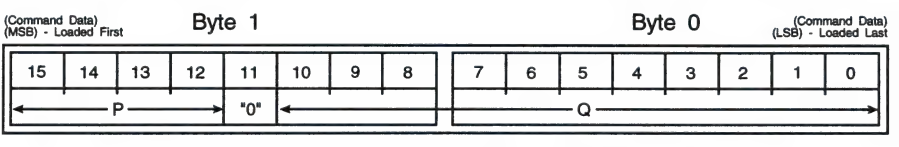
The chosen mode for this register (a, b or c) is determined by the MX805A modes enabled by the Control Register, as shown in the table below.

Control Register Bits 7	6	5	MX805 Mode Enabled	CTCSS TX/NRZ Baud Rate Register Function
0	0	0	CTCSS Decode	
0	0	1	NRZ Decode	NRZ RX Baud Rate
0	1	0	CTCSS Encode	CTCSS TX Frequency
0	1	1	NRZ Encode	NRZ TX Baud Rate
1	0	0	CTCSS Encode and Decode	CTCSS TX Frequency
1	0	1	NRZ Encode & CTCSS Decode	NRZ TX Baud Rate
1	1	0	NRZ & CTCSS Decode	NRZ RX Baud Rate
1	1	1	NRZ Decode	NRZ RX Baud Rate

Table 5 - CTCSS Frequency/NRZ Baud Rate Register Configurations

Data Format

Data is transmitted to this register as 2 bytes of Command Data in the form illustrated in the diagram below. This register is not affected by the General Reset Command (01_H) and may adopt any random configuration at power-up.



CTCSS TX Frequency/NRZ Baud Rate Register

Figure 7 - Format of the CTCSS TX Frequency/NRZ Baud Rate Register

Command Words P and Q

The two data words, P and Q, loaded to this register are interpreted as:

P = a binary number to set the TX Sub-Audio Lowpass Filter bandwidth (applicable to NRZ and CTCSS modes).
Q = a binary number to set the frequency or baud rate of the selected function.

Command Word P

Bits 15	14	LSB 13	12	P	LPF Bandwidth
0	0	1	0	2	300Hz
0	0	1	1	3	200Hz
0	1	0	0	4	150Hz
0	1	0	1	5	120Hz
0	1	1	0	6	100Hz
0	1	1	1	7	85.7Hz
1	0	0	0	8	75Hz

Table 6 - Valid Values of P

Bits 12 to 15 are used to produce the data word "P" as shown in the table at left. The cutoff frequency $f_{C/O}$ (0.5dB point) of the TX Sub-Audio Lowpass filter is calculated as:

$$f_{C/O} = \frac{f_{XTAL}}{32 \times 208.33 \times P}$$

$$\text{so } P = \frac{f_{XTAL}}{32 \times 208.33 \times f_{CO}}$$

Table 6 is given as an example and calculated using a Xtal/Clock (f_{XTAL}) frequency of 4.00MHz. As illustrated, only values of "P" of 2 to 8 are usable.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol...

"Write to CTCSS TX Frequency/NRZ Baud Rate Register"...

Command Word "Q"

Bits 0 to 10 (see Figure 7) are used to produce the data word "Q" which sets one of the parameters described below. As you can see, Command Word "Q" could be used to produce a parameter outside that specified in the "Characteristics" section of this data bulletin. Care should be taken not to do this. Examples for limits of "Q" in each operational configuration are included. "Q" = 0 is not valid in the following calculations. Bit 11 is not used and must be set to logic "0."

(a) CTCSS TX Tone Frequency ($f_{CTCSS\ OUT}$)

$$f_{CTCSS\ OUT} = \frac{f_{XTAL}}{32 \times \text{"Q"}} \text{ Hz}$$

$$\text{so "Q"} = \frac{f_{XTAL}}{32 \times f_{CTCSS\ OUT}} \text{ Hz}$$

Example Limits

$f_{CTCSS\ OUT}$ = 67Hz
so "Q" = 1866 "11101001010"

$f_{CTCSS\ OUT}$ = 250Hz
so "Q" = 500 "00111110100"

(b) NRZ TX Baud Rate ($R_{NRZ\ TX}$)

$$R_{NRZ\ TX} = \frac{f_{XTAL}}{32 \times \text{"Q"}} \text{ bits/sec.}$$

$$\text{so "Q"} = \frac{f_{XTAL}}{32 \times R_{NRZ\ TX}}$$

Example Limits

$R_{NRZ\ TX}$ = 67bits/sec.
so "Q" = 1866 "11101001010"

$R_{NRZ\ TX}$ = 300bits/sec.
so "Q" = 417 "00110100001"

(c) NRZ RX Baud Rate ($R_{NRZ\ RX}$)

$$R_{NRZ\ RX} = \frac{f_{XTAL}}{32 \times 11 \times \text{"Q"}} \text{ bits/sec.}$$

$$\text{so "Q"} = \frac{f_{XTAL}}{352 \times R_{NRZ\ RX}}$$

Example Limits

$R_{NRZ\ RX}$ = 100bits/sec.
so "Q" = 114 "00001110010"

$R_{NRZ\ RX}$ = 300bits/sec.
so "Q" = 38 "00000100110"

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol...

"Read NRZ RX Data Register" -- A/C 74_H ($7C_H$), followed by 1 byte of Reply Data

Received NRZ data bits are organized into bytes and made available to the microcontroller via the Reply Data line. As 8 bits are received into this register an interrupt is generated to indicate that a complete byte has been received. This byte must be read before the arrival of the last (8th) bit of the next incoming byte. If this is not done, an interrupt to indicate this condition will be generated and the previous RX data is discarded. (See Table 4.)

Word synchronization is not provided. Byte synchronization and any codeword recognition will be performed by the host microcontroller. The RX baud rate is set by writing to the CTCSS TX Frequency/NRZ Baud Rate Register (73_H/$7B_H$). The first bit received is the first bit sent to the microcontroller.

This register is not affected by the General Reset Command (01_H), and may adopt any random configuration at Power-Up.

"Write to NRZ TX Data Register" -- A/C 75_H ($7D_H$), followed by 1 byte of Command Data

A byte for transmission is loaded from the C-BUS Command Data line with this A/C. The first data bit received via the C-BUS is transmitted first. This transmitter operation is non-inverting.

The first data byte loaded after the NRZ Encoder is enabled (Control Register) initiates the transmission sequence and an interrupt will be generated when the NRZ TX Data Buffer is ready for the next data byte. Subsequently, interrupts occur for every 8 bits transmitted.

Transmission is terminated, the TX Sub-Audio Output is placed at V_{BIAS}, and an interrupt is generated if the next byte is not loaded within 7 bit periods (see Table 4).

This register is not affected by the General Reset Command (01_H), and may adopt any random configuration at Power-Up.

"Write to Gain Set Register" -- A/C 76_H ($7E_H$), followed by 1 byte of Command Data

Setting				Gain Setting
MSB				
7	*6*	*5*	*4*	***Transmitted Bit 7 First***
0	0	0	0	These 4 bits must be "0"
			3	**Pre-Emphasis Setting**
			1	1.72dB Gain Enabled
			0	1.72dB Gain Disabled
		2	*1*	*0*	**TX Level Adjust Gain Setting**
		0	0	0	-2.58dB
		0	0	1	-1.72dB
		0	1	0	-0.86dB
		0	1	1	0dB
		1	0	0	+0.86dB
		1	0	1	+1.72dB
		1	1	0	+2.58dB
		1	1	1	Not Used

Table 7 - Gain Set Register Settings

The Gain Set Register Settings

The settings of this register control the CTCSS and NRZ signal level that is presented at the TX Sub-Audio Output.

Bit 3, when enabled, is used to produce a pre-emphasis effect on the NRZ TX Data by increasing the gain of the data bit before a level change (see Figure 8), by 1.72dB to make that data pulse level slightly more positive (or negative). The signal level will be 1.72dB greater than that set by Bits 0 to 2. If the TX Sub-Audio Output level is set to +2.58dB, the pre-emphasized level will be +4.3dB.

The pre-emphasis function will remain enabled until disabled by setting Bit 3 to a logic 0 If this function remains enabled when using the CTCSS Encoder, the output signal may be adversely affected. Therefore this function should only be enabled when in the NRZ Encode mode.

This register is not affected by the General Reset Command (01_H), and may adopt any random configuration at Power-Up.

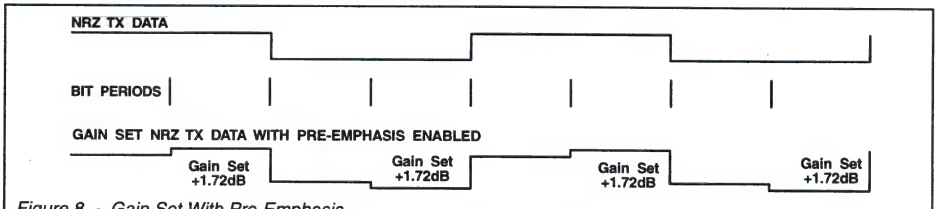


Figure 8 - Gain Set With Pre-Emphasis

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Timing Information

Figure 9 shows the timing parameters for two-way communication between the µC and the MX805A on the C-BUS.

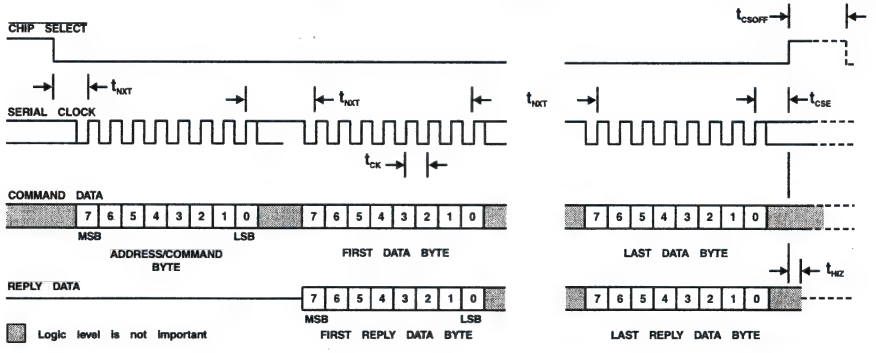


Figure 9 - C-BUS Timing

Parameter		Min.	Typ.	Max.	Unit
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0	-	-	µs
t_{CSH}	Last Serial Clock Rising Edge to Chip Select High	4.0	-	-	µs
t_{CSOFF}	Chip Select High	2.0	-	-	µs
t_{NXT}	Command Data Inter-Byte Time	4.0	-	-	µs
t_{CK}	Serial Clock Period	2.0	-	-	µs
t_{CH}	Decoder or Encoder Clock High	500	-	-	ns
t_{CL}	Decoder or Encoder Clock Low	500	-	-	ns
t_{CDS}	Command Data Set-Up Time	250	-	-	ns
t_{CDH}	Command Data Hold Time	0	-	-	ns
t_{RDS}	Reply Data Set-Up Time	250	-	-	ns
t_{RDH}	Reply Data Hold Time	50.0	-	-	ns
t_{HIZ}	Chip Select High to Reply Data High - Z	-		2.0	µs

Notes: 1. Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the MX805A MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into the MX805A and into the microcontroller on the rising Serial Clock edge.
3. Loaded data instructions are acted upon at the end of each individual, loaded byte.
4. To allow for differing microcontroller serial interface formats, the MX805A will work with either polarity Serial Clock pulses.

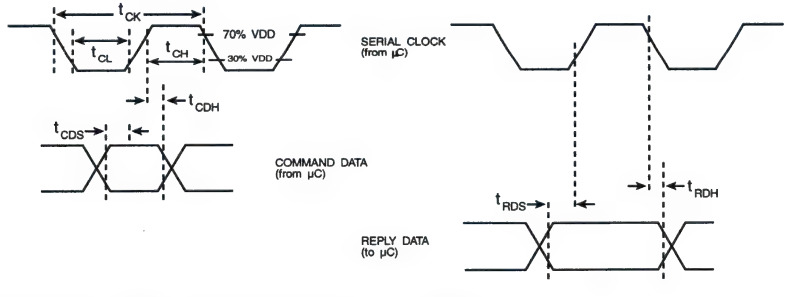


Figure 10 - Timing Relationships for C-BUS Information Transfer

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref. V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/Source Current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

XTAL/Clock frequency = 4.0MHz

Audio level 0dB ref. = 308mVrms @ 1kHz

Composite Signal = 308mVrms @ 1kHz +75mVrms Noise + 31mVrms Sub-Audio Signal

Noise Bandwidth = 5kHz Band Limited Gaussian

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current (All Functions Enabled)		-	5.0	7.0	mA
(Decoders only Enabled)		-	2.0	3.0	mA
(Powersave All)		-	0.9	1.5	mA
Analog Impedances					
RX Sub-Audio Input		350.0	1500.0	-	kΩ
Audio Input		350.0	-	-	kΩ
Audio Bypass Switch On	5	-	2.0	-	kΩ
Audio Bypass Switch Off	5	1.0	6.5	-	MΩ
RX Amp Input (+ and -)		1.0	6.5	-	MΩ
Comparator Input (+ and -)		1.0	6.5	-	MΩ
RX Sub-Audio Output		-	2.0	-	kΩ
TX Sub-Audio Output (Encoder Enabled)	5	-	2.0	-	kΩ
(Encoder Disabled)	5	-	500.0	-	kΩ
Audio Output (Enabled)	5	-	2.0	-	kΩ
(Disabled)	5	-	500.0	-	kΩ
RX Amp and Comparator Outputs					
(Large Signal)		-	6.0	-	kΩ
(Small Signal)		-	600.0	-	Ω
Dynamic Values					
Digital Interface					
Input Logic 1	1	3.5	-	-	V
Input logic 0	1	-	-	1.5	V
Output Logic 1 (IOH = -120µA)	2	4.6	-	-	V
Output Logic 0 (IOL - 360µA)	3	-	-	0.4	V
I_{OUT} Tristate (Logic 1 or 0)	3	-	-	4.0	µA
Input Capacitance	1	-	-	7.5	pF
Logic Input Current (V_{IN} = 0 to 5.0V)	1	-	-	1.0	µA
IOX (V_{OUT} = 5.0V)	4	-	-	4.0	µA

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Overall Performance					
CTCSS - Decode					
Sensitivity (Composite Signal)	6	-20.0	-26.0	-	dB
Response Time (Composite Signal)					
100 Hz to 257 Hz Tone		-	210.0	250.0	ms
65 Hz Tone	9	-	210.0	384.0	ms
Tone Measurement Resolution		-	0.2	-	%
Tone Measurement Accuracy		-0.5	-	+0.5	%
Notone Response Time (Composite Signal)	7	-	175.0	250.0	ms
False Tone Interrupts (Noise Input only)	10	-	20.0	-	/Hr.
CTCSS - Encode					
Frequency Range		65.0	-	257.0	Hz
Tone Frequency Resolution		-	-	0.2	%
Tone Amplitude Tolerance	12	-1.0	-	+1.0	dB
Rise Time (to 90%)		-	-	30.0	ms
Fall Time (to 10%)		-	-	50.0	ms
Total Harmonic Distortion		-	-	5.0	%
NRZ - Decode					
RX Bit Rate Sync Time		-	2	-	edges
RX Bit Error Rate	11	-	$1x10^{-3}$	-	$P_{(error)}$
NRZ - TX					
TX Bit Rate		67.0	-	300.0	bits/s
TX LPF (3dB) Bandwidth		75.0	-	300.0	Hz
Sub-Audio TX Output Level					
CTCSS		-	0	-	dB
NRZ		-	0.871	-	V p-p
Amplitude Adjustment Range		-2.58	-	2.58	dB
Adjustment Step Size (7 steps)	8	-	0.86	-	dB
Sub-Audio Bandstop Filter					
Passband		297.0	-	3000.0	Hz
Passband Gain (@ 1.0 kHz)		-	0	-	dB
Passband Ripple (w.r.t. gain at 1.0 kHz)		-1.5	-	0.5	dB
Stopband Gain					
< 250 Hz		-	36.0	-	dB
Residual Hum and Noise		-	-50.0	-45.7	dB
Alias Frequency		-	-	62.5	kHz
Receive Lowpass Filter (see Figure 11)					
Cutoff Frequency (-3dB)		-	280.0	-	Hz
Passband Gain		-	6.0	-	dB
Xtal/Clock Frequency (f_{XTAL})		-	4.0	6.1	MHz

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

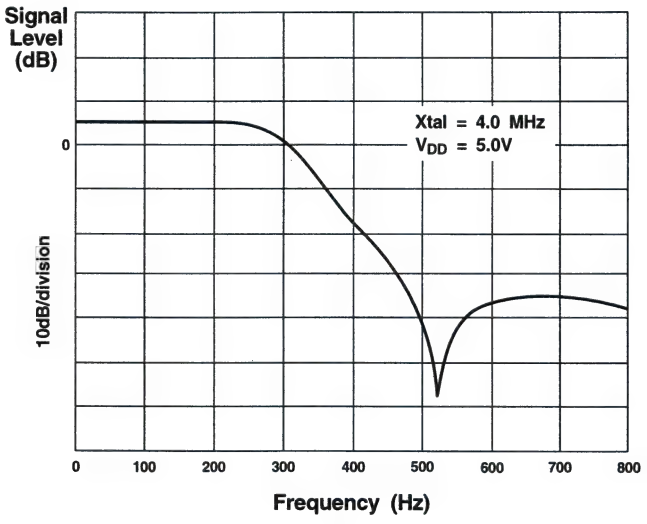


Figure 11 - Typical Frequency Response of RX Lowpass Filter

NOTES:

1. Device control pins: Serial Clock, Command Data, $\overline{\text{Wake}}$ and $\overline{\text{CS}}$.
2. Reply Data output.
3. Reply Data and $\overline{\text{IRQ}}$ outputs.
4. Leakage current into the "Off" $\overline{\text{IRQ}}$ output.
5. See Control Register
6. With input gain components set as recommended in Figure 2.
7. Probability 97%.
8. See Gain Set Register.
9. For $f_{CTCSSIN}$ of 65 Hz to 100 Hz, Response Time $t_R = (100/f_{TONE}) \times 250$ ms.
10. Distributed across the RX frequency band.
11. With 10dB signal-to-noise ratio in a bit-rate bandwidth.
12. At any gain setting of Gain Register.

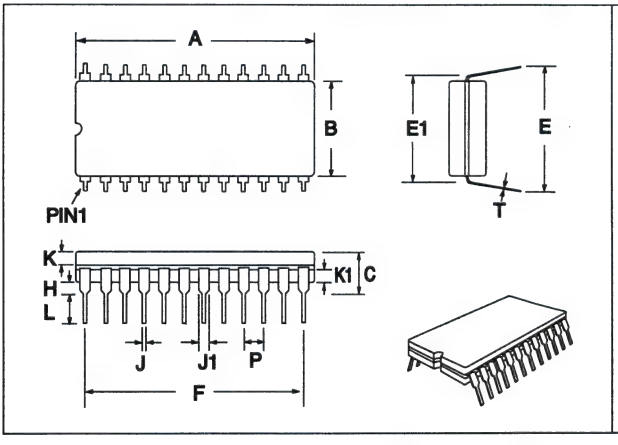
© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Packaging

The MX805AJ CDIP Package is shown in Figure 11. The MX805ALH is in Figure 12. For identification purposes the MX805ALH has an ident spot adjacent to pin 1 and a chamfered corner between pins 3 and 4.

Handling Precautions

The MX805A is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

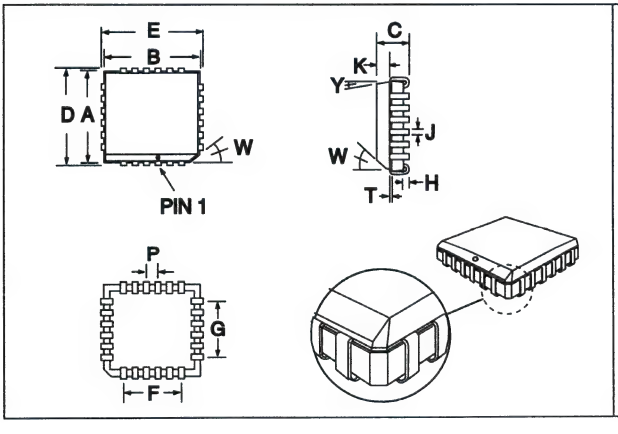


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE: All dimensions in inches (mm.)
Angles are in degrees

Figure 11 - MX805AJ 24-pin CDIP



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE: All dimensions in inches (mm.)
Angles are in degrees

Figure 12 - MX805ALH 24-pin PLCC

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480116.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX818 CTCSS Signaling Processor

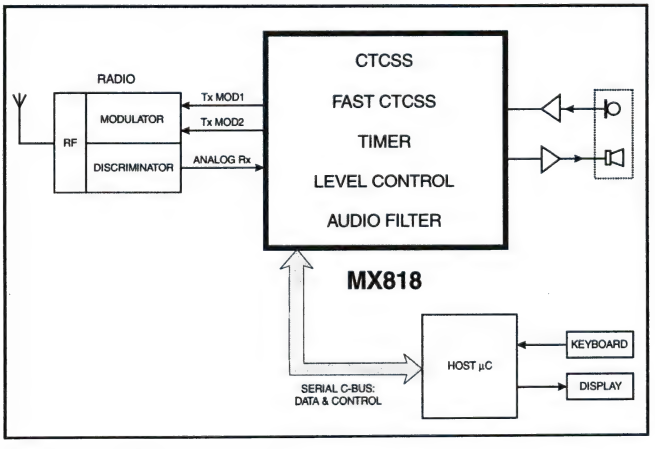
PRELIMINARY INFORMATION

Features

- **Fast CTCSS Detection**
- **Predictive Tone Detection**
- **Low Power 3.3V/5.0V Operation**
- **Variable Gain Audio Filter**
- **Programmable:**
  - **Modulator Drivers**
  - **Tone Decoder**
  - **Tone Encoder**
- **Pin compatible with enhanced function MX828**
- **Full control via 4-Wire Serial Interface**

Applications

- **Radio Systems Requiring Sub-Audible Signaling**
  - **Trunking Control**
  - **Selective Calling**
  - **Group Calling**
- **Increased Efficiency**
  - **Scanning Systems**
  - **Trunking Systems**



The MX818 is a low power CTCSS Signal Processor designed for use in the latest generation of LMR (Land Mobile Radio) equipment where sub-audible signaling is required for functions such as Trunking Control, Selective Calling and Group Calling applications. The MX818 is full duplex and offers many advanced features to assist in the operation of new CTCSS based systems including: programmable tone decoders to facilitate the decoding of between 1 and 15 programmable CTCSS tones, a CTCSS Fast/Predictive detector which may respond to a single programmed tone in less than 60ms, a high resolution tone encoder that will accurately generate CTCSS tones, and High and Low pass filters for CTCSS and Voice Band signals. The MX818 also provides on chip audio summation and digitally adjustable modulation drivers to facilitate design integration and reduce part count.

The MX818 may be used with a 3.0 to 5.5 volt supply and is available in the following packages: 24-pin SSOP(MX818DS), 24-pin SOIC (MX818DW), and 24-pin PDIP (MX818P).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

CONTENTS

Section **Page**

1. Block Diagram 3-81

2. Signal List 3-82

3. External Components 3-83

4. General Description 3-84

4.1 Software Description 3-84

4.1.1 Command Summary 3-84

4.1.2 Address/Commands 3-84

4.1.3 Write Only Register Description 3-84

4.1.4 8-bit Read Only Registers 3-92

4.1.5 Read Only Register Description 3-92

5. Application 3-96

5.1 General 3-96

5.2 Transmitter 3-96

5.3 Receiver (Decode) 3-96

5.4 Receiver (Fast Detect) 3-96

5.5 General Purpose Timer (GPT) 3-97

6. Performance Specification 3-99

6.1 Electrical Performance 3-99

6.1.1 Absolute Maximum Ratings 3-99

6.1.2 Operating Limits 3-99

6.1.3 Operating Characteristics 3-100

6.1.4 Timing Diagrams 3-103

6.2 Packaging 3-104

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1. Block Diagram

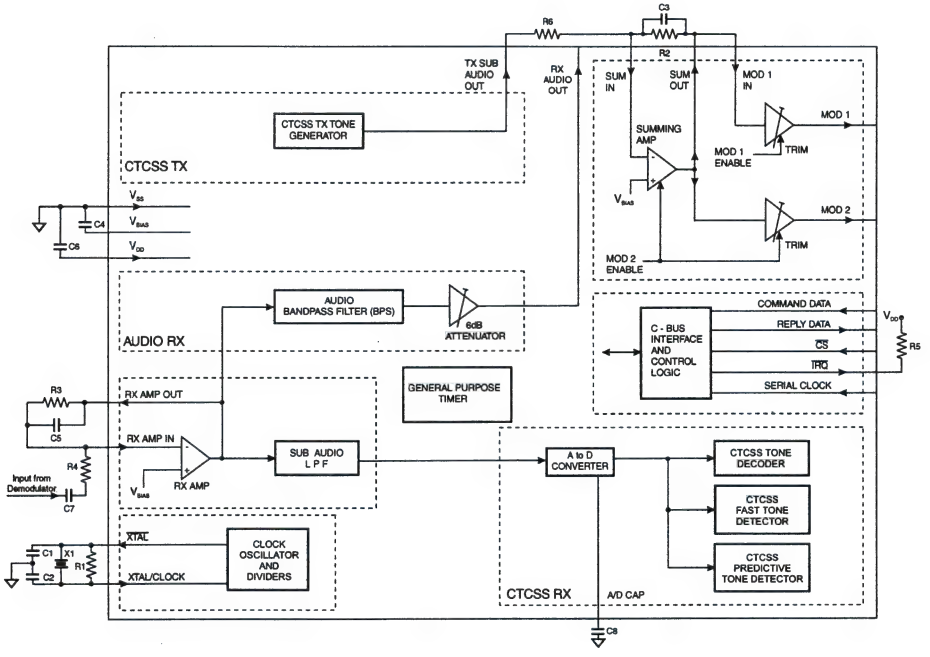


Figure 1: Device Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. Signal List

Pin No.	Name	Type	Description
1	$\overline{\text{XTAL}}$	output	The inverted output of the on-chip oscillator.
2	XTAL/CLOCK	input	The input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	input	The C-BUS serial clock input. This clock, produced by the µC, is used for transfer timing of commands and data to and from the device. See Figure 4
4	COMMAND DATA	input	The C-BUS serial data input from the µC. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the SERIAL CLOCK. See Figure 4
5	REPLY DATA	output	The C-BUS serial data output to the µC. The transmission of REPLY DATA bytes is synchronized to the SERIAL CLOCK under the control of the $\overline{\text{CS}}$ input. This tri-state output is held at high impedance when not sending data to the µC. See Figure 4
6	$\overline{\text{CS}}$	input	The C-BUS data loading control function: this input is provided by the µC. Data transfer sequences are initiated, completed or aborted by the $\overline{\text{CS}}$ signal. See Figure 4.
7	$\overline{\text{IRQ}}$	output	This output indicates an interrupt condition to the µC by going to a logic 0. This is a wire-ORable output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic 0 when active and a high-impedance when inactive. An external pullup resistor is required. The conditions that cause interrupts are indicated in the IRQ FLAG register and are effective if not masked out by a corresponding bit in the IRQ MASK register.
8	N/C		No internal connection. Do not make any connection to these pin
9	N/C		No internal connection. Do not make any connection to these pin
10	A/D CAP	output	An internal reference voltage for the A to D, decoupled to V_{SS} by an external capacitor.
11	N/C		No internal connection. Do not make any connection to this pin.
12	V_{SS}	power	Negative supply (ground).
13	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed by a capacitor mounted close to the device pins.
14	RX AMP IN	input	The inverting input to the Rx input amplifier.
15	RX AMP OUT	output	The output of the Rx input amplifier and the input to the audio filter section.
16	RX AUDIO OUT	output	Output of the Rx audio filter section.
17	N/C		No internal connection. Do not make any connection to this pin.
18	SUM IN	input	Input to the audio summing amplifier.
19	SUM OUT	output	Output of the audio summing amplifier, internally tied to input of MOD2
20	MOD1 IN	input	Input to MOD1 audio gain control.
21	TX SUB AUDIO OUT	output	Output of the CTCSS tone generator.
22	MOD1	output	Output of MOD1 audio gain control.
23	MOD2	output	Output of MOD2 audio gain control.
24	V_{DD}	power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components

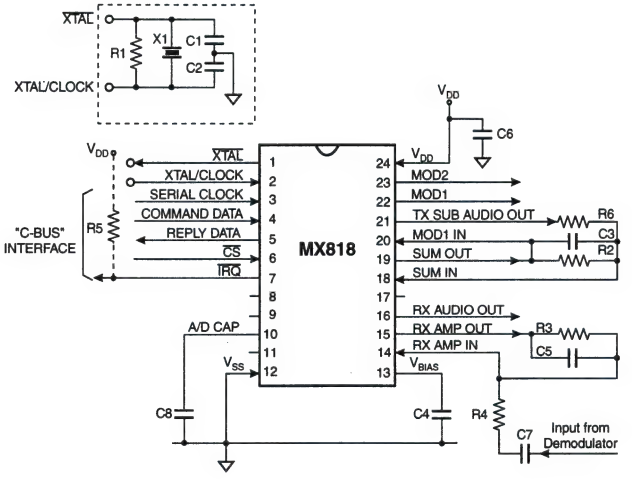


Figure 2: Recommended External Components

R1		1MΩ	±5%
R2	Note 2	100kΩ	±10%
R3	Note 3	100kΩ	±10%
R4	Note 3, 4		±10%
R5		22kΩ	±10%
R6	Note 2		±10%
C1		22pF	±20%
C2		22pF	±20%

C3	Note 2	100pF	±20%
C4		0.1µF	±20%
C5	Note 3	100pF	±20%
C6		0.1µF	±20%
C7	Note 3, 4		±20%
C8		0.1µF	±20%
X1	Note 1	4.032MHz	±100ppm

Table 1: Recommended External Components

Recommended External Components Notes:

1. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. R2, R6 and C3 form the gain components for the Summing Amplifier. R6 should be chosen as required from the system specification, using the following formula:

   $$\text{Tx Sub Audio Gain} = -\frac{R2}{R6}$$

3. R3, R4, C5 and C7 form the gain components for the Rx Input Amplifier. R4 should be chosen as required by the signal level, using the following formula:

   $$\text{Gain} = -\frac{R3}{R4}$$

4. C7 x R4 should be chosen so as not to compromise the low frequency performance of this product.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4. General Description

The MX818 is a programmable CTCSS sub-audio encoder/decoder for use in land mobile radio equipment.

The receiver section of the MX818 has a fast/predictive tone detector which operates in parallel with a tone decoder. The latter decodes a user-programmable set of up to 15 tones and performs a more accurate (but slower) analysis of the tones detected by the fast/predictive tone detector, which is a single detector that is switchable to provide either a fast response to any CTCSS tone (FAST DETECT mode) or a fast response to a single user-programmed CTCSS tone (PREDICTIVE mode).

The high pass audio filter is designed to filter out the CTCSS sub-audio tones. The summing and modulation amplifiers allow the audio modulation to be controlled digitally via the C-BUS. A general purpose timer is included.

Each function, and the routing of signals, is flexible and may be configured or controlled by the user's software.

4.1 Software Description

4.1.1 Command Summary

The following table contains a brief description of all valid Commands. Details follow below.

				DATA BYTE(S)	
REGISTER NAME	**SECTION**	**HEX ADDRESS COMMAND**	**READ / WRITE**	**BYTE 1**	**BYTE 2**
General Reset	4.1.3.1	$01	W	none	none
Sub-Audio Control	4.1.3.2	$80	W	Refer to Bit Description	none
Sub-Audio Status	4.1.4, 4.1.5.1	$81	R	Refer to Bit Description	none
Sub-Audio Set-Up	4.1.3.3	$82	W	Refer to Bit Description	none
CTCSS TX/ Fast RX Frequency	4.1.3.7	$83	W	Specify Tx or Fast Rx Frequency per command $80 & $83 Bit descriptions	
CTCSS RX Program	4.1.3.8	$84	W	1 of 15 possible Register Select & Decode Frequencies	
General Control	4.1.3.4	$88	W	Refer to Bit Description	none
Audio Control	4.1.3.9	$8A	W	Mod 1 Attenuation	Mod 2 Attenuation
General Purpose Timer	4.1.3.5	$8B	W	Refer to Bit Description	none
IRQ Mask	4.1.3.6	$8E	W	Refer to Bit Description	none
IRQ Flag	4.1.4, 4.1.5.2	$8F	R	Refer to Bit Description	none

Table 2: Command Summary

4.1.2 Address/Commands

Instructions and data are transferred, via C-BUS, in accordance with the timing information provided in Figure 4.

Instruction and data transactions to and from the MX818 consist of an Address/Command (A/C) byte followed by either:

a. further instruction or data (0,1, or 2 bytes)
b. status or Rx data reply (1 byte)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.1.2.1 8-bit Write Only Registers

HEX ADDRESS COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	GENERAL RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$80	SUB-AUDIO CONTROL	CTCSS TX ENABLE	CTCSS DECODE RX ENABLE	CTCSS FAST DETECT ENABLE	0	0	0	0	0
$82	SUB-AUDIO SET-UP	CTCSS DECODER BANDWIDTH MSB BIT 3	BIT 2	BIT 1	LSB BIT 0	FAST CTCSS MODE DETECT/ PREDICTIVE	0	0	0
$88	GENERAL CONTROL	AUDIO BAND-PASS FILTER BPF ENABLE	BPF UN-MUTE	BPF 6dB PAD	0	0	0	TIMER ENABLE	TIMER RE-CYCLE
$8B	GENERAL PURPOSE TIMER	GENERAL PURPOSE TIMER (GPT) MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8E	IRQ MASK	0	GPT IRQ MASK	0	0	CTCSS IRQ MASK	CTCSS FAST IRQ MASK	0	0

Table 3: 8-bit Write Only Register

4.1.2.2 16-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$83	CTCSS TX/ FAST RX FREQUENCY (1)	CTCSS (TX) NOTONE	0	0	CTCSS TX / FAST RX FREQUENCY MSB BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
	CTCSS TX/ FAST RX FREQUENCY (2)	CTCSS TX / FAST RX FREQUENCY BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$84	CTCSS RX PROGRAM (1)	CTCSS TONE ADDRESS MSB BIT 3	BIT 2	BIT 1	LSB BIT 0	CTCSS FREQUENCY MSB BIT 11	BIT 10	BIT 9	BIT 8
	CTCSS RX PROGRAM (2)	CTCSS FREQUENCY BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8A	AUDIO CONTROL (1)	0	0	MOD 1 ENABLE	MOD 1 MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
	AUDIO CONTROL (2)	0	0	MOD 2 ENABLE	MOD 2 MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0

Table 4: 16-bit Write Only Registers

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.1.3 Write Only Register Description

4.1.3.1 GENERAL RESET (Hex address $01)

The reset command has no data attached to it. It sets the device registers into the specific (all powersaved) states as listed below:

REGISTER NAME	HEX ADDRESS	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
SUB-AUDIO CONTROL	$80	0	0	0	0	0	0	0	0
SUB-AUDIO STATUS	$81	0	0	0	0	X	X	X	X
SUB-AUDIO SET-UP	$82	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX FREQUENCY (1)	$83	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX FREQUENCY (2)		0	0	0	0	0	0	0	0
CTCSS RX PROGRAM (1)	$84	0	0	0	0	0	0	0	0
CTCSS RX PROGRAM (2)		0	0	0	0	0	0	0	0
GENERAL CONTROL	$88	0	0	0	0	0	0	0	0
AUDIO CONTROL (1)	$8A	0	0	0	0	0	0	0	0
AUDIO CONTROL (2)		0	0	0	0	0	0	0	0
GENERAL PURPOSE TIMER	$8B	0	0	0	0	0	0	0	0
IRQ MASK	$8E	0	0	0	0	0	0	0	0
IRQ FLAG	$8F	0	0	0	0	0	0	0	0

X = undefined

Table 5: General Reset (Hex Address $01)

4.1.3.2 SUB-AUDIO CONTROL Register (Hex address $80)

This register is used to control the functions of the device as described below:

CTCSS TX ENABLE and DECODER ENABLE (Bits 7 and 6)	Bit 7 and Bit 6 enable and disable the CTCSS decoder (Rx) or transmitter (Tx) according to Table 7. See Note 1
CTCSS FAST DETECT ENABLE (Bit 5)	When bit 5 is set to 1, the FAST CTCSS DETECT or FAST CTCSS PREDICTIVE mode is enabled, depending upon the setting of FAST CTCSS MODE (Bit 3 SUB-AUDIO SET-UP Register, $82). When this bit is 0, both FAST CTCSS DETECT and FAST CTCSS PREDICTIVE tone detectors are disabled. See Note 2
(Bits 4, 3, 2, 1 and 0)	Reserved for future use. These bits should be set to 0.

Table 6: Sub-Audio Control Register (Hex Address $80)

Tx Bit 7	Rx Bit 6	Function
0	0	Tx disabled, Rx disabled
0	1	Tx disabled, Rx enabled
1	0	Tx enabled, Rx disabled
1	1	Tx enabled, Rx enabled

Table 7: CTCSS Tx Enable and Decoder Enable

Notes:

1. Bit 7 should be set to 0 if CTCSS FAST DETECT ENABLE (Bit 5 SUB-AUDIO CONTROL Register, $80) is set to 1.
2. Bit 5 should be set to 0 if CTCSS TX ENABLE (Bit 7 SUB-AUDIO CONTROL Register, $80) is set to 1.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.1.3.3 SUB-AUDIO SET-UP Register (Hex address $82)

This register is used to define the CTCSS parameters, as described below:

CTCSS DECODER BANDWIDTH (Bits 7, 6, 5 and 4)	These four bits set the bandwidth of the CTCSS tone decoder according to Table 9
FAST CTCSS MODE (Bit 3)	When CTCSS FAST DETECT ENABLE (Bit 5 SUB-AUDIO CONTROL Register, $80) is 1, this bit selects the FAST CTCSS DETECT or the FAST CTCSS PREDICTIVE mode, according to Table 10.
(Bits 2, 1 and 0)	Reserved for future use. These bits should be set to 0.

Table 8: Sub-Audio Set-up Register (Hex Address $82)

				BANDWIDTH	
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Will Decode**	**Will Not Decode**
1	0	0	0	±1.1%	±2.4%
1	0	0	1	±1.3%	±2.7%
1	0	1	0	±1.6%	±2.9%
1	0	1	1	±1.8%	±3.2%
1	1	0	0	±2.0%	±3.5%
1	1	0	1	±2.2%	±3.7%
1	1	1	0	±2.5%	±4.0%
1	1	1	1	±2.7%	±4.2%

Table 9: CTCSS Decoder Bandwidth

DETECT/PREDICTIVE Bit 3	FUNCTION
0	DETECT mode
1	PREDICTIVE mode

If the CTCSS FAST DETECT ENABLE bit is 0 then both modes are deselected.

Table 10: Fast CTCSS Mode

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.1.3.4 GENERAL CONTROL Register (Hex address $88)

This register is used to control the functions of the device as described below

BPF ENABLE (Bit 7)	When this bit is 1 the audio band-pass filter is enabled. When this bit is 0 the audio band-pass filter is disabled (powersaved).
BPF UN-MUTE (Bit 6)	When this bit is 1 the audio band-pass filter output is switched to the RX AUDIO OUT pin. When this bit is 0 the output of the filter is disconnected from RX AUDIO OUT, which is then in a high impedance state. This control, along with BPF ENABLE, allows the filter to power up and settle internally before switching the output on, to avoid clicks when coming out of powersave.
BPF 6dB PAD (Bit 5)	When this bit is 1 a 6dB attenuator is inserted into the output of the audio band-pass filter. When this bit is 0 the output of the audio band-pass filter is not attenuated.
(Bits 4, 3 and 2)	Reserved for future use. These bits should be set to 0.
TIMER ENABLE (Bit 1)	When this bit goes to a 1 the general purpose timer is restarted and its internal register is re-loaded from the value specified in the GENERAL PURPOSE TIMER Register (Hex address $8B). It will then count down from the count held in its internal register. When this bit is 0 the count down is disabled and the last pre-programmed value is retained in the timer's internal register.
TIMER RE-CYCLE (Bit 0)	When this bit is 1 the general purpose timer will re-load its internal register from the value specified in the GENERAL PURPOSE TIMER Register (Hex Address $8B) when the count in the internal register reaches zero (i.e. the timeout has expired). It then restarts the count down, so that the timer continuously cycles. When this bit is 0 the general purpose timer will stop when the count in the internal register reaches zero (i.e. the timeout has expired). The timer can only be restarted by reloading a value into the GENERAL PURPOSE TIMER Register (Hex address $8B). If this bit is switched from 1 to 0 while the timer is enabled then the timer will complete the present count before stopping.

Table 11: General Control Register (Hex Address $88)

4.1.3.5 GENERAL PURPOSE TIMER (GPT) Register (Hex address $8B)

This register is used to preset the value of a countdown timer. Once a binary value has been loaded into this register, it will be automatically transferred to an internal register within the timer. This internal register is then decremented at each count interval (0.95ms) until it reaches zero. On reaching zero, the GPT IRQ FLAG in the IRQ FLAG Register (Hex address $8F) is set to 1. An interrupt is generated on the $\overline{IRQ}$ pin if the GPT IRQ MASK in the IRQ MASK Register (Hex address $8E) is 1 otherwise the GPT IRQ FLAG remains set to 1 and no interrupt is generated.

When the internal register has reached a count of zero, the action of the timer depends on the setting of the TIMER RE-CYCLE bit in the GENERAL CONTROL Register (Hex address $88). If the TIMER RE-CYCLE bit is 1 then the timer will re-load the countdown value from the GENERAL PURPOSE TIMER Register and restart the countdown from this value. If the TIME RE-CYCLE bit is 0 then the timer will stop and no further action or timer interrupts will take place until the GENERAL PURPOSE TIMER Register is re-loaded. Loading the GENERAL PURPOSE TIMER with 0 will cause the timer circuitry to be disabled (i.e. powersaved).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.1.3.6 IRQ MASK Register (Hex address $8E)

This register is used to control the interrupts (IRQs) as described below:

(Bits 7, 5, 4, 1 and 0)	Reserved for future use. These bits should be set to 0.
GPT IRQ MASK (Bit 6)	When bit 6 is set to 1 it enables an interrupt that occurs when GPT IRQ FLAG (Bit 6, IRQ FLAG Register, $8F) changes from 0 to 1. When this bit is 0 the interrupt is masked.
CTCSS IRQ MASK (Bit 3)	When bit is set to 1 it enables an interrupt that occurs when CTCSS IRQ FLAG (Bit 3, IRQ FLAG Register, $8F) changes from 0 to 1. When this bit is 0 the interrupt is masked.
CTCSS FAST IRQ MASK (Bit 2)	When this bit is set to 1 it enables an interrupt that occurs when CTCSS FAST IRQ FLAG (Bit 2, IRQ FLAG Register, $8F) changes from 0 to 1. When this bit is 0 the interrupt is masked.

Table 12: IRQ MASK Register (Hex address $8E)

4.1.3.7 CTCSS TX/FAST RX FREQUENCY Register (Hex address $83)

This is a 16-bit register. Byte (1) is sent first. When the CTCSS fast detector is enabled, bits 0 - 12 defines the receive frequency the fast predictive detector is looking for, according to the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{16 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When the CTCSS transmitter is enabled, bits 0 - 12 control the frequency of the transmitted CTCSS tones, according to the formula above.

When the fast detector and the transmitter are both enabled, bits 0-12 define the receive frequency which the fast predictive detector is looking for and the frequency of the transmitted tone according to the formula above: (i.e. Tx tone = predictive tone).

When Bit 7 (in the first 8 bits) is set to 1, the tone output is set at V_{BIAS} or NOTONE without regard to the number (A) programmed. When Bit 7 is 0 the programmed tone is set on the output. Programming the bits 0 - 12 to 0 puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the Tx and the FAST DETECT.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.1.3.8 CTCSS RX PROGRAM Register (Hex address $84)

This is a 16-bit register. Byte (1) is sent first. Byte 1 and Byte 2 are used to program the center frequencies of up to 15 tones in the sub-audio band that will be decoded by the receiver.

Each tone is identified by its address in bits 7, 6, 5 and 4 of byte (1). The remaining 12 bits contain the data representing the tone frequency according to the formula below. If a tone is not required the 12 bits should be set to zero.

Byte 1								Byte 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	<---------- N ---------->				<---------- R ---------->							
0	0	0	1												
0	0	1	0												
0	0	1	1												
0	1	0	0												
0	1	0	1	N is the binary representation of the				R is the nearest 6-bit binary							
0	1	1	0	following decimal number (n):				representation of (r), where:							
0	1	1	1												
1	0	0	0	$n = INT(948982 \times f_{TONE} / f_{XTAL})$				$r = \{[237245/f_{XTAL}] - [n/(4 \times f_{TONE})]\} \times 8400$							
1	0	0	1												
1	0	1	0												
1	0	1	1												
1	1	0	0												
1	1	0	1												
1	1	1	0												

Table 13: CTCSS RX PROGRAM Register (Hex address $84)

Example: To program 100Hz when using the recommended 4.032MHz Xtal.

$$n = INT(948982 \times 100 / 4.032 \times 10^6)$$
$$= INT(23.536) = 23$$
$$N = 010111 \text{ (binary)}$$

$$r = \{[237245 / 4.032 \times 10^6] - [23 / (4 \times 100)]\} \times 8400$$
$$= 11.26$$
$$R = 11 \text{ (rounding up if exactly halfway)}$$
$$= 001011 \text{ (binary)}$$

This generates the 12-bit code of 010111001011

The Hex address represented by bits 7, 6, 5 and 4 in byte (1) is used as the code to indicate which tone has been decoded. This code appears in bits 3, 2, 1 and 0 of the SUB-AUDIO STATUS Register (Hex address $81). The 15 programmed tones use Hex addresses $0 - $E.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.1.3.9 AUDIO CONTROL Register (Hex address $8A)

This is a 16-bit register. Byte (1) is sent first. The six least significant bits of the first byte in this register are used to set the attenuation of the Modulator 1 amplifier and the six least significant bits of the second byte in this register are used to set the attenuation of the Modulator 2 amplifier, according to the tables below:

BYTE 1						
5	4	3	2	1	0	Mod. 1 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	12.0dB
1	0	0	0	1	0	11.6dB
1	0	0	0	1	1	11.2dB
1	0	0	1	0	0	10.8dB
1	0	0	1	0	1	10.4dB
1	0	0	1	1	0	10.0dB
1	0	0	1	1	1	9.6dB
1	0	1	0	0	0	9.2dB
1	0	1	0	0	1	8.8dB
1	0	1	0	1	0	8.4dB
1	0	1	0	1	1	8.0dB
1	0	1	1	0	0	7.6dB
1	0	1	1	0	1	7.2dB
1	0	1	1	1	0	6.8dB
1	0	1	1	1	1	6.4dB
1	1	0	0	0	0	6.0dB
1	1	0	0	0	1	5.6dB
1	1	0	0	1	0	5.2dB
1	1	0	0	1	1	4.8dB
1	1	0	1	0	0	4.4dB
1	1	0	1	0	1	4.0dB
1	1	0	1	1	0	3.6dB
1	1	0	1	1	1	3.2dB
1	1	1	0	0	0	2.8dB
1	1	1	0	0	1	2.4dB
1	1	1	0	1	0	2.0dB
1	1	1	0	1	1	1.6dB
1	1	1	1	0	0	1.2dB
1	1	1	1	0	1	0.8dB
1	1	1	1	1	0	0.4dB
1	1	1	1	1	1	0dB

BYTE 2						
5	4	3	2	1	0	Mod. 2 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	6.0dB
1	0	0	0	1	0	5.8dB
1	0	0	0	1	1	5.6dB
1	0	0	1	0	0	5.4dB
1	0	0	1	0	1	5.2dB
1	0	0	1	1	0	5.0dB
1	0	0	1	1	1	4.8dB
1	0	1	0	0	0	4.6dB
1	0	1	0	0	1	4.4dB
1	0	1	0	1	0	4.2dB
1	0	1	0	1	1	4.0dB
1	0	1	1	0	0	3.8dB
1	0	1	1	0	1	3.6dB
1	0	1	1	1	0	3.4dB
1	0	1	1	1	1	3.2dB
1	1	0	0	0	0	3.0dB
1	1	0	0	0	1	2.8dB
1	1	0	0	1	0	2.6dB
1	1	0	0	1	1	2.4dB
1	1	0	1	0	0	2.2dB
1	1	0	1	0	1	2.0dB
1	1	0	1	1	0	1.8dB
1	1	0	1	1	1	1.6dB
1	1	1	0	0	0	1.4dB
1	1	1	0	0	1	1.2dB
1	1	1	0	1	0	1.0dB
1	1	1	0	1	1	0.8dB
1	1	1	1	0	0	0.6dB
1	1	1	1	0	1	0.4dB
1	1	1	1	1	0	0.2dB
1	1	1	1	1	1	0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte)	When this bit is 1 the MOD1 attenuator is enabled. When this bit is 0 the MOD1 attenuator is disabled (i.e. powersaved).
MOD2 ENABLE (Bit 5, second byte)	When this bit is 1 the MOD2 attenuator and the SUMMER AMP are enabled. When this bit is 0 they are both disabled (i.e. powersaved).
(Bits 7 and 6, first and second bytes)	Reserved for future use. These should be set to 0

Table 14: AUDIO CONTROL Register (Hex address $8A)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.1.4 8-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
						CTCSS RX TONE			
$81	SUB-AUDIO STATUS	0	CTCSS FAST TONE	0	TONE DECODE	MSB BIT 3	BIT 2	BIT 1	LSB BIT 0
$8F	IRQ FLAG	0	GP TIMER IRQ FLAG	0	0	CTCSS IRQ FLAG	CTCSS FAST IRQ FLAG	0	0

4.1.5 Read Only Register Description

4.1.5.1 SUB-AUDIO STATUS Register (Hex address $81)

This register is used to indicate the status of the device as described below:

(Bit 7)	Reserved for future use. This will be set to 0 and should be ignored by user's software.
CTCSS FAST TONE (Bit 6)	When Bit 5 in the SUB-AUDIO CONTROL Register and Bit 3 in the SUB-AUDIO SET-UP Register are set to enable FAST CTCSS DETECT mode, this bit will be set to 1 if a periodic tone is detected. If no periodic tone is detected this bit will be set to 0. When Bit 5 in the SUB-AUDIO CONTROL Register and Bit 3 in the SUB-AUDIO SET-UP Register are set to enable FAST CTCSS PREDICTIVE mode, this bit will be set to 1 if a periodic tone that matches the frequency programmed in the CTCSS TX/FAST RX Register is detected. If no match is found this bit will be set to 0. When Bit 5 in the SUB-AUDIO CONTROL Register is set to 0 this bit will be a 0.
(Bit 5)	Reserved for future use. This will be set to 0 and should be ignored by the user's software.
TONE DECODE (Bits 4)	This bit indicates the status of the tone decoder. A 1 indicates a tone has been detected (TONE DECODE). A 0 indicates the loss of the tone (NOTONE). TONE DECODE means that a tone has been decoded and its characteristics are defined by the bandwidth (See SUB-AUDIO SET-UP Register bits 7, 6, 5 and 4) and the CTCSS RX TONE number (See SUB-AUDIO STATUS Register bits 3, 2, 1 and 0). When Bit 6 in the SUB-AUDIO CONTROL Register is set to 0 the TONE DECODE bit 4 will be set to 0. Identification of a valid tone which is not in the pre-programmed list of up to 15 tones will cause the decoder to move to the TONE DECODE state with the RX TONE address of 1111 in bits 3, 2, 1 and 0; indicating a valid, but unrecognized, tone. Loss of tone will cause the NOTONE timer to be started. If loss of tone continues for the duration of the time-out period, then the decoder will move to NOTONE state and the identification of pre-programmed tones will start again.
CTCSS RX TONE (Bits 3, 2, 1 and 0)	These four bits hold a Hex number from $0 to $F. Numbers $0 to $E represent the address of the CTCSS tone decoded according to the tones programmed in the CTCSS RX PROGRAM Register, $84. The Hex number $F indicates the presence of any tone that is not described by CTCSS DECODER BANDWIDTH (Bits 7, 6, 5 and 4, SUB-AUDIO SET-UP Register, $82) and CTCSS FREQUENCY (Bits 11 - 0, CTCSS RX PROGRAM Register, $84).

Table 15: SUB-AUDIO STATUS Register (Hex address $81)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.1.5.2 IRQ FLAG Register (Hex address $8F)

This register is used to indicate when the device requires attention as indicated below.

(Bits 7, 5, 4, 1 and 0)	Reserved for future use. These will be set to 0 and should be ignored by user's software.
GPT IRQ FLAG (Bit 6)	When the general purpose timer has reached zero in its internal register, this bit will be set to 1 to indicate the timeout has expired. This bit is cleared to 0 by a read of the IRQ FLAG Register (Hex address $8F).
CTCSS IRQ FLAG (Bit 3)	When CTCSS RX DECODE (Bit 4, SUB-AUDIO STATUS Register, $81) changes state this bit will be set to 1. This bit is cleared to 0 by a read of the IRQ FLAG Register (Hex address $8F).
CTCSS FAST IRQ FLAG (Bit 2)	When CTCSS FAST TONE (Bit 6, SUB-AUDIO STATUS Register, $81) changes state this bit will be set to 1. This bit is cleared to 0 by a read of the IRQ FLAG Register (Hex address $8F).

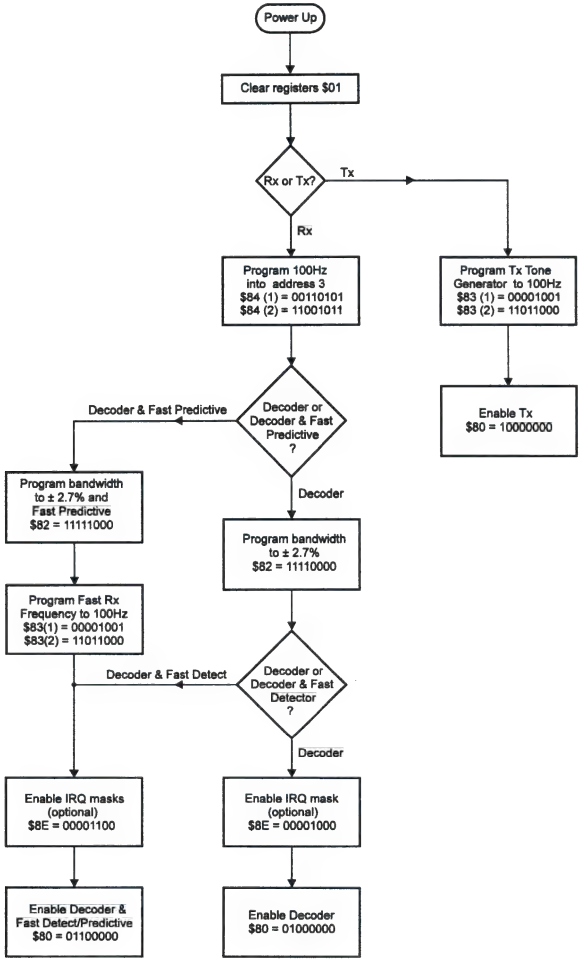
Table 16: IRQ FLAG Register (Hex address $8F)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

The flow chart shows the following modes of operation for the example below:

1. Decode)
2. Decode and Fast Detect) e.g. Address 3 = 100Hz, bandwidth = ±2.7%, interrupt enabled
3. Decode & Fast Predictive)
4. Transmit, e.g. Tx = 100Hz

Note: $8X is the Hex address/command.

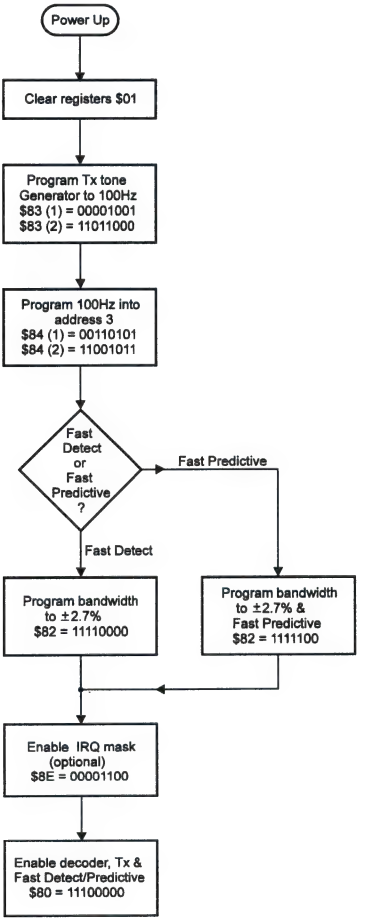

Power Up
Clear registers $01
Rx or Tx?
Tx
Rx
Program 100Hz into address 3 $84 (1) = 00110101 $84 (2) = 11001011
Program Tx Tone Generator to 100Hz $83 (1) = 00001001 $83 (2) = 11011000
Enable Tx $80 = 10000000
Decoder or Decoder & Fast Predictive ?
Decoder & Fast Predictive
Decoder
Program bandwidth to ± 2.7% and Fast Predictive $82 = 11111000
Program bandwidth to ± 2.7% $82 = 11110000
Program Fast Rx Frequency to 100Hz $83(1) = 00001001 $83(2) = 11011000
Decoder or Decoder & Fast Detector ?
Decoder & Fast Detect
Decoder
Enable IRQ masks (optional) $8E = 00001100
Enable IRQ mask (optional) $8E = 00001000
Enable Decoder & Fast Detect/Predictive $80 = 01100000
Enable Decoder $80 = 01000000

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

The flow chart shows the decoder, fast detect/fast predictive and transmitter enabled with the following example.

1. Tx tone generator = 100Hz
2. Decoder programmed with 100Hz in address 3
3. Bandwidth setting = ±2.7%
4. Interrupt enabled

Note: $8X is the Hex address/command.



© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. Application

5.1 General

The MX818 is intended for use in radio systems where sub-audio signaling is required for functions such as trunking control, selective calling or group calling.

The CTCSS fast/predictive detector is useful for the detection of occupied channels indicating either the presence of any sub-audio tone, or range of tones, depending if it is set in fast detect or predictive mode. This will increase the efficiency of scanning and trunking systems, reducing the average time allocated to assessing each channel.

The facility to decode any of up to 15 programmed tones allows the use of tones for various signaling functions such as masking a free channel or identifying sub groups within a user's groups.

Adjustable decoder bandwidths permits certainty and signal to noise performance to be traded when congestion or range, limits the system performance.

5.2 Transmitter

The transmitter is enabled with Bit 7 in the SUB-AUDIO CONTROL register ($80).

The Tx frequency is set using Bit 0 to Bit 12 in the CTCSS TX/FAST RX register ($83) using the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{16 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to 1 the tone output is set at V_{BIAS} or NOTONE without regard to the number (A) programmed. When Bit 7 is 0 the programmed tone is set on the output. Programming the bits 0 to 12 to 0 puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the Tx and the FAST DETECT (Bits 7 and 5 in the SUB-AUDIO CONTROL register $80).

5.3 Receiver (Decode)

The CTCSS Receiver (Decoder) should first be set up according to the desired characteristics. This entails setting the CTCSS decoder bandwidth in the SUB-AUDIO SET-UP register ($82), also programming the center frequencies of the desired tones in the CTCSS RX PROGRAM register ($84). (It can hold up to 15 different tones). Any tone can be in any location. During operation when the device is receiving, the tones are scanned in the sequence of their location, i.e. $0 first and $E last and once a tone is detected the remaining tones are not checked. Therefore if two tones are close enough in frequency for their bandwidths to overlap then the one in the lowest location will be detected.

The CTCSS IRQ MASK in the IRQ MASK register ($8E) should also be set as required.

The CTCSS DECODER ENABLE in the SUB-AUDIO CONTROL register ($80) should then be set to 1. While in the Decode mode the FAST DETECT may be enabled (see below).

When the receiver detects a change in its present state an IRQ will be generated and Bit 3 of the IRQ FLAG register ($8F) will indicate this.

The change that occurred can be read from Bit 4 of the SUB-AUDIO STATUS register ($81) and if a tone is indicated by this bit then the number of that tone can be read from Bits 3, 2, 1 and 0 of the same register.

5.4 Receiver (Fast Detect)

This is used for detecting, in the fastest possible time, that sub-audio tones are present on the Rx channel. Response time is optimized for speed at the expense of frequency resolution.

It is enabled using Bit 5 of the SUB-AUDIO CONTROL register ($80). It has an IRQ which may be unmasked with Bit 2 of the IRQ MASK register ($8E). The FAST CTCSS MODE DETECT/PREDICTIVE Bit 3 in the SUB-AUDIO SET UP register ($82) allows for one of two alternatives in the FAST mode. In DETECT mode it will detect any periodic tone in the sub-audio band and when in PREDICTIVE mode it will detect specific tones determined by the frequency set in the CTCSS TX/FAST RX register ($83) and the fixed PREDICTIVE mode bandwidth. Successful detection is indicated by the CTCSS FAST IRQ FLAG Bit 2 in the IRQ FLAG register ($8F), and the CTCSS FAST TONE Bit 6 in the SUB-AUDIO STATUS register ($81).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.5 General Purpose Timer (GPT)

This may be used in conjunction with the Rx Decoder to form part of the decode algorithm or as a timer for any other purpose. It has an 8-bit value register GENERAL PURPOSE TIMER register ($8B) set in units of 0.95ms, an IRQ FLAG Bit 6 of the IRQ FLAG register ($8F) and an IRQ MASK Bit 6 IRQ MASK register ($8E).

5.6 Tx / Fast Rx Tone Table

The following table lists the commonly used CTCSS tones and the corresponding values for programming the transmitter frequency / fast predictive frequency register (Hex address $83).

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	E	B1	**114.8**	8	93	**186.2**	5	49
69.3	E	34	**118.8**	8	49	**189.9**	5	2F
71.9	D	B1	**123.0**	8	1	**192.8**	5	1B
74.4	D	3B	**127.3**	7	BC	**196.6**	5	2
77.0	C	C9	**131.8**	7	78	**199.5**	4	EF
79.7	C	5A	**136.5**	7	36	**203.5**	4	D6
82.5	B	EF	**141.3**	6	F7	**206.5**	4	C4
85.4	B	87	**146.2**	6	BC	**210.7**	4	AC
88.5	B	1F	**151.4**	6	80	**218.1**	4	83
91.5	A	C2	**156.7**	6	48	**225.7**	4	5D
94.8	A	62	**159.8**	6	29	**229.1**	4	4C
97.4	A	1B	**162.2**	6	12	**233.6**	4	37
100.0	9	D8	**167.9**	5	DD	**241.8**	4	12
103.5	9	83	**173.8**	5	AA	**250.3**	3	EF
107.2	9	2F	**179.9**	5	79	**254.1**	3	E0
110.9	8	E0	**183.5**	5	5D			

Table 17: Tx / Fast Rx Tone Table

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.7 Rx Program Tone Table

The following table lists the commonly used CTCSS tones together with the values for programming the "CTCSS RX PROGRAM" register (Hex address $84).

Note: The values for byte 1 and 2 below apply to tone address 0 only. These values will vary depending on the location they are programmed into.

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	3	D8	**114.8**	6	C0	**186.2**	A	C9
69.3	4	9	**118.8**	6	D1	**189.9**	B	8
71.9	4	1B	**123.0**	7	10	**192.8**	B	44
74.4	4	4E	**127.3**	7	50	**196.6**	B	83
77.0	4	83	**131.8**	7	C0	**199.5**	B	8A
79.7	4	94	**136.5**	8	2	**203.5**	B	C9
82.5	4	CB	**141.3**	8	44	**206.5**	C	6
85.4	5	2	**146.2**	8	86	**210.7**	C	46
88.5	5	14	**151.4**	8	C9	**218.1**	C	C3
91.5	5	4C	**156.7**	9	C	**225.7**	D	41
94.8	5	87	**159.8**	9	48	**229.1**	D	48
97.4	5	94	**162.2**	9	82	**233.6**	D	89
100.0	5	CB	**167.9**	9	C6	**241.8**	E	8
103.5	6	7	**173.8**	A	B	**250.3**	E	88
107.2	6	45	**179.9**	A	84	**254.1**	E	C7
110.9	6	82	**183.5**	A	C2			

Table 18: Rx Program Tone Table

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW / P Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency		4.0315968	4.0324032	MHz

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
Xtal Frequency = 4.032MHz
Audio Level 0dB ref. = 308mVrms at 1kHz
V_{DD} = 3.3V / 5.0V, T_{AMB} = 25°C.
Composite Signal = 308mV_{RMS} at 1kHz + 75mV_{RMS} Noise + 31mV_{RMS} Sub-Audio Signal
Noise Bandwidth = 5kHz Band Limited Gaussian

		Note	Min.	Typ.	Max.	Units
DC Parameters						
I_{DD}						
All Powersaved		1, 2		0.5		mA
FAST DETECT Enabled		1, 2		3.0		mA
Rx Operating		1, 2		3.5		mA
Tx Operating		1, 2		3.0		mA
C-BUS Interface						
Input Logic 1			70%			V_{DD}
Input Logic 0					30%	V_{DD}
Input Leakage Current (Logic 1 or 0)			-1.0		1.0	µA
Input Capacitance					7.5	pF
Output Logic 1 (I_{OH} = 120µA)			90%			V_{DD}
Output Logic 0 (I_{OL} = 360µA)					10%	V_{DD}
Off State Leakage Current (V_{OUT} = V_{DD})		6			10	µA
AC Parameters						
CTCSS Decoder						
Sensitivity	(Pure CTCSS Tone)	5		-26.0		dB
Response Time	(Composite Signal)			140		ms
De-Response Time	(Composite Signal)			145		ms
Frequency Range			60		253	Hz
CTCSS Detector - Fast Detect						
Sensitivity	(Pure CTCSS Tone)	5		-26.0		dB
Response Time	(Composite Signal)			56.0		ms
CTCSS Detector - Fast Predictive						
Sensitivity	(Pure CTCSS Tone)	5		-26.0		dB
Response Time	(Composite Signal)	7		37.0		ms
CTCSS Encoder						
Frequency Range			60		253	Hz
Tone Frequency Resolution					0.3	%
Tone Amplitude Tolerance		1	-1.0	0	1.0	dB
Total Harmonic Distortion		9		2.0		%
Audio Band-Pass Filter						
Passband		8	300		3000	Hz
Passband Gain	(at 1.0kHz)	8		0		dB
Passband Ripple	(wrt gain at 1.0kHz)	8	-2		0.5	dB
Stopband Attenuation		8	33.0			dB
Residual Hum and Noise				-50.0		dBp
Alias Frequency				63		kHz

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

		Note	Min.	Typ.	Max.	Units
Output Impedance						
TX SUB-AUDIO OUT	(Enabled)			2.0		kΩ
RX AUDIO OUT	(Disabled)			500		kΩ
Rx Amp and Summing Amp						
Open Loop Gain	(input = 1mV at 100Hz)			70.0		dB
Unity Gain Bandwidth				5.0		MHz
Input Impedance	(at 100Hz)		10			MΩ
Output Impedance	(Open Loop)			6.0		kΩ
Transmitter Modulator Drives:						
Mod.1 Attenuator						
Attenuation (at 0dB)			-0.2	0	0.2	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)			-1.0		1.0	dB
Output Impedance		3		600		Ω
Input Impedance	(at 100Hz)			15.0		kΩ
Mod.2 Attenuator						
Attenuation (at 0dB)			-0.2	0	0.2	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)			-0.6		0.6	dB
Output Impedance		3		600		Ω
General Purpose Timer						
Timing Period Range			0.95		242.25	ms
Count Interval				1		ms
Xtal/Clock Input						
Pulse Width ('High' or 'Low')		4	40.0			ns
Input Impedance (at 100Hz)			10.0			MΩ
Gain (input = $1mV_{RMS}$ at 100Hz)			20.0			dB

Operating Characteristics Notes:

1. At V_{DD} = 5.0V only. Signal levels or currents are proportional to V_{DD}.
2. Not including any current drawn from the device by external circuitry.
3. Small signal impedance.
4. Timing for an external input to the XTAL/CLOCK pin.
5. With input gain components set as recommended in Figure 2.
6. $\overline{IRQ}$ pin.
7. From one tone to another tone.
8. See filter response (Figure 3).
9. Measured at MOD1 or MOD2 output.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

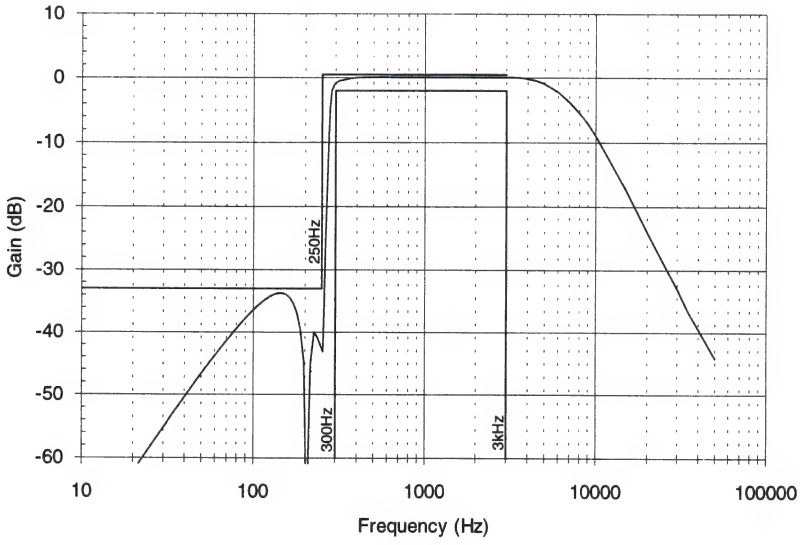


Figure 3: Audio Band-Pass Filter Frequency Response

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.1.4 Timing Diagrams

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, V_{DD} = 5.0V, T_{AMB} = 25°C.

Parameter		Min.	Typ.	Max.	Units
t_{CSE}	CS-Enable to Clock-High	2.0			µs
t_{CSH}	Last Clock-High to CS-High	4.0			µs
t_{HIZ}	CS-High to Reply Output 3-state			2.0	µs
t_{CSOFF}	CS-High Time between transactions	2.0			µs
t_{NXT}	Inter-Byte Time	4.0			µs
t_{CK}	Clock-Cycle time	2.0			µs

Timing Diagrams Notes

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

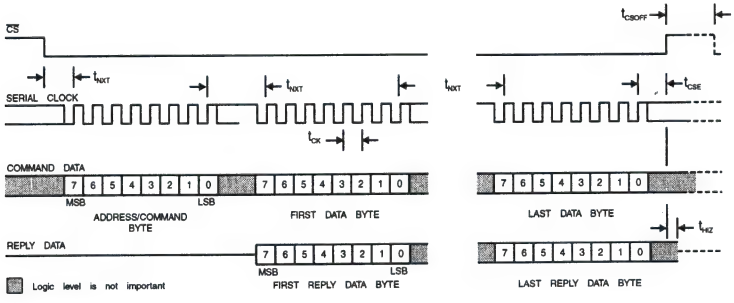
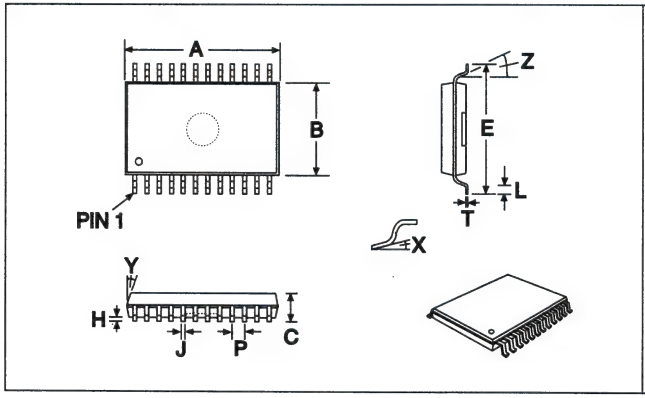


Figure 4: C-BUS Timing

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.2 Packaging

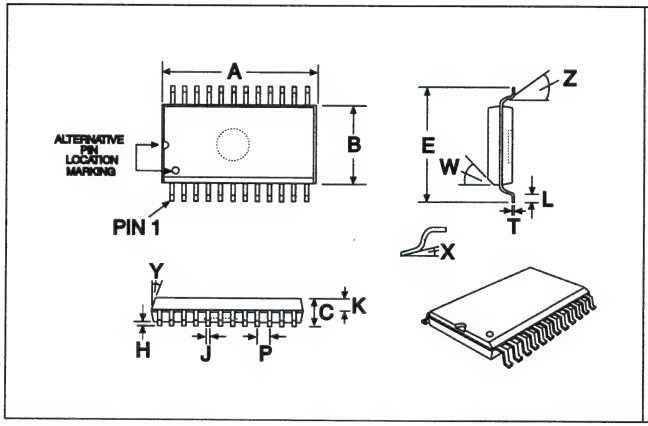


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 24-pin SSOP Mechanical Outline: *Order as part no. MX818DS*



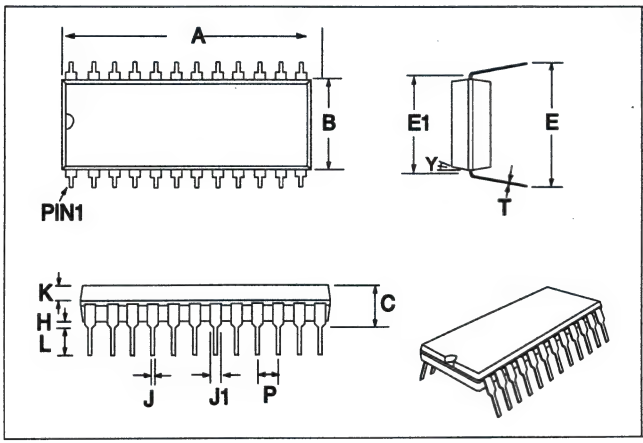
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin SOIC Mechanical Outline: *Order as part no. MX818DW*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 24-pin PDIP Mechanical Outline: *Order as part no. MX818P*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480163.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX828 CTCSS/DCS/SelCall Processor

ADVANCE INFORMATION

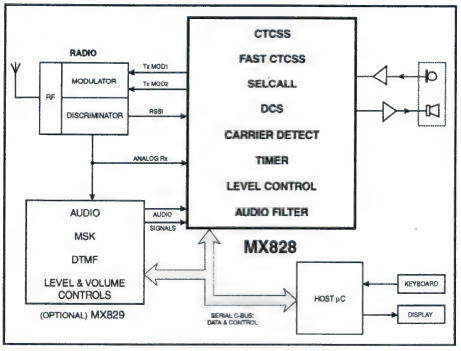
Shipping JULY 1997

Features

- **Fast CTCSS Detection**
- **Full 23/24 Bit DCS Codec**
- **SelCall Codec**
- **Predictive Tone Detection**
- **Low Power 3.3V/5.0V Operation**
- **Variable Gain Audio Filter**
- **Programmable:**
  - **Tone Decoder**
  - **Tone Encoder**
  - **Modulator Drivers**
  - **Comparator for RSSI**
- **Pin compatible with reduced function MX818**
- **Full control via 4-Wire Serial Interface**

Applications

- **Radio Systems Requiring Sub-Audible Signaling**
  - **Trunking Control**
  - **Selective Calling**
  - **Group Calling**
- **Increased Efficiency**
  - **Scanning Systems**
  - **Trunking Systems**



The MX828 is a low power SelCall, CTCSS, and DCS signal processor designed for use in the latest generation of LMR (Land Mobile Radio) equipment where sub-audible signaling is required for functions such as Trunking Control, Selective Calling, and Group Calling applications. The MX828 is full duplex and offers many advanced features to assist in the design of new Sub-Audible and in-band based systems. These include: a programmable tone decoder which may be set to respond to between 1 and 15 CTCSS or SelCall tones with minimum software intervention, a Fast/Predictive CTCSS detector that can respond to a single programmed tone in less than 60ms or provide an output if CTCSS tone is present at the detector input, two high resolution tone encoders that accurately generate CTCSS or SelCall tones, and a full 23/24 bit DCS encoder and decoder. The MX828 also provides a general purpose timer, a comparator with a programmable threshold, and a summing amplifier with two adjustable gain blocks to facilitate design integration and reduce part count.

The MX828 may be used with a 3.0 to 5.5 volt supply and is available in the following packages: 24-pin SSOP (MX828DS), 24-pin SOIC (MX828DW), and 24-pin PDIP (MX828P).

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480161.001

CONTENTS

Section **Page**

1. Block Diagram **3-109**

2. Signal List **3-110**

3. External Components **3-111**

4. General Description **3-112**
4.1 Software Description 3-113
4.2 8-bit Write Only Registers 3-114
4.3 16-bit Write Only Registers 3-115
4.4 Write Only Register Description 3-116
4.5 8-bit Read Only Registers 3-122
4.6 Read Only Register Description 3-122

5. Application Notes **3-126**
5.1 General 3-126
5.2 Transmitters 3-126
5.3 Receiver (CTCSS/SelCall Decoder) 3-127
5.4 Receiver (CTCSS Fast/Predictive Detector) 3-127
5.5 Receiver (DCS Decoder) 3-127
5.6 General Purpose Timer (GPT) 3-127
5.7 Full Duplex Modes 3-127

6. Performance Specification **3-132**
6.1 Electrical Performance 3-132
6.2 Timing Diagrams 3-137
6.3 Packaging 3-138

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1. Block Diagram

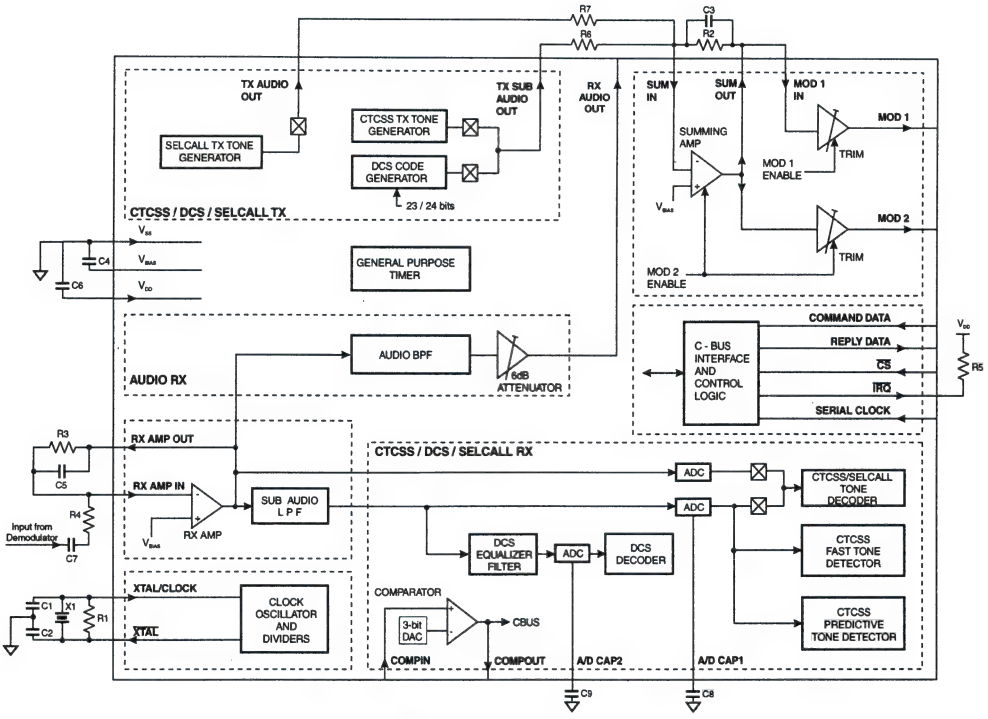


Figure 1: Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. Signal List

Pin No.	Name	Type	Description
1	$\overline{XTAL}$	output	The inverted output of the on-chip oscillator.
2	XTAL/CLOCK	input	The input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	input	The "C-BUS" serial clock input. This clock, produced by the µC, is used for timing transfer of commands and data to and from the device. (Figure 4).
4	COMMAND DATA	input	The "C-BUS" serial data input from the µC. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the SERIAL CLOCK. (Figure 4).
5	REPLY DATA	output	The "C-BUS" serial data output to the µC. The transmission of REPLY DATA bytes is synchronized to the SERIAL CLOCK under the control of the $\overline{CS}$ input. This 3-state output is held at high impedance when not sending data to the µC. (Figure 4).
6	$\overline{CS}$	input	The "C-BUS" data loading control function: this input is provided by the µC. Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal (Figure 4).
7	$\overline{IRQ}$	output	This output indicates an interrupt condition to the µC by going to a logic "0". This is a "wire-ORable" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pullup resistor is required. The conditions that cause interrupts are indicated in the IRQ FLAG register and are effective if not masked out by a corresponding bit in the IRQ MASK register.
8	COMPOUT	output	The output of the comparator.
9	COMPIN	input	The input to the comparator.
10	A/D CAP 1	output	An internal reference voltage for the CTCSS A/D. Bypassed to V_{SS} with an external capacitor.
11	A/D CAP 2	output	An internal reference voltage for the DCS A/D. Bypassed to V_{SS} with an external capacitor.
12	V_{SS}	Power	Negative supply (ground).
13	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed by a capacitor mounted close to the device pins.
14	RX AMP IN	input	The inverting input to the Rx input amplifier.
15	RX AMP OUT	output	Output of the Rx input amplifier
16	RX AUDIO OUT	output	Output of the Rx audio filter section.
17	TX AUDIO OUT	output	Output of the SelCall tone generator.
18	SUM IN	input	Input to the audio summing amplifier.
19	SUM OUT	output	Output of the audio summing amplifier.
20	MOD1 IN	input	Input to MOD1 audio gain control.
21	TX SUB AUDIO OUT	output	Output of the CTCSS or DCS Tx tone generator.
22	MOD1	output	Output of MOD1 audio gain control.
23	MOD2	output	Output of MOD2 audio gain control.
24	V_{DD}	Power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

Table 1: Signal List

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components

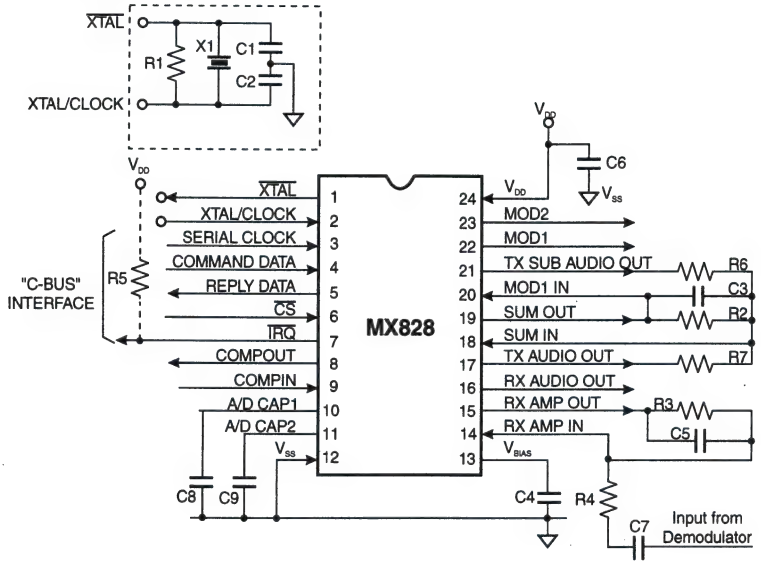


Figure 2: Recommended External Components

R1		1MΩ	±5%	C3		100pF	±20%
R2		100kΩ	±10%	C4		0.1µF	±20%
R3		100kΩ	±10%	C5		100pF	±20%
R4	Note 2		±10%	C6		0.1µF	±20%
R5		22kΩ	±10%	C7	Note 2		±20%
R6	Note 1		±10%	C8		0.1µF	±20%
R7	Note 1		±10%	C9		TBA	±20%
C1		22pF	±20%				
C2		22pF	±20%	X1	Note 3	4.032MHz	±100ppm

Table 2: External Components

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

External Components Notes:

1. R2, R6, R7 and C3 form the gain components for the Summing Amplifier. R6 and R7 should be chosen as required from the system specification, using the following formula:
   Tx Sub Audio Gain $= -\frac{R2}{R6}$ Tx Audio Gain $= -\frac{R2}{R7}$
2. R3, R4, C5 and C7 form the gain components for the Rx Input Amplifier. R4 should be chosen as required by the signal level, using the following formula:
   Gain $= -\frac{R3}{R4}$
   C7 x R4 should be chosen so as not to compromise the low frequency performance of this product.
3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

The MX828 is a signaling encoder/decoder for use in land mobile radio equipment, see Figure 1. The transmitter section of the MX828 has independently controllable tone generators for sub-audio (CTCSS) and inband (SelCall) signaling. Also featured is a DCS code generator, which may be used in place of the CTCSS tone generator.

The receiver section of the MX828 has a fast/predictive CTCSS tone detector which operates in parallel with a DCS decoder and a CTCSS/SelCall tone decoder. The latter is switchable to perform either CTCSS or SelCall tone decoding of a user-programmable set of up to 15 tones. In the CTCSS mode it performs a more accurate (but slower) analysis of the tones detected by the fast/predictive CTCSS tone detector, which is a single detector that is switchable to provide either a fast response to any CTCSS tone (FAST DETECT mode) or a fast response to a single user-programmed CTCSS tone (PREDICTIVE mode).

Both the DCS transmit and receive bit rates are fixed at 134.4bps.

Other functions on the MX828 are a comparator with programmable threshold level, a general purpose timer and a summing amplifier with two adjustable gain blocks, which may be used for two point modulation, for example. All MX828 functions are controlled by an external µC over the "C-BUS" interface, a serial interface designed to reduce interference levels in radio equipment.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.1 Software Description

4.1.1 Command Summary

The following table contains a brief description of all valid Commands. Details follow below.

				DATA BYTE(S)	
REGISTER NAME	**SECTION**	**HEX ADDRESS COMMAND**	**READ / WRITE**	**BYTE 1**	**BYTE 2**
General Reset	4.4.1	$01	W	none	none
Sub-Audio Control	4.4.2	$80	W	Refer to Bit Description	none
SelCall Sub-Audio Status	4.5 4.6.1	$81	R	Refer to Bit Description	none
Sub-Audio Set-Up	4.4.3	$82	W	Refer to Bit Description	none
CTCSS TX/ Fast RX Frequency	4.4.10	$83	W	Specify Tx or Fast Rx Frequency per command $80 & $83 Bit descriptions	
RX Tone Program	4.4.11	$84	W	1 of 15 possible Registers Select & Decode Frequencies	
DCS Code	4.4.4	$85	W	Byte 3 of 3	none
DCS Code	4.4.5	$86	W	Byte 2 of 3	none
DCS Code	4.4.6	$87	W	Byte 1 of 3	none
General Control	4.4.7	$88	W	Refer to Bit Description	none
Audio Control	4.4.12	$8A	W	Mod 1 Attenuation	Mod 2 Attenuation
General Purpose Timer	4.4.8	$8B	W	Refer to Bit Description	none
SelCall TX	4.4.13 4.4.2 4.4.3	$8D	W	Specify TX SelCall Frequencies	
IRQ Mask	4.4.9	$8E	W	Refer to Bit Description	none
IRQ Flag	4.5 4.6.2	$8F	R	Refer to Bit Description	none

Table 3: Command Summary

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.1.2 Address/Commands

Instructions and data are transferred, via "C-BUS", in accordance with the timing information given in Figure 4.

Instruction and data transactions to and from the MX828 consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction or data (1 or 2 bytes) or

(ii) a status or Rx data reply (1 byte)

4.2 8-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	GENERAL RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$80	SIGNALLING CONTROL	SUBAUDIO TX ENABLE	TONE DECODER ENABLE	FAST DETECT ENABLE	0	0	SELCALL TX ENABLE	0	DCS RX ENABLE
$82	SIGNALLING SET-UP	TONE DECODER BANDWIDTH MSB BIT 3	BIT 2	BIT 1	LSB BIT 0	FAST CTCSS MODE DETECT/ PREDICTIVE	TONE DECODER MODE	SUBAUDIO TX MODE	DCS 23/24
$85	DCS BYTE 3	DCS BYTE 3 OPTIONAL MSB BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
$86	DCS BYTE 2	DCS BYTE 2 BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
$87	DCS BYTE 1	DCS BYTE 1 BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$88	GENERAL CONTROL	BPF ENABLE	BPF UN-MUTE	BPF 6dB PAD	MSB DAC BIT 2	DAC BIT 1	LSB DAC BIT 0	GP TIMER ENABLE	GP TIMER RE-CYCLE
$8B	GENERAL PURPOSE TIMER	GENERAL PURPOSE TIMER MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8E	IRQ MASK	0	GP TIMER IRQ MASK	COMP 0 to 1 IRQ MASK	COMP 1 to 0 IRQ MASK	TONE IRQ MASK	CTCSS FAST IRQ MASK	0	DCS IRQ MASK
$9C	*Reserved for later use*								

Table 4: 8-bit Write Only Registers

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.3 16-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$83	CTCSS TX/ FAST RX FREQUENCY (1)	CTCSS (TX) NOTONE	0	0	CTCSS TX/FAST RX FREQUENCY MSB BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
	CTCSS TX/ FAST RX FREQUENCY (2)	CTCSS TX/FAST RX FREQUENCY BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$84	RX TONE PROGRAM (1)	TONE ADDRESS MSB BIT 3	BIT 2	BIT 1	LSB BIT 0	TONE FREQUENCY MSB BIT 11	BIT 10	BIT 9	BIT 8
	RX TONE PROGRAM (2)	TONE FREQUENCY BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8A	AUDIO CONTROL (1)	0	0	MOD 1 ENABLE	MOD 1 MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
	AUDIO CONTROL (2)	0	0	MOD 2 ENABLE	MOD 2 MSB BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
$8D	SELCALL TX (1)	SELCALL NOTONE	0	0	SELCALL TX TONE MSB BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
	SELCALL TX (2)	SELCALL TX TONE BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0

Table 5: 16-bit Write Only Registers

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.4 Write Only Register Description

4.4.1 GENERAL RESET (Hex address $01)

The reset command has no data attached to it. It sets the device registers into the specific (all powersaved) states as listed below:

REGISTER NAME	HEX ADDRESS	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 D0)
SIGNALING CONTROL	$80	0	0	0	0	0	0	0	0
SELCALL & SUB-AUDIO STATUS	$81	0	0	0	0	X	X	X	X
SIGNALING SET-UP	$82	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX FREQUENCY (1)	$83	0	0	0	0	0	0	0	0
CTCSS TX / FAST RX FREQUENCY (2)		0	0	0	0	0	0	0	0
RX TONE PROGRAM (1)	$84	0	0	0	0	0	0	0	0
RX TONE PROGRAM (2)		0	0	0	0	0	0	0	0
DCS BYTE 3	$85	0	0	0	0	0	0	0	0
DCS BYTE 2	$86	0	0	0	0	0	0	0	0
DCS BYTE 1	$87	0	0	0	0	0	0	0	0
GENERAL CONTROL	$88	0	0	0	0	0	0	0	0
AUDIO CONTROL (1)	$8A	0	0	0	0	0	0	0	0
AUDIO CONTROL (2)		0	0	0	0	0	0	0	0
GENERAL PURPOSE TIMER	$8B	0	0	0	0	0	0	0	0
SELCALL TX (1)	$8D	0	0	0	0	0	0	0	0
SELCALL TX (2)		0	0	0	0	0	0	0	0
IRQ MASK	$8E	0	0	0	0	0	0	0	0
IRQ FLAG	$8F	0	0	0	0	0	0	0	0

X = undefined

Table 6: GENERAL RESET (Hex address $01)

4.4.2 SIGNALING CONTROL Register (Hex address $80)

This register is used to control the functions of the device as described below:

SUBAUDIO TX ENABLE and TONE DECODER ENABLE (Bits 7 and 6)	These two bits enable and disable the CTCSS/SelCall tone decoder (Rx) or CTCSS/DCS subaudio transmitter (Tx) according to Table 8. Bit 7 should be set to "0" if the CTCSS FAST DETECT ENABLE (Bit 5 SIGNALING CONTROL Register, $80) is set to "1". The subaudio Tx type will depend on the state of the SUBAUDIO TX MODE (Bit 1 SIGNALING SET-UP Register $82).
CTCSS FAST DETECT ENABLE (Bit 5)	When this bit is "1", the FAST CTCSS DETECT or FAST CTCSS PREDICTIVE mode is enabled, depending upon the setting of FAST CTCSS MODE (Bit 3 SIGNALING SET-UP Register, $82). When this bit is "0", both FAST CTCSS DETECT and FAST CTCSS PREDICTIVE tone detectors are disabled. This bit should be set to "0" if SUBAUDIO TX ENABLE (Bit 7 SIGNALING CONTROL Register, $80) is set to "1".
SELCALL TX ENABLE (Bit 2)	When this bit is "1" the SelCall transmitter is enabled. When this bit is "0" the SelCall transmitter is disabled and powersaved.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

DCS RX ENABLE (Bit 0)	When this bit is "1", the DCS decoder is enabled. When this bit is "0" the DCS decoder is disabled. The DCS decoder and the subaudio (CTCSS or DCS) transmitter should not be enabled at the same time.
(Bits 4, 3, and 1)	Reserved for future use. These bits should be set to "0".

Table 7: SIGNALING CONTROL Register (Hex address $80)

Tx (Bit 7)	Rx (Bit 6)	Function
0	0	Tx disabled, Rx disabled
0	1	Tx disabled, Rx enabled
1	0	Tx enabled, Rx disabled
1	1	Tx Enabled, Rx Enabled

Table 8: SUBAUDIO TX ENABLE and TONE DECODER ENABLE

4.4.3 SIGNALING SET-UP Register (Hex address $82)

This register is used to define the signaling parameters, as described below:

TONE DECODER BANDWIDTH (Bits 7, 6, 5 and 4)	These four bits set the bandwidth of the CTCSS/SelCall tone decoder according to the table below:
FAST CTCSS MODE (Bit 3)	When CTCSS FAST DETECT ENABLE (Bit 5 SIGNALING CONTROL Register, $80) is "1", this bit selects the FAST CTCSS DETECT or the FAST CTCSS PREDICTIVE mode, according to the table below: If the CTCSS FAST DETECT ENABLE bit is "0" then both modes are deselected.
TONE DECODER MODE (Bit 2)	When this bit is "1" the CTCSS/SelCall tone decoder is set to detect inband (SelCall) tones. When this bit is "0" the tone decoder is set to detect subaudio (CTCSS) tones.
SUBAUDIO TX MODE (Bit 1)	When this bit is "1" the subaudio transmitter will be set to transmit DCS signals, if enabled. When this bit is "0" the subaudio transmitter will be set to transmit CTCSS signals, if enabled.
DCS 23/24 (Bit 0)	When this bit is "1" the DCS transmitter and decoder are configured for a 23-bit code. When this bit is "0" they are configured for a 24-bit code.

Table 9: SIGNALING SET-UP Register (Hex address $82)

					BANDWIDTH	
	Bit 7	Bit 6	Bit 5	Bit 4	Will Decode	Will Not Decode
Recommended for CTCSS	1	0	0	0	±1.1%	±2.4%
Recommended for CCIR	1	0	0	1	±1.3%	±2.7%
	1	0	1	0	±1.6%	±2.9%
	1	0	1	1	±1.8%	±3.2%
	1	1	0	0	±2.0%	±3.5%
	1	1	0	1	±2.2%	±3.7%
Recommended for ZVEI	1	1	1	0	±2.5%	±4.0%
	1	1	1	1	±2.7%	±4.2%

Table 10: TONE DECODER BANDWIDTH

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

DETECT/PREDICTIVE Bit 3	Function
0	DETECT mode
1	PREDICTIVE mode

Table 11: FAST CTCSS MODE

4.4.4 DCS BYTE 3 Register (Hex address $85)

4.4.5 DCS BYTE 2 Register (Hex address $86)

4.4.6 DCS BYTE 1 Register (Hex address $87)

These three bytes set the code that is transmitted or received in the DCS mode. The LSB bit "0" of the DCS BYTE 1 is transmitted first and the last bit is the MSB bit 23 of DCS BYTE 3 in the 24-bit mode or bit 22 in the 23-bit mode. See Table 23 or refer to the latest version of ANSI/TIA/EIA - 603 specification and programming documentation for DCS standard 23-bit codes.

4.4.7 GENERAL CONTROL Register (Hex address $88)

This register is used to control the functions of the device as described below:

BPF ENABLE (Bit 7)	When this bit is "1" the audio band-pass filter is enabled. When this bit is "0" the audio band-pass filter is disabled (powersaved).
BPF UN-MUTE (Bit 6)	When this bit is "1" the audio band-pass filter output is switched to the RX AUDIO OUT pin. When this bit is "0" the output of the filter is disconnected from RX AUDIO OUT, which is then in a high impedance state. This control, along with BPF ENABLE, allows the filter to power up and settle internally before switching the output on, to avoid clicks when coming out of powersave.
BPF 6dB PAD (Bit 5)	When this bit is "1" a 6dB attenuator is inserted into the output of the audio band-pass filter. When this bit is "0" the output of the audio band-pass filter is not attenuated.
DAC (Bits 4, 3 and 2)	These three bits set the level of the digital to analogue converter that feeds the negative input of the comparator. The DAC can be set to one of eight levels equally spaced between V_{SS} and V_{BIAS}, not including V_{SS}, but including V_{BIAS}, i.e. with a 5V supply, the lowest level would be 312.5mV set by "000" in bits 2, 3 and 4 and the highest level would be 2.5V set by "111" in bits 2, 3 and 4.
TIMER ENABLE (Bit 1)	When this bit goes to a "1" the general purpose timer is restarted and its internal register is re-loaded from the value specified in the GENERAL PURPOSE TIMER Register (Hex address $8B). It will then count down from the count held in its internal register. When this bit is "0" the count down is disabled and the last pre-programmed value is retained in the timer's internal register.
TIMER RE-CYCLE (Bit 0)	When this bit is "1" the general purpose timer will re-load its internal register from the value specified in the GENERAL PURPOSE TIMER Register (Hex Address $8B) when the count in the internal register reaches zero (i.e. the timeout has expired). It then restarts the count down, so that the timer continuously cycles. When this bit is "0" the general purpose timer will stop when the count in the internal register reaches zero (i.e. the timeout has expired). The timer can only be restarted by reloading a value into the GENERAL PURPOSE TIMER Register (Hex address $8B). If this bit is switched from "1" to "0" while the timer is enabled then the timer will complete the present count before stopping.

Table 12: GENERAL CONTROL Register (Hex address $88)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.4.8 GENERAL PURPOSE TIMER (GPT) Register (Hex address $8B)

This register is used to preset the value of a countdown timer. Once a binary value has been loaded into this register, it will be automatically transferred to an internal register within the timer. This internal register is then decremented at each count interval (1ms) until it reaches zero. On reaching zero, the GPT IRQ FLAG in the IRQ FLAG Register (Hex address $8F) is set to "1". An interrupt is generated on the IRQN pin if the GPT IRQ MASK in the IRQ MASK Register (Hex address $8E) is "1" otherwise the GPT IRQ FLAG remains set to "1" and no interrupt is generated.

When the internal register has reached a count of zero, the action of the timer depends on the setting of the TIMER RE-CYCLE bit in the GENERAL CONTROL Register (Hex address $88). If the TIMER RE-CYCLE bit is "1" then the timer will re-load the countdown value from the GENERAL PURPOSE TIMER Register and restart the countdown from this value. If the TIME RE-CYCLE bit is "0" then the timer will stop and no further action or timer interrupts will take place until the GENERAL PURPOSE TIMER Register is re-loaded. Loading the GENERAL PURPOSE TIMER with "0" will cause the timer circuitry to be disabled (i.e. powersaved).

4.4.9 IRQ MASK Register (Hex address $8E)

This register is used to control the interrupts (IRQs) as described below:

(Bits 7 and 1)	Reserved for future use. These should be set to "0".
GPT IRQ MASK (Bit 6)	When this bit is set to "1" it enables an interrupt that occurs when GPT IRQ FLAG (Bit 6, IRQ FLAG Register, $8F) changes from "0" to "1". When this bit is "0" the interrupt is masked.
COMP 0 to 1 IRQ MASK (Bit 5)	When this bit is set to "1" it enables an interrupt that occurs when the comparator output goes from "0" to "1". When this bit is set to "0" the interrupt is masked.
COMP 0 to 1 IRQ MASK (Bit 4)	When this bit is set to "1" it enables an interrupt that occurs when the comparator output goes from "1" to "0". When this bit is set to "0" the interrupt is masked.
TONE IRQ MASK (Bit 3)	When this bit is set to "1" it enables an interrupt that occurs when the TONE IRQ FLAG (Bit 3, IRQ FLAG Register, $8F) changes from "0" to "1". When this bit is "0" the interrupt is masked.
CTCSS FAST IRQ MASK (Bit 2)	When this bit is set to "1" it enables an interrupt that occurs when the CTCSS FAST IRQ FLAG (Bit 2, IRQ FLAG Register, $8F) changes from "0" to "1". When this bit is "0" the interrupt is masked.
DCS IRQ MASK (Bit 0)	When this bit is set to "1" it enables an interrupt that occurs when the DCS DECODE/NO DECODE FLAG (Bit 7, SELCALL & SUB-AUDIO STATUS Register $81) changes state. When this bit is set to "0" the interrupt is masked.

Table 13: IRQ MASK Register (Hex address $8E)

4.4.10 CTCSS TX/FAST RX FREQUENCY Register (Hex address $83)

This is a 16-bit register. Byte (1) is sent first. When the CTCSS fast detector is enabled, the bits 0 to 12 define the receive frequency which the fast predictive detector is looking for according to the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{16 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When the CTCSS transmitter is enabled, the bits 0 to 12 control the frequency of the transmitted CTCSS tones according to the formula above.

When the fast detector and the transmitter are both enabled, bits 0-12 define the receive frequency which the fast predictive detector is looking for and the frequency of the transmitted tone according to the formula above. (i.e. Tx Tone = predictive tone).

When Bit 7 in byte (1) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming the bits 0 to 12 to "0" puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the SUBAUDIO Tx and the CTCSS FAST DETECT.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.4.11 RX TONE PROGRAM Register (Hex address $84)

This is a 16-bit register. Byte (1) is sent first. The two bytes are used to program the center frequencies of up to 15 tones in either the audio or sub-audio band that will be decoded by the receiver.

Each tone is identified by its address in bits 7, 6, 5 and 4 of byte (1). The remaining 12 bits contain the data representing the tone frequency according to the formula below. If a tone is not required the 12 bits should be set to zero.

Byte 1								Byte 2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	<---------- N ---------->				<---------- R ---------->							
0	0	0	1												
0	0	1	0	N is the binary representation of the				R is the nearest 6-bit binary							
0	0	1	1	following decimal number (n):				representation of (r), where:							
0	1	0	0												
0	1	0	1												
0	1	1	0												
0	1	1	1	SUBAUDIO (CTCSS)				SUBAUDIO (CTCSS)							
1	0	0	0	$n = INT (958982 \times f_{TONE} / f_{XTAL})$				$r = ((237245/f_{XTAL}) - (n/(4 \times f_{TONE}))) \times 8400$							
1	0	0	1												
1	0	1	0												
1	0	1	1												
1	1	0	0	INBAND (SELCALL)				INBAND (SELCALL)							
1	1	0	1	$n = INT (83244 \times f_{TONE} / f_{XTAL})$				$r = ((20811/f_{XTAL}) - (n/(4 \times f_{TONE}))) \times 96000$							
1	1	1	0												

Table 14: RX TONE PROGRAM Register (Hex address $84)

Example: To program 100Hz when using the recommended 4.032MHz Xtal in SUBAUDIO (CTCSS) mode.

n = INT (958982 x 100 / 4.032 x 10^6)
= INT (23.536) = 23
N = 010111 (binary)

r = ((237245 / 4.032 x 10^6) - (23 / (4 x 100))) x 8400
= 11.26

R = 11 (rounding up if exactly halfway)
= 001011 (binary)

Thus the 12-bit code is 010111001011

The Hex address represented by bits 7, 6, 5 and 4 in byte (1) is used as the code to indicate which tone has been decoded. This code appears in bits 3, 2, 1 and 0 of the SELCALL and SUB-AUDIO STATUS Register (Hex address $81). The 15 programmed tones use Hex addresses $0 - $E.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.4.12 AUDIO CONTROL Register (Hex address $8A)

This is a 16-bit register. Byte (1) is sent first. Bits 0 - 5 of the first byte in this register are used to set the attenuation of the Modulator 1 amplifier and bits 0 - 5 of the second byte in this register are used to set the attenuation of the Modulator 2 amplifier, according to Table 15.

BYTE 1							BYTE 2						
5	4	3	2	1	0	Mod. 1 Attenuation	5	4	3	2	1	0	Mod. 2 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})	0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB	1	0	0	0	0	0	>40dB
1	0	0	0	0	1	12.0dB	1	0	0	0	0	1	6.0dB
1	0	0	0	1	0	11.6dB	1	0	0	0	1	0	5.8dB
1	0	0	0	1	1	11.2dB	1	0	0	0	1	1	5.6dB
1	0	0	1	0	0	10.8dB	1	0	0	1	0	0	5.4dB
1	0	0	1	0	1	10.4dB	1	0	0	1	0	1	5.2dB
1	0	0	1	1	0	10.0dB	1	0	0	1	1	0	5.0dB
1	0	0	1	1	1	9.6dB	1	0	0	1	1	1	4.8dB
1	0	1	0	0	0	9.2dB	1	0	1	0	0	0	4.6dB
1	0	1	0	0	1	8.8dB	1	0	1	0	0	1	4.4dB
1	0	1	0	1	0	8.4dB	1	0	1	0	1	0	4.2dB
1	0	1	0	1	1	8.0dB	1	0	1	0	1	1	4.0dB
1	0	1	1	0	0	7.6dB	1	0	1	1	0	0	3.8dB
1	0	1	1	0	1	7.2dB	1	0	1	1	0	1	3.6dB
1	0	1	1	1	0	6.8dB	1	0	1	1	1	0	3.4dB
1	0	1	1	1	1	6.4dB	1	0	1	1	1	1	3.2dB
1	1	0	0	0	0	6.0dB	1	1	0	0	0	0	3.0dB
1	1	0	0	0	1	5.6dB	1	1	0	0	0	1	2.8dB
1	1	0	0	1	0	5.2dB	1	1	0	0	1	0	2.6dB
1	1	0	0	1	1	4.8dB	1	1	0	0	1	1	2.4dB
1	1	0	1	0	0	4.4dB	1	1	0	1	0	0	2.2dB
1	1	0	1	0	1	4.0dB	1	1	0	1	0	1	2.0dB
1	1	0	1	1	0	3.6dB	1	1	0	1	1	0	1.8dB
1	1	0	1	1	1	3.2dB	1	1	0	1	1	1	1.6dB
1	1	1	0	0	0	2.8dB	1	1	1	0	0	0	1.4dB
1	1	1	0	0	1	2.4dB	1	1	1	0	0	1	1.2dB
1	1	1	0	1	0	2.0dB	1	1	1	0	1	0	1.0dB
1	1	1	0	1	1	1.6dB	1	1	1	0	1	1	0.8dB
1	1	1	1	0	0	1.2dB	1	1	1	1	0	0	0.6dB
1	1	1	1	0	1	0.8dB	1	1	1	1	0	1	0.4dB
1	1	1	1	1	0	0.4dB	1	1	1	1	1	0	0.2dB
1	1	1	1	1	1	0dB	1	1	1	1	1	1	0dB
X = don't care													
MOD1 ENABLE (Bit 5, first byte)						When this bit is "1" the MOD1 attenuator is enabled. When this bit is "0" the MOD1 attenuator is disabled (i.e. powersaved).							
MOD2 ENABLE (Bit 5, second byte)						When this bit is "1" the MOD2 attenuator and the SUMMING AMP are enabled. When this bit is "0" they are both disabled (i.e. powersaved).							
(Bits 7 and 6, first and second bytes)						Reserved for future use. These should be set to "0".							

Table 15: AUDIO CONTROL Register (Hex address $8A)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.4.13 SELCALL TX Register (Hex address $8D)

This is a 16-bit register. Byte (1) is sent first.

When the SELCALL transmitter is enabled, bits 0 to 12 control the frequency of the transmitted SELCALL tones according to the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{4 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming bits 0 through 12 to "0" places the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the SELCALL Tx.

4.5 8-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
	SELCALL &	DCS	CTCSS			RX TONE			
$81	SUB-AUDIO STATUS	DECODE/ NO DECODE	FAST TONE	0	TONE DECODE	MSB BIT 3	BIT 2	BIT 1	LSB BIT 0
			GP TIMER	COMP	COMP	TONE	CTCSS FAST		DCS
$8F	IRQ FLAG	0	IRQ FLAG	0 to 1 IRQ FLAG	1 to 0 IRQ FLAG	IRQ FLAG	IRQ FLAG	0	IRQ FLAG

Table 16: 8-bit Read Only Registers

4.6 Read Only Register Description

4.6.1 SELCALL and SUB-AUDIO STATUS Register (Hex address $81)

This register is used to indicate the status of the device as described below:

DCS DECODE/ NO DECODE (Bit 7)	When the DCS decoder is enabled this bit is continuously updated with the result. A "1" indicates a successful decode (with 3 or less errors). A "0" indicates a failure to decode.
CTCSS FAST TONE (Bit 6)	When Bit 5 in the SIGNALING CONTROL Register and Bit 3 in the SIGNALING SET-UP Register are set to enable FAST CTCSS DETECT mode, this bit will be set to "1" if a periodic tone is detected. If no periodic tone is detected this bit will be "0".
	When bits 5 and 3 are set to enable FAST CTCSS PREDICTIVE mode, this bit will be set to "1" if a periodic tone that matches the frequency programmed in the CTCSS TX/FAST RX FREQUENCY Register is detected. If no match is found this bit will be "0". When Bit 5 in the SIGNALING CONTROL Register is set to "0" this bit will be "0".
(Bit 5)	Reserved for future use. This will be set to "0" but should be ignored by the user's software.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

TONE DECODE (Bit 4)	This bit indicates the status of the tone decoder. A "1" indicates a tone has been detected (TONE DECODE) and a "0" indicates the loss of the tone (NOTONE). TONE DECODE means that a tone has been decoded and its characteristics are defined by the bandwidth (See SIGNALING SET-UP Register bits 7, 6, 5 and 4) and the RX TONE number (See SELCALL and SUB-AUDIO STATUS Register bits 3, 2, 1 and 0). When Bit 6 in the SIGNALING CONTROL Register is set to "0" the TONE DECODE bit 4 will be set to "0". Identification of a valid tone which is not in the pre-programmed list of up to 15 tones will cause the decoder to move to the TONE DECODE state with the RX TONE address of "1111" in bits 3, 2, 1 and 0; indicating a valid, but unrecognized, tone. Loss of tone, will cause the NOTONE timer to be started. If loss of tone continues for the duration of the timeout period, then the decoder will move to NOTONE state and the identification of pre-programmed tones will start again.
RX TONE (Bits 3, 2, 1 and 0)	These four bits hold a Hex number from $0 to $F. Numbers $0 to $E represent the address of the tone decoded according to the tones programmed in the RX TONE PROGRAM Register, $84. The Hex number $F indicates the presence of any tone that is not described by DECODER BANDWIDTH (Bits 7, 6, 5 and 4, SIGNALING SET-UP Register, $82) and FREQUENCY (Bits 11 - 0, RX TONE PROGRAM Register, $84).

Table 17: SELCALL and SUB-AUDIO STATUS Register (Hex address $81)

4.6.2 IRQ FLAG Register (Hex address $8F)

This register is used to indicate when the device requires attention as below:

(Bits 7 and 1)	Reserved for future use. These will be set to "0" but should be ignored by user's software.
GPT IRQ FLAG (Bit 6)	When the general purpose timer has reached zero in its internal register, this bit will be set to "1" to indicate the timeout has expired. This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).
COMP 0 to 1 IRQ FLAG (Bit 5)	When the comparator output goes from "0" to "1" (i.e. when the input voltage is above the DAC output voltage) this bit will be set to "1" and an interrupt generated (if bit 5 of the IRQ MASK Register $8E is set to "1"). This bit is set to "0" when the IRQ FLAG Register $8F is read.
COMP 1 to 0 IRQ FLAG (Bit 4)	When the comparator output goes from "1" to "0" this bit will be set to "1" and an interrupt generated (if bit 4 of the IRQ MASK Register $8E is set to "1"). This bit is set to "0" when the IRQ FLAG Register $8F is read.
TONE IRQ FLAG (Bit 3)	When RX TONE DECODE (Bit 4, SELCALL and SUB-AUDIO STATUS Register, $81) changes state this bit will be set to "1". This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).
CTCSS FAST IRQ FLAG (Bit 2)	When CTCSS FAST TONE (Bit 6, SELCALL and SUB-AUDIO STATUS Register, $81) changes state this bit will be set to "1". This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).
DCS IRQ FLAG (Bit 0)	When DCS DECODE/NO DECODE (Bit 7 SELCALL and SUB-AUDIO STATUS Register, $81) changes state this bit will be set to "1". This bit is cleared to "0" by a read of the IRQ FLAG Register (Hex address $8F).

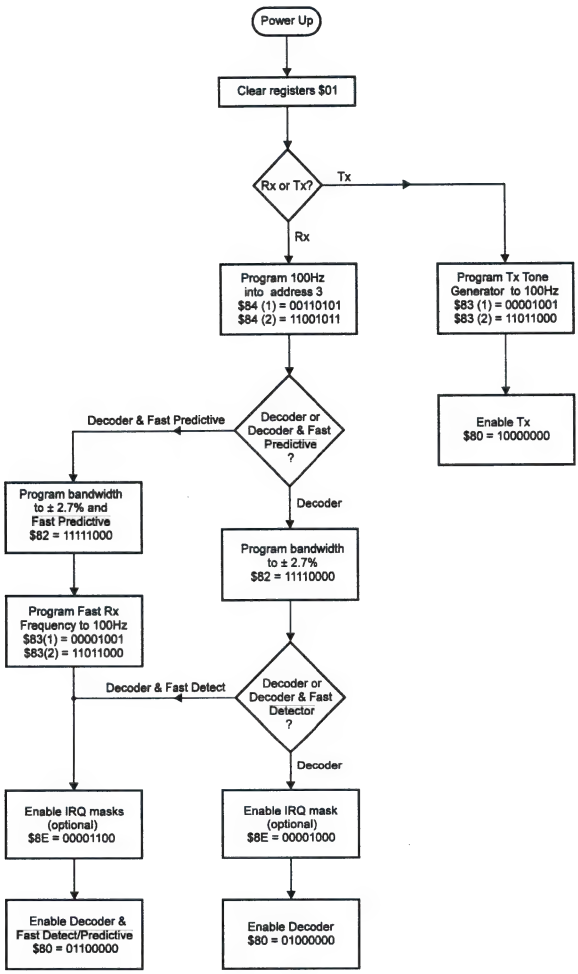
Table 18: IRQ FLAG Register (Hex address $8F)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

The flow chart shows the following modes of operation for the example below:

1. Decode)
2. Decode and Fast Detect) e.g. Address 3 = 100Hz, bandwidth = ±2.7%, interrupt enabled
3. Decode & Fast Predictive)
4. Transmit, e.g. Tx = 100Hz

Note: $8X is the Hex address/command.

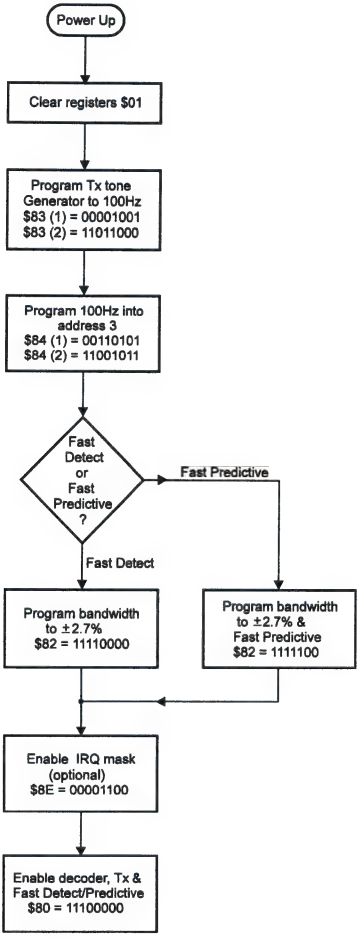

Power Up
Clear registers $01
Rx or Tx?
Tx
Rx
Program 100Hz into address 3 $84 (1) = 00110101 $84 (2) = 11001011
Program Tx Tone Generator to 100Hz $83 (1) = 00001001 $83 (2) = 11011000
Enable Tx $80 = 10000000
Decoder or Decoder & Fast Predictive ?
Decoder & Fast Predictive
Decoder
Program bandwidth to ± 2.7% and Fast Predictive $82 = 11111000
Program bandwidth to ± 2.7% $82 = 11110000
Program Fast Rx Frequency to 100Hz $83(1) = 00001001 $83(2) = 11011000
Decoder or Decoder & Fast Detector ?
Decoder & Fast Detect
Decoder
Enable IRQ masks (optional) $8E = 00001100
Enable IRQ mask (optional) $8E = 00001000
Enable Decoder & Fast Detect/Predictive $80 = 01100000
Enable Decoder $80 = 01000000

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

The flow chart shows the decoder, fast detect/fast predictive and transmitter enabled with the following example.

1. Tx tone generator = 100Hz
2. Decoder programmed with 100Hz in address 3
3. Bandwidth setting = ±2.7%
4. Interrupt enabled

Note: $8X is the Hex address/command.


Power Up
Clear registers $01
Program Tx tone Generator to 100Hz $83 (1) = 00001001 $83 (2) = 11011000
Program 100Hz into address 3 $84 (1) = 00110101 $84 (2) = 11001011
Fast Detect or Fast Predictive ?
Fast Predictive
Fast Detect
Program bandwidth to ±2.7% $82 = 11110000
Program bandwidth to ±2.7% & Fast Predictive $82 = 1111100
Enable IRQ mask (optional) $8E = 00001100
Enable decoder, Tx & Fast Detect/Predictive $80 = 11100000

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. Application

5.1 General

The MX828 is intended for use in radio systems where signaling is required for functions such as trunking, control, selective calling or group calling.

The CTCSS fast/predictive detector is useful for the detection of occupied channels indicating either the presence of any sub-audio tone, or range of tones, depending if it is set in fast detect or predictive mode. This will increase the efficiency of scanning and trunking systems, reducing the average time allocated to assessing each channel.

The facility to decode any of up to 15 programmed tones allows the use of tones for various signaling functions such as masking a free channel or identifying sub groups within a user's groups.

Adjustable decoder bandwidths permit certainty and signal to noise performance to be traded when congestion or range limits the system performance.

5.2 Transmitters

5.2.1 CTCSS

The CTCSS transmitter is enabled with Bit 7 in the SIGNALING CONTROL Register ($80) and bit 1 in the SIGNALING SET UP Register ($82).

The Tx frequency is set using Bit 0 to Bit 12 in the CTCSS TX/FAST RX FREQUENCY Register ($83) using the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{16 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming the bits 0 to 12 to "0" puts the Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the SUBAUDIO Tx and the CTCSS FAST DETECT (Bits 7 and 5 in the SIGNALING CONTROL Register $80).

5.2.2 The SelCall transmitter

The SelCall transmitter is enabled with Bit 2 in the SIGNALING CONTROL Register ($80).

The Tx frequency is set using Bit 0 to Bit 12 in the SELCALL TX Register ($8D) using the formula below:

$$A = \frac{f_{XTAL}\ (Hz)}{4 \times f_{TONE}\ (Hz)}$$

where A is the binary number programmed into the 13 bits.

When Bit 7 (in the first 8 bits) is set to "1" the tone output is set at V_{BIAS} or NOTONE without regard to the number "A" programmed. When Bit 7 is "0" the programmed tone is set on the output. Programming the bits 0 to 12 to "0" puts the SelCall Tx into powersave and the output goes to V_{BIAS}. Powersave is also achieved by disabling the SELCALL TX ENABLE (Bit 2 in the SIGNALING CONTROL Register $80).

5.2.3 DCS Transmitter

The DCS transmitter is enabled with Bit 7 in the SIGNALING CONTROL Register ($80) and bit 1 in the SIGNALING SET UP Register ($82).

The Tx data is set in the DCS BYTE 3, DCS BYTE 2 and DCS BYTE 1 Registers ($85, $86 and $87).

Note: The DCS transmitter produces an inverted output. When the signal is fed through the summing amp, in an inverted configuration, the correct polarity of the DCS signal will be restored (The MOD1 and MOD2 amplifier blocks do not invert).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.3 Receiver (CTCSS/SelCall Decoder)

The CTCSS/SelCall decoder should first be set up according to the desired characteristics. This entails setting the TONE DECODER MODE Bit 2 of the SIGNALING SET UP Register ($82), and setting the TONE decoder bandwidth in the SIGNALING SET-UP Register ($82), also programming the center frequencies of the desired tones in the RX TONE PROGRAM Register ($84). (It can hold up to 15 different tones). Any tone can be in any location. When the device is decoding, the tones are scanned in the sequence of their location, i.e. $0 first and $E last. Once a tone is detected the remaining tones are not checked. Therefore if two tones are close enough in frequency for their bandwidths to overlap then the one in the lowest location will be detected.

The TONE IRQ MASK in the IRQ MASK Register ($8E) should also be set as required.

The TONE DECODER ENABLE in the SIGNALING CONTROL Register ($80) should then be set to "1". While in the CTCSS/SelCall decoder mode the fast/predictive detector may be enabled (see below).

When the CTCSS/SelCall decoder detects a change in its present state an IRQ will be generated and Bit 3 of the IRQ FLAG Register ($8F) will indicate this.

The change that occurred can be read from Bit 4 of the SELCALL and SUB-AUDIO STATUS Register ($81) and if a tone is indicated by this bit then the number of that tone can be read from Bits 3, 2, 1 and 0 of the same register.

5.4 Receiver (CTCSS Fast/Predictive Detector)

This is used for detecting, in the fastest possible time, that sub-audio tones are present on the Rx channel. Response time is optimized for speed at the expense of frequency resolution.

It is enabled using Bit 5 of the SIGNALING CONTROL Register ($80). It has an IRQ which may be unmasked with Bit 2 of the IRQ MASK Register ($8E). The FAST CTCSS MODE DETECT/PREDICTIVE Bit 3 in the SIGNALING SET-UP Register ($82) allows for one of two alternatives in the FAST mode. In DETECT mode it will detect any periodic tone in the sub-audio band and when in PREDICTIVE mode it will detect specific tones determined by the frequency set in the CTCSS TX/FAST RX FREQUENCY Register ($83) and the fixed PREDICTIVE mode bandwidth. Successful detection is indicated by the CTCSS FAST IRQ FLAG Bit 2 in the IRQ FLAG Register ($8F), and the CTCSS FAST TONE Bit 6 in the SELCALL and SUB-AUDIO STATUS Register ($81).

5.5 Receiver (DCS Decoder)

The incoming signal is matched with the DCS code programmed into the DCS BYTE 1/2/3 Registers. When the DCS decoder is enabled, the DCS DECODE/NO DECODE FLAG in Bit 7 of the SELCALL and SUB-AUDIO STATUS Register ($81) will be set if the decode is successful (3 or fewer errors). A "0" flag indicates a failure to decode. This flag is updated for every bit of the incoming signal.

In order to detect the DCS turn-off code (134Hz) the CTCSS tone decoder should also be enabled and programmed with this value. Once detected, this will cause a CTCSS tone decoder interrupt, the receiver audio output should then be muted.

5.6 General Purpose Timer (GPT)

This may be used in conjunction with the CTCSS/SelCall decoder to form part of the decode algorithm or as a timer for any other purpose. It has an 8-bit value in the GENERAL PURPOSE TIMER Register ($8B) set in units of 1msec, an IRQ FLAG in Bit 6 of the IRQ FLAG Register ($8F) and an IRQ MASK in Bit 6 of the IRQ MASK Register ($8E).

5.7 Full Duplex Modes

Although the device is specified as half duplex, the only functions that must operate as such are:

DCS Tx	or	DCS Rx
DCS Tx	or	CTCSS Tx
CTCSS decode	or	SELCALL decode

All other functions are totally independent and therefore a full duplex CTCSS or full duplex SELCALL along with many other combinations are possible.

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.

5.7.1 Tx / Fast Rx Tone Table : CTCSS

The following table lists the commonly used CTCSS tones and the corresponding values for programming the transmitter frequency / fast predictive frequency register (Hex address $83).

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	E	B1	**114.8**	8	93	**186.2**	5	49
69.3	E	34	**118.8**	8	49	**189.9**	5	2F
71.9	D	B1	**123.0**	8	1	**192.8**	5	1B
74.4	D	3B	**127.3**	7	BC	**196.6**	5	2
77.0	C	C9	**131.8**	7	78	**199.5**	4	EF
79.7	C	5A	**136.5**	7	36	**203.5**	4	D6
82.5	B	EF	**141.3**	6	F7	**206.5**	4	C4
85.4	B	87	**146.2**	6	BC	**210.7**	4	AC
88.5	B	1F	**151.4**	6	80	**218.1**	4	83
91.5	A	C2	**156.7**	6	48	**225.7**	4	5D
94.8	A	62	**159.8**	6	29	**229.1**	4	4C
97.4	A	1B	**162.2**	6	12	**233.6**	4	37
100.0	9	D8	**167.9**	5	DD	**241.8**	4	12
103.5	9	83	**173.8**	5	AA	**250.3**	3	EF
107.2	9	2F	**179.9**	5	79	**254.1**	3	E0
110.9	8	E0	**183.5**	5	5D			

Table 19: Tx/Fast Rx Tone Table CTCSS

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.7.2 Rx Tone Program Tables : CTCSS

The following table lists the commonly used CTCSS tones together with the values for programming the "RX TONE PROGRAM" register (Hex address $84).

Note: The values for byte 1 and 2 below apply to tone address 0 only. These values will vary depending on the location they are programmed into.

Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
67.0	3	D8	**114.8**	6	C0	**186.2**	A	C9
69.3	4	9	**118.8**	6	D1	**189.9**	B	8
71.9	4	1B	**123.0**	7	10	**192.8**	B	44
74.4	4	4E	**127.3**	7	50	**196.6**	B	83
77.0	4	83	**131.8**	7	C0	**199.5**	B	8A
79.7	4	94	**136.5**	8	2	**203.5**	B	C9
82.5	4	CB	**141.3**	8	44	**206.5**	C	6
85.4	5	2	**146.2**	8	86	**210.7**	C	46
88.5	5	14	**151.4**	8	C9	**218.1**	C	C3
91.5	5	4C	**156.7**	9	C	**225.7**	D	41
94.8	5	87	**159.8**	9	48	**229.1**	D	48
97.4	5	94	**162.2**	9	82	**233.6**	D	89
100.0	5	CB	**167.9**	9	C6	**241.8**	E	8
103.5	6	7	**173.8**	A	B	**250.3**	E	88
107.2	6	45	**179.9**	A	84	**254.1**	E	C7
110.9	6	82	**183.5**	A	C2			

Table 20: Rx Tone Program Tables : CTCSS

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.7.3 Tx Tone Program Table : SelCall

The following two tables list commonly used SelCall tonesets together with the values for programming the 'SELCALL TX' register ($8D).

EEA			CCIR			ZVEI 1			ZVEI 2		
Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)
1981	01	FD	1981	01	FD	2400	01	A4	2400	01	A4
1124	03	81	1124	03	81	1060	03	B7	1060	03	B7
1197	03	4A	1197	03	4A	1160	03	65	1160	03	65
1275	03	17	1275	03	17	1270	03	1A	1270	03	1A
1358	02	E6	1358	02	E6	1400	02	D0	1400	02	D0
1446	02	B9	1446	02	B9	1530	02	93	1530	02	93
1540	02	8F	1540	02	8F	1670	02	5C	1670	02	5C
1640	02	67	1640	02	67	1830	02	27	1830	02	27
1747	02	41	1747	02	41	2000	01	F8	2000	01	F8
1860	02	1E	1860	02	1E	2200	01	CA	2200	01	CA
1055	03	BB	2400	01	A4	2800	01	68	885	04	73
930	04	3C	930	04	3C	810	04	DC	810	04	DC
2247	01	C1	2247	01	C1	970	04	0F	740	04	0F
991	03	F9	991	03	F9	885	04	73	680	05	CA
2110	01	DE	2110	01	DE	2600	01	84	970	04	0F

Table 21: Tx Tone Program Table : SelCall

5.7.4 Rx Tone Program Table : SelCall

The following two tables list commonly used SelCall tonesets together with the values for programming the 'RX TONE PROGRAM' register ($84) in each Tone Address location as shown.

	EEA			CCIR			ZVEI 1			ZVEI 2		
Tone Address	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq. (Hz)	Byte 1 (hex)	Byte 2 (hex)	Freq (Hz)	Byte 1 (hex)	Byte 2 (hex)
0	1981	A	A	1981	A	A	2400	C	44	2400	C	44
1	1124	15	C3	1124	15	C3	1060	15	53	1060	15	53
2	1197	26	D	1197	26	D	1160	25	D2	1160	25	D2
3	1275	36	85	1275	36	85	1270	36	83	1270	36	83
4	1358	46	D1	1358	46	D1	1400	47	E	1400	47	E
5	1446	57	4D	1446	57	4D	1530	57	C8	1530	57	C8
6	1540	67	CB	1540	67	CB	1670	68	86	1670	68	86
7	1640	78	4B	1640	78	4B	1830	79	49	1830	79	49
8	1747	88	CD	1747	88	CD	2000	8A	42	2000	8A	42
9	1860	99	84	1860	99	84	2200	9B	43	2200	9B	43
10	1055	A5	51	2400	AC	44	2800	AE	46	885	A4	86
11	930	B4	C4	930	B4	C4	810	B4	14	810	B4	14
12	2247	CB	83	2247	CB	83	970	C4	D8	740	C3	C8
13	991	D5	A	991	D5	A	885	D4	86	680	D3	80
14	2110	EA	C5	2110	EA	C5	2600	ED	45	970	E4	D8

Table 22: Rx Tone Program Table : SelCall

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.7.5 DCS Code Table

The following table gives a list of DCS codes together with the corresponding values (in Hex) which should be programmed into the DCS BYTE registers for a 23-bit DCS sequence.

DCS Code	DCS Byte 3 ($85)	DCS Byte 2 ($86)	DCS Byte 1 ($87)
023	76	38	13
025	6B	78	15
026	65	D8	16
031	51	F8	19
032	5F	58	1A
043	5B	68	23
047	0F	D8	27
051	7C	A8	29
054	6F	48	2C
065	5D	18	35
071	67	98	39
072	69	38	3A
073	2E	68	3B
074	74	78	3C
114	35	E8	4C
115	72	B8	4D
116	7C	18	4E
125	07	B8	55
131	3D	38	59
132	33	98	5A
134	2E	D8	5C
143	37	A8	63
152	1E	C8	6A
155	44	D8	6D
156	4A	78	6E
162	6B	C8	72
165	31	D8	75
172	05	F8	7A
174	18	B8	7C
205	6E	98	85
223	68	E8	93
226	7B	08	96
243	45	B8	A3
244	1F	A8	A4
245	58	F8	A5
251	62	78	A9
261	17	78	B1
263	5E	88	B3
265	43	C8	B5
271	79	48	B9
306	0C	F8	C6
311	38	D8	C9

DCS Code	DCS Byte 3 ($85)	DCS Byte 2 ($86)	DCS Byte 1 ($87)
315	6C	68	CD
331	23	E8	D9
343	29	78	E3
346	3A	98	E6
351	0E	B8	E9
364	68	58	F4
365	2F	08	F5
371	15	88	F9
411	77	69	09
412	79	C9	0A
413	3E	99	0B
423	4B	99	13
431	6C	59	19
432	62	F9	1A
445	7B	89	25
464	27	E9	34
465	60	B9	35
466	6E	19	36
503	3C	69	43
506	2F	89	46
516	41	B9	4E
532	0E	39	5A
546	19	E9	66
565	0C	79	75
606	5D	99	86
612	67	19	8A
624	0F	59	94
627	01	F9	97
631	72	89	99
632	7C	29	9A
654	4C	39	AC
662	24	79	B2
664	39	39	B4
703	22	B9	C3
712	0B	D9	CA
723	39	89	D3
731	1E	49	D9
732	10	E9	DA
734	0D	A9	DC
743	14	D9	E3
754	20	F9	EC

Table 23: DCS Code Table

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW / P Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency		4.0315968	4.0324032	MHz

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz
Audio Level 0dB ref. = 308 mV_{RMS} at 1kHz
V_{DD} = 3.3V to 5.0V, T_{AMB}= 25°C.
Composite Signal = 308 mV_{RMS} at 1kHz + 75mV_{RMS} Noise + 31 mV_{RMS} Sub-Audio Signal
Noise Bandwidth = 5kHz Band Limited Gaussian

		Notes	Min.	Typ.	Max.	Units
DC Parameters						
I_{DD}						
All Powersaved		1, 2		0.6	TBA	mA
FAST DETECT Enabled		1, 2		3.0	TBA	mA
Rx Operating						
DCS, FAST DETECT and CTCSS or SelCall		1, 2		4.0	TBA	mA
Tx Operating						
DCS or SelCall or SUB AUDIO		1, 2		4.0	TBA	mA
DCS and SelCall		1, 2		5.0	TBA	mA
"C-BUS" Interface						
Input Logic "1"			70%			V_{DD}
Input Logic "0"					30%	V_{DD}
Input Leakage Current	Logic "1" or "0"		-1.0		1.0	µA
Input Capacitance					7.5	pF
Output Logic "1"	I_{OH} = 120µA		90%			V_{DD}
Output Logic "0"	I_{OL} = 360µA				10%	V_{DD}
"Off" State Leakage Current	$V_{OUT} = V_{DD}$	6			10	µA
AC Parameters						
TONE Decoder						
Sensitivity	Pure Tone	5		-26.0		dB
CTCSS						
Response Time	Composite Signal			140		ms
De-response Time	Composite Signal			145		ms
Frequency Range			60		253	Hz
SelCall						
Response Time	Composite Signal			14		ms
De-response Time	Good Signal			22		ms
Frequency Range			625		3000	Hz
DCS Decoder						
Bit-Rate Sync Time				2		edges
Sensitivity		1	58		116	mV_{P-P}
CTCSS Detector - Fast Detect						
Sensitivity	Pure CTCSS Tone	5		-26.0		dB
Response Time	Composite Signal			56.0		ms

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

		Notes	Min.	Typ.	Max.	Units
CTCSS Detector - Fast Predictive						
Sensitivity	Pure CTCSS Tone	5		-26.0		dB
Response Time	Composite Signal	7		37.0		ms
CTCSS Encoder						
Frequency Range			60.0		253	Hz
Tone Frequency Resolution					0.3	%
Tone Amplitude Tolerance		1	-1.0	0	+1.0	dB
Total Harmonic Distortion		9		2.0		%
SELCALL Encoder						
Frequency Range			208		3000	Hz
Tone Frequency Resolution					0.2	%
Tone Amplitude Tolerance		1	-1.0		+1.0	dB
Total Harmonic Distortion		9		2.0		%
DCS Encoder						
Bit Rate				134.4		bps
Amplitude Tolerance		1	-1.0		+1.0	dB
Amplitude		1		871		mV_{P-P}
Audio Band-Pass Filter						
Passband		8	300		3000	Hz
Passband Gain (at 1.0kHz)		8		0		dB
Passband Ripple	wrt gain at 1.0kHz	8	-2		+0.5	dB
Stopband Attenuation		8	33.0			dB
Residual Hum and Noise				-50.0		dBp
Alias Frequency				63		kHz
Output Impedance						
TX AUDIO OUT, TX SUB AUDIO OUT and RX AUDIO OUT						
Enabled		10		2.0		kΩ
Disabled				500		kΩ
Rx Amp and Summing Amp						
Open Loop Gain	input = 1mV at 100Hz			70.0		dB
Unity Gain Bandwidth				5.0		MHz
Input Impedance	at 100Hz		10			MΩ
Output Impedance	Open Loop			6.0		kΩ
Transmitter Modulator Drives:						
Mod.1 Attenuator						
Attenuation	at 0dB		-0.2	0	0.2	dB
Cumulative Attenuation Error	wrt attenuation at 0dB		-1.0		1.0	dB
Output Impedance		3		600		Ω
Input Impedance	at 100Hz			15.0		kΩ

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

	Notes	Min.	Typ.	Max.	Units
Mod.2 Attenuator					
Attenuation at 0dB		-0.2	0	0.2	dB
Cumulative Attenuation Error wrt attenuation at 0dB		-0.6		0.6	dB
Output Impedance	3		600		Ω
General Purpose Timer					
Timing Period Range		1		255	ms
Count Interval			1		ms
Xtal/Clock Input					
Pulse Width ('High' or 'Low'	4	40.0			ns
Input Impedance (at 100Hz)		10.0			MΩ
Gain input = $1mV_{RMS}$ at 100Hz		20.0			dB
D/A					
Range	1	312.5		2500	mV
Step Size	1		312.5		mV
Step Accuracy	1		±10		mV
Input Impedance COMPIN			10		MΩ
Output Impedance COMPOUT			1		kΩ

Table 24: Operating Characteristics

Operating Characteristics Notes:

1. At V_{DD} = 5.0V only. Signal levels or currents are proportional to V_{DD}.
2. Not including any current drawn from the device by external circuitry.
3. Small signal impedance, at V_{DD} = 5.0V and T_{AMB} = 25°C.
4. Timing for an external input to the XTAL/CLOCK pin.
5. With input gain components set as recommended in Figure 2.
6. $\overline{IRQ}$ pin.
7. From one tone to another tone.
8. See filter response (Figure 3).
9. Measured at MOD 1 or MOD 2 output.
10. SUBAUDIO, SELCALL and DCS.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

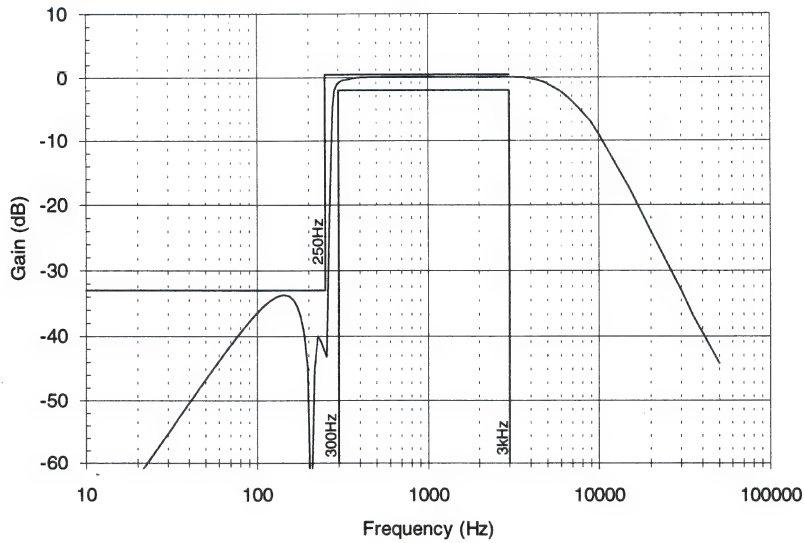


Figure 3: Audio Band-Pass Filter Frequency Response

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.2 Timing Diagrams

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, V_{DD} = 3.3V to 5.0V, T_{AMB} = -40°C to +85°C.

	Parameter	Min.	Typ.	Max.	Units
t_{CSE}	"CS-Enable to Clock-High"	2.0			µs
t_{CSH}	Last "Clock-High to CS-High"	4.0			µs
t_{HIZ}	"CS-High to Reply Output 3-state"			2.0	µs
t_{CSOFF}	"CS-High" Time between transactions	2.0			µs
t_{NXT}	"Inter-Byte" Time	4.0			µs
t_{CK}	"Clock-Cycle" time	2.0			µs

Notes:

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µC serial interface formats "C-BUS" compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

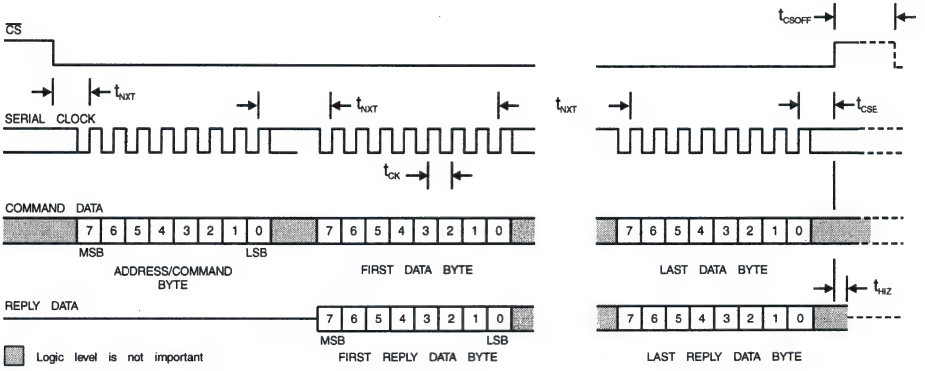
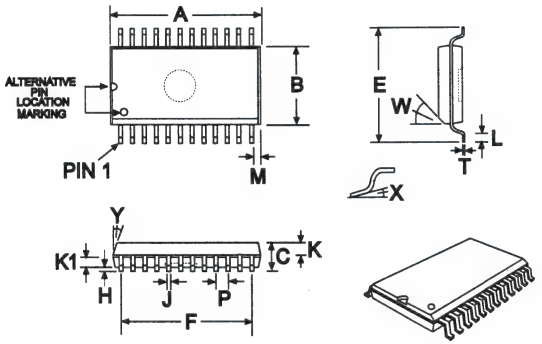


Figure 4: "C-BUS" Timing

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

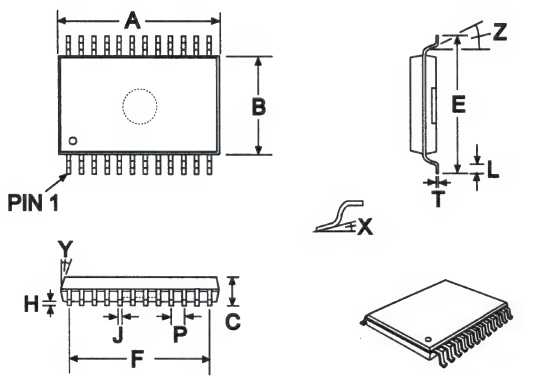
6.3 Packaging



DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.291 (7.39)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.394 (10.01)		0.419 (10.64)
F		0.566 (14.37)	
H	0.004 (0.10)		0.012 (0.30)
J	0.014 (0.36)		0.018 (0.46)
K	0.036 (0.91)		0.046 (1.17)
K1	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
M	0.021 (0.53)		0.031 (0.79)
P		0.050 (1.27)	
T	0.009 (0.23)		0.012 (0.30)
W		45°	
X	0°		8°
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 5: 24-pin SOIC Mechanical Outline: *Order as part no. MX828DW*

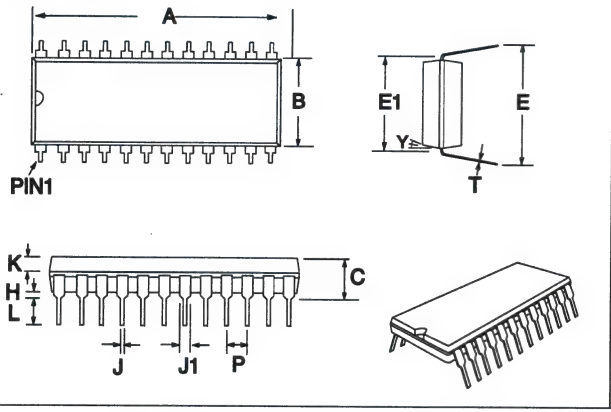


DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.212 (5.38)
C	0.068 (1.73)		0.078 (1.99)
E	0.301 (7.65)		0.311 (7.90)
F		0.286 (7.15)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 6: 24-pin SSOP Mechanical Outline: *Order as part no. MX828DS*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: Figure 5: 24-pin PDIP Mechanical Outline: Order as part no. MX828P

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480161.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Technical Specifications

Section 4: Sequential Tone Encoder/Decoder IC's

Device	Description	Page
MX803A	Audio Signaling Processor	3

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX803A Audio Signaling Processor

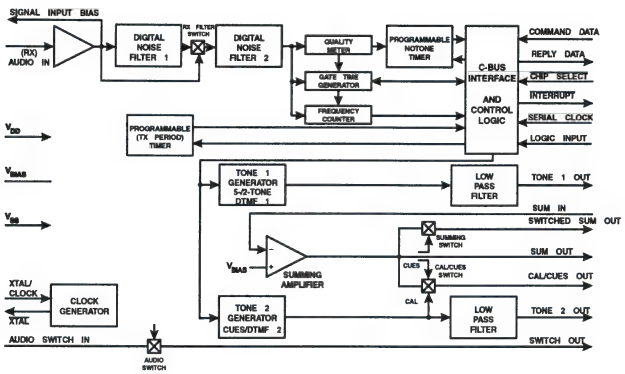
PRELIMINARY INFORMATION

Features

- **Full Duplex Audio Signaling Processor**
  - **Single Tone**
  - **Selective Call systems**
- **Tone Decoder with programmable NOTONE timer.**
- **Two Individual tone encoders and a programmable TX Period Timer.**
- **Low Power CMOS Device**
- **On-Chip programmable amplifier.**
- **C-BUS Compatible**

Applications

- **Signaling Systems supported**
  - **SelCall (CCIR, EEA, ZVEI I / II /III)**
  - **2-Tone SelCall**
  - **DTMF Encode**
- **Inband Tone Signaling capability for LMR and other Radio Systems.**



The MX803A is an audio signaling processor that provides inband tone signaling capabilities for LMR and other Radio systems. A low-power CMOS device, the MX803A is a member of the DBS800 (Digitally integrated Baseband Sub-system) IC family (See section 4.2). Supported Signaling systems include SelCall (CCIR, EEA, ZVEI I, II, and III) 2-Tone SelCall and DTMF encode. The use of a non-predictive decoder and a versatile encoder, allows the MX803A to operate in any standard or non-standard tone system.

The MX803A is a full-duplex device for use with Single Tone or Selective Call systems. The MX803A consists of a tone decoder with a programmable NOTONE timer, two individual tone encoders and a programmable TX period timer, and an on-chip summing amplifier. Under the control of a µC, the MX803A will simultaneously encode and transmit 1 or 2 audio tones in the 208-3000Hz range, as well as detect, decode, and indicate the frequency of any non-predicted input tone in the frequency range of 313 to 6000Hz.

The MX803A is available in 24-pin CDIP (MX803AJ), 24-pin PLCC (MX803ALH), and 24-pin SOIC (MX803ADW) packages.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480122.003

CONTENTS

Section Page

1. Block Diagram 4-5
2. Signal List 4-6
3. External Components 4-8
4. General Description 4-9
   - 4.1 DESCRIPTION 4-9
   - 4.2 DBS800 Systems 4-9
   - 4.3 C-BUS Control 4-10
5. Application 4-10
   - 5.1 MX803A Internal Registers 4-10
   - 5.2 Address/Commands 4-11
   - 5.3 Powersave 4-20
   - 5.4 Interrupt Request $\overline{IRQ}$ 4-21
   - 5.5 Operational Recommendations 4-22
   - 5.6 General Reset 4-22
6. Timing Information 4-22
7. Performance Specification 4-24
   - 7.1 Electrical Performance 4-24
   - 7.2 Packaging 4-27

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480122.003

1. Block Diagram

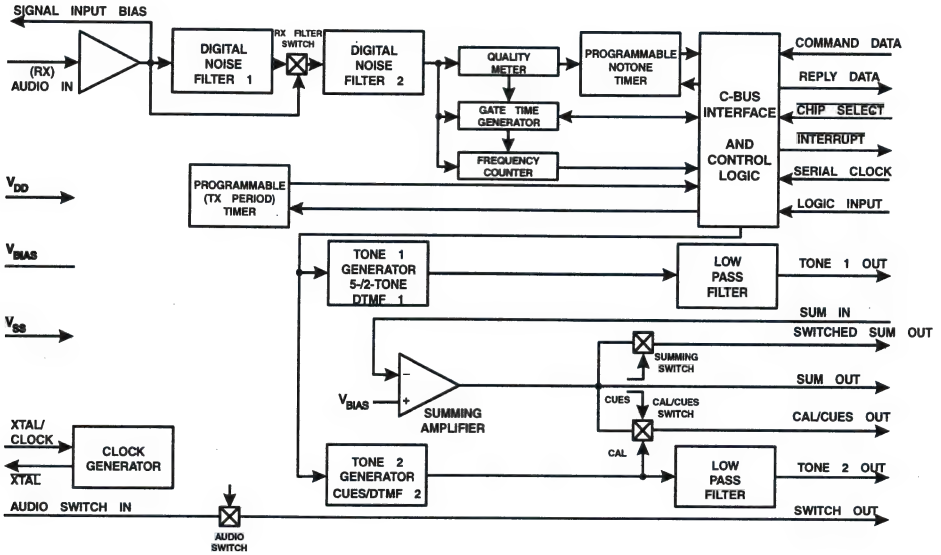


Figure 1: Block Diagram

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480122.003

2. Signal List

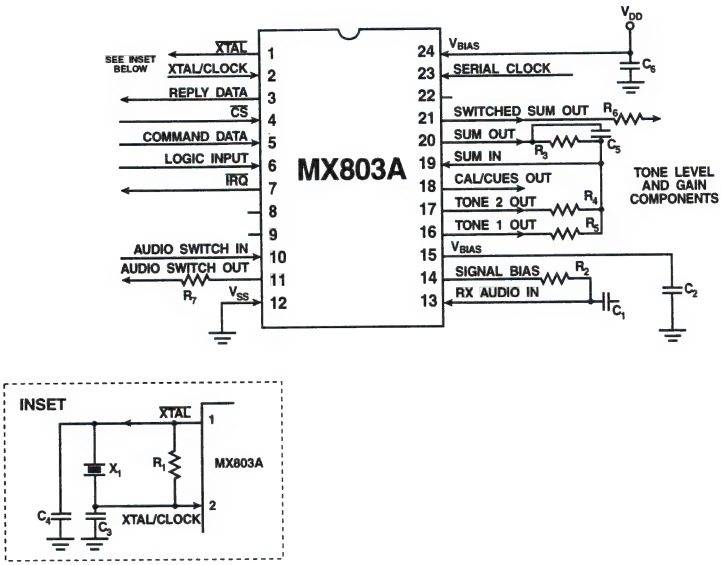
Pin No.	Name	Type	Description
1	$\overline{XTAL}$	Output	Output of the on-chip clock oscillator. External components are required at this output when a Xtal is used. See Figure 2.
2	Xtal/Clock	Input	Input to the on-chip clock oscillator inverter. A Xtal or externally derived clock should be connected here. See Figure 2.
3	Reply Data	Output	C-BUS serial data output to the µC. The transmission of Reply Data bytes is synchronized to the Serial Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the µC. See Figure 8 and Figure 9.
4	$\overline{CS}$	Input	C-BUS data loading control function. This input is provided by the µC. Data transfer sequences are initiated, completed or aborted by the chip select signal. See Figure 8 and Figure 9.
5	Command Data	Input	C-BUS serial data input from the µC. Data is loaded to this device in 8-bit bytes, MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock. See Figure 8 and Figure 9.
6	Logic Input	Input	This "real-time" input is available as a general purpose logic input port which can be read from the Status Register. See Table 3. G/Purpose Timer Period Expired NOTONE Timer Period Expired RX Tone Measurement Complete These interrupts are inactive during relevant powersave conditions and can be disabled by bits 5 and 6 in the Control Register.
7	$\overline{IRQ}$	Output	Output of this pin indicates an interrupt condition to the µC by going to a logic "0." This is a "wire-or-able" output, allowing the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic "0" when active and a high impedance when inactive. The system IRQ line requires one pullup resistor to V_{DD}. The conditions that cause interrupts are indicated in the Status Register and are shown below:
10	Audio Switch In	Input	Input to the stand-alone on-chip Audio Switch. This function is enabled/disabled by Bit 7 of the Control Register
11	Audio Switch Out	Output	Output of the stand-alone on-chip Audio Switch..
12	V_{SS}	Power	Negative supply (GND).
13	Rx Audio In	Input	Received audio tone signaling input. This input must be ac coupled and connected, using external components, to the Signal Input Bias pin. See Figure 2.
14	Signal Input Bias	Input	External components are required between this input and the RX Audio In pin. See Figure 2.
15	V_{BIAS}	Output	Internal circuitry bias signal, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C2. See Figure 2..
16	Tone 1 Out	Output	Tone 1 Generator (2-/5-tone Selcall or DTMF 1) output. External gain and coupling components are required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to the TX Tone Generator 1 Register (Table 5). See Figure 2.
17	Tone 2 Out	Output	Tone 2 Generator (2-/5-tone Selcall, CUES or DTMF 2) output. External gain and coupling components are required at this output when operating in a complete DBS 800 audio installation. The frequency of this output is determined by writing to the TX Tone Generator 2 Register (Table 5). See Figure 2.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Pin No.	Name	Type	Description
18	CAL/CUES Out	Output	An auxiliary, selectable tone frequency output, providing a square wave CALibration signal from the Tone 2 Generator or a sine wave CUES (beep) signal from the Summing Amplifier. The output mode (CAL or CUES) is selected by Bit 14 in the TX Tone Generator 2 Register (Table 5). When Tone Generator 2 is set to Notone, the CAL input is pulled to V_{BIAS}; during a powersave of Tone Generator 2 it is held at V_{SS}.
19	Sum in	Input	Input to the on-chip Summing Amplifier. This amplifier is available for combining Tone 1 and Tone 2 outputs (DTMF). Gain and coupling components should be used at this input to provide the required system gains. See Figure 2 and Figure 3
20	Sum Out	Output	Output of the on-chip summing amplifier. Combined tones (1 and 2) are available at this output. See Figure 2 and Figure 3.
21	Switched Sum Out	Output	This is the combined tone output available for transmitter modulation. The switch allows control of the MX803A output. Control of this switch is by Bit 4 of the Control Register. See Figure 2 and Figure 3.
23	Serial Clock	Input	C-BUS serial clock input. This clock, produced by the µC, is used for transfer timing of commands and data to and from the MX803A. See Figure 8 and Figure 9.
24	V_{DD}	Power	Positive supply. A single +5 volt power supply is required. Levels and voltages within this Audio Signaling Processor are dependent upon this supply..
8, 9, 22	N/C		No Internal Connection. These pins may be connected to V_{SS} to improve screening and reduce noise levels around the MX803A.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

3. External Components



R1		1.0MΩ	±10%
R2		2.0MΩ	±10%
R3	Note 2, 3	100kΩ	±10%
R4	Note 2, 3	82.0kΩ	±10%
R5	Note 2, 3	122kΩ	±10%
R6	Note 2	100kΩ	±10%
R7	Note 2, 5	100kΩ	±10%

C1		0.1µF	±20%
C2		1.0µF	±20%
C3	Note 4	33.0pF	±20%
C4	Note 4	33.0pF	±20%
C5	Note 3	22.0pF	±20%
C6		1.0µF	±20%
X1	Note 1, 4	4.00MHz	

Figure 2: Recommended External Components

Notes:

1. Xtal/clock components described are recommended in accordance with MX-COM's Application Note on Standard and DBS 800 Crystal Oscillator Circuits (April 1990). For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. System Components whose values are calculated to allow the MX803A to operate with other DBS 800 microcircuits. Figure 3 shows these components used in the system signal paths.
3. R3, R4, R5 and C5 are tone mixing components calculated to provide a 3dB tone differential (twist) for use in a DTMF configuration. Single tone output levels are set independently.
4. When X1 > 5.00MHz, C3 = C4 = 18pF
5. R7 provides modulation level and matching outputs for the MX803A.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480122.003

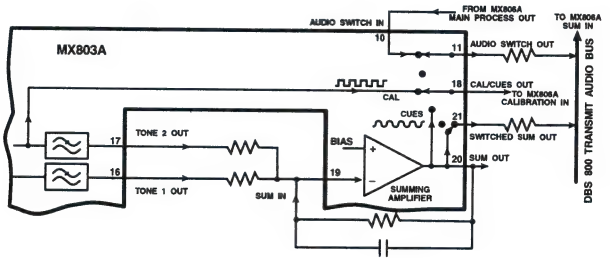


Figure 3: Example of Signal Switching in a DBS800 microcircuit

4. General Description

4.1 DESCRIPTION

The MX803A is an audio signaling processor that provides inband tone signaling capabilities for LMR and other Radio systems. A low-power CMOS device, the MX803A is a member of the DBS800 (Digitally integrated Baseband Subsystem) IC family (See section 4.2). Supported Signaling systems include SelCall (CCIR, EEA, ZVEI I, II, and III) 2-Tone SelCall and DTMF encode. The use of a non-predictive decoder and a versatile encoder, allows the MX803A to operate in any standard or non-standard tone system.

The MX803A is a full-duplex device for use with Single Tone or Selective Call systems. The MX803A consists of a tone decoder with a programmable NOTONE timer, two individual tone encoders and a programmable TX period timer, and an on-chip summing amplifier. Under the control of a µC, the MX803A will simultaneously encode and transmit 1 or 2 audio tones in the 208-3000Hz range, as well as detect, decode, and indicate the frequency of any non-predicted input tone in the frequency range of 313 to 6000Hz.

A general purpose logic input, interfacing directly with the Status Register, is provided. This may be used as an auxiliary method of routing digital information to the µC via C-BUS. Output frequencies are produced from data loaded to the MX803A. A programmable, general purpose, on-chip timer sets the tone transmit periods. A Dual-Tone Multi-Frequency (DTMF) output is obtained by combining the 2 independent output frequencies in the integral summing amplifier. This process can also be used for level correction.

Tones produced by the MX803A can be used in the system as modulation calibration inputs and as "CUE" audio indications to the operator. Received tones are measured and their frequency indicated to the µC in the form of a received data word. A poor quality or incoherent tone will indicate Notone.

4.2 DBS800 Systems

The Digitally-Integrated Baseband Subsystem (DBS800) is a family of low power ICs which provide a comprehensive range of audio processing and signaling functions for use within LMR and other Radio Systems. Each DBS800 IC may be used as part of a complete audio system, or each IC may operate as a stand alone. The system and ICs are partitioned in such a way that radio designers can easily select the device or devices appropriate to their needs.

The DBS800 family consists of the following ICs:

4.2.1 MX802 DVSR Codec

This is a full-duplex CVSD speech encoder/decoder with the ability to store and retrieve data within attached DRAM (Dynamic Random Access Memory) using an on-chip DRAM controller. The MX802 also provides on-chip input and output audio filtering.

4.2.2 MX803A Audio Signaling Processor

This provides an inband tone signaling ability to LMR and other Radio Systems.

4.2.3 MX805A Sub-Audio Signaling Processor

This provides a sub-audio and digital signaling (NRZ) ability to LMR and other Radio Systems.

4.2.4 MX806A Audio Processor

This is a half duplex audio processor providing all DBS800 system audio signal conditioning and filtering capabilities for the system transmit and receive paths.

4.2.5 MX809 MSK Modem

This is an intelligent, half-duplex 1200bps MSK/FFSK Modem with software programmable byte-synchronization system and checksum generation and checking.

4.2.6 MX812 VSR Codec

This is a half-duplex CVSD speech encoder/decoder with the ability to store and retrieve data within attached DRAM (Dynamic Random Access Memory) using an on-chip DRAM controller

4.3 C-BUS Control

C-BUS is the controlling hardware and software interface for all members of the DBS800 family. It enables the serial, bi-directional transfer of commands and data throughout the system, allowing total flexibility of operational control and data handling. System upgrades can be achieved by a simple software or firmware change.

The C-BUS physically consist of 5 lines. These lines are Serial Clock, Command Data, Reply Data, Chip Select ($\overline{CS}$), and Interrupt Request ($\overline{IRQ}$). A description of each may be found in section 2.

5. Application

Control of the MX803A Audio Signaling Processor's operation is by communication between the µC and the MX803A internal registers on the C-BUS using Address/Commands (A/Cs) and appended instructions or data. See Figure 8. The use and content of these instructions is detailed in the following sections.

For additional application information contact MX•COM, Inc.

5.1 MX803A Internal Registers

Control Register	30_H	Write only, control and configuration of the MX803A.
Status Register	31_H	Read only, reporting of device functions.
RX Tone Frequency Register	32_H	Read only, indicates frequency of the last received input.
RX Notone Timer	33_H	Write only, setting of the RX Notone period.
TX Tone Generator 1 Register	34_H	Write only, setting the required output frequency from TX Tone Generator 1.
TX Tone Generator 2 Register	35_H	Write only, setting the required output frequency from TX Tone Generator 2.
General Purpose Timer Register	36_H	Write only, setting of a general purpose sequential time period.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

5.2 Address/Commands

The first byte of a loaded data sequence is always recognized by the C-BUS as an Address/Command (A/C) byte. Instruction and data transactions to and from this device consist of an A/C byte followed by further instruction/data or a status/data reply.

Instructions and data are loaded and transferred via C-BUS in accordance with the timing information given in Figure 8 and Figure 9. Table 1 shows the list of A/C bytes relevant to the MX803A.

Command Assignment	Address/Command (A/C) Byte		Data Bytes
	Hex	Binary	
		msb lsb	
General Reset	01	00000001	
Write to Control Register	30	00110000	+ 1 byte instruction to Control Register
Read Status Register	31	00110001	+ 1 byte reply from Status Register
Read RX Tone Frequency	32	00110010	+ 2 bytes reply from RX Tone Register
Write to Notone Timer	33	00110011	+ 1 byte instruction to Notone Register
Write to TX Tone Gen. 1	34	00110100	+ 2 bytes instruction to TX Tone Gen. 1
Write to TX Tone Gen. 2	35	00110101	+ 2 bytes instruction to TX Tone Gen. 2
Write to G/Purpose Timer	36	00110110	+ 1 byte instruction to G/Purpose Timer

Table 1: C-BUS Address/Commands

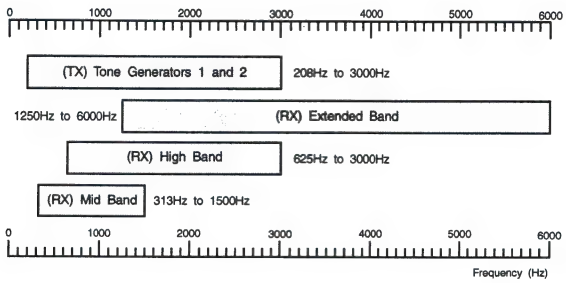


Figure 4: MX803A Frequencies

5.2.1 Write to Control Register

A/C 30_H, followed by 1 byte of Command Data

Audio Switch: Enables or Disables the stand-alone on-chip Audio Switch.

General Purpose Timer: This should be set up before interrupts are enabled since a General Reset command will set the timer period to 00_H - 0ms (permanent interrupt).

Interrupt Enable Instructions: Status bits 0, 1 and 2 are produced regardless of the state of these settings.

Band Selection: Bits 2 and 3 set the required frequency range. See Figure 4.

Summing Switch: Used to Enable or Disable the switch that controls the MX803A output.

Interrupt Designation: Decoder Interrupts

Notone Timer and RX Tone Measurement

Transmitter Interrupt

G/Purpose Timer Interrupt

Setting		Control Bits
MSB		Transmitted First
Bit 7		Audio switch
1		Enable
0		Disable
Bit 6		G/Purpose Timer Interrupt
1		Enable
0		Disable
Bit 5		Decoder Interrupts
1		Enable
0		Disable
Bit 4		Summing Switch
1		Enable
0		Disable
Bit 3	Bit 2	Band Selection
0	0	High Band
0	1	Mid Band
1	0	Extended Band
1	1	Do not use this setting
Bit 1		Set to
0		0
Bit 0		Set to
0		0

Table 2: Control Register

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

5.2.2 Read Status Register

A/C 31_H, followed by 1 byte of Reply Data

Interrupt Requests (IRQ): Interrupts on this device are available to draw the attention of the µC to a change in the condition of the bit in the status register. However, bits are set in the status register irrespective of the setting of interrupt enable bits (Table 2) and these changes may be recognized by polling the register.

General Purpose Timer Period: Set to a logic "1" when the timer period has expired. Cleared to a logic "0" by:

1. Reading the Status Register
2. New G/Purpose Timer information
3. General Reset command

Notone Timer Period: Set to a logic "1" when the timer period has expired. Cleared to a logic "0" by:

1. Reading the Status Register
2. New Notone Timer information
3. General Reset command

RX Tone Measurement: Set to a logic "1" when the RX Tone Measurement is complete. Cleared to a logic "0" by:

1. Reading the Status Register
2. General Reset command

Setting	Status Bits
MSB	Received First
Bit 7	Set to
0	0
Bit 6	Set to
0	0
Bit 5	Set to
0	0
Bit 4	Set to
0	0
Bit 3	Logic Input Status
1	1
0	0
Bit 2	G/Purpose Timer Period
1	Expired
	(Interrupt Generated)
Bit 1	Notone Timer Period
1	Expired
	(Interrupt Generated)
Bit 0	RX Tone Measurement
1	Complete
	(Interrupt Generated)

Table 3: Status Register

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

5.2.3 TX Tone Generator Registers 1 and 2

Each TX Tone Generator is controlled individually by writing a two-byte command to the relevant TX Tone Generator Register. The format of this command word, which is different for each tone generator, is shown below with the calculations required for tone frequency (f_{TONE}) generation described in the following text.

5.2.3.1 Write to TX Tone Generator 1 Register

A/C 34_H, followed by 2 bytes of Command Data

MSB (loaded first)			Bit Numbers												LSB (loaded last)
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Notone/Enable	These 13 bits (0 to 12) are used to produce a binary number, designated 'A'. 'A' is used in the formulas below to set the TX Tone 1 frequency ($f_{TONE}1$).												

Table 4: Tx Tone Generator 1

5.2.3.1.1 SETTING TX TONE GENERATOR 1

The binary number produced by Bits 0 to 12 (MSB) is designated "A." If "A" = all logic "0" TX Tone Generator 1 is Powersaved.

Bit 13 at logic 1 = Tone 1 Output at V_{BIAS} (NOTONE)
0 = Tone 1 Output Enabled

Bits14 and15(MSB) must be logic 0

5.2.3.2 Write to TX Tone Generator 2 Register

A/C 35_H, followed by 2 bytes of Command Data

MSB (loaded first)			Bit Numbers												LSB (loaded last
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CAL/CUES	Notone/Enable	These 13 bits (0 to 12) are used to produce a binary number, designated 'B'. 'B' is used in the formulas below to set the TX Tone 2 frequency ($f_{TONE}2$).												

Table 5: Tx Tone Generator 2

Write to TX Tone Generator 2 Register Notes:

Programming Tone Generator 2 to Notone will place the CAL/CUES output at V_{BIAS} via a 40kΩ internal resistor.

Programming Tone Generator 2 to Powersave will place the CAL/CUES output at V_{SS}.

If both Tone Generators are Powersaved, the Input Amplifier is also Powersaved

5.2.3.2.1 SETTING TX TONE GENERATOR 2

The binary number produced by bits 0 to 12 (MSB) is designated "B." If "B" = all logic "0" then TX Tone Generator 2 is Powersaved.

Bit 13 at logic 1 = Tone 1 Output at V_{BIAS} (NOTONE)
0 = Tone 1 Output Enabled
Bit 14 at logic 1 = Squarewave CAL Output
0 = Sinewave CUES Output

Bit 15 (MSB) must be a logic "0."

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

5.2.3.3 Calculations

As seen in Table 4 and Table 5, a binary number ("A" or "B" - bits 0 to 12) is loaded to the respective TX Tone Generator. The formulas described below are used to produce the required output frequency.

Required TX Tone output frequency	=	f_{TONE} 1 or 2
Xtal/clock frequency	=	f_{XTAL}
Input Data Word (bits 0 to 12)	=	"A" or "B"

$$f_{TONE} = \frac{f_{XTAL}}{4 \times \text{'A' or 'B'}} \text{ Hz} \quad \text{or} \quad \text{Input 'A' or 'B'} = \frac{f_{XTAL}}{4 \times f_{TONE}} \text{ Hz}$$

5.2.3.4 Tx Tone Frequencies

With reference to Table 4 and Table 5, while Input Data Words "A" or "B" can be programmed for frequencies outside the stated limits of 208Hz and 3000Hz, any output frequencies obtained may not be within specified parameters. See section 7.

5.2.4 Read RX Tone Frequency Register

A/C 32_H, followed by 2 bytes of Reply Data

5.2.4.1 Measurement of RX Signal Frequency S_{IN}

The input audio signal, S_{IN}, is measured in the Frequency Counter over a specified measurement period (9.125ms or 18.250ms).

The measuring function counts the number of complete input cycles occurring within the count period and then the number of measuring clock cycles necessary to make up the period.

When the count period of a successful decode is complete, the RX Tone Measurement bit in the Status Register and the Interrupt bit are set.

The RX Tone Frequency Register will now indicate the signal frequency S_{IN} in the form of 2 bytes (1 and 0) as illustrated in Figure 6.

Note: The following measurements are based on a clock frequency of 4.032 MHz. See section 5.2.4.4 for a scaling formula for other crystal values).

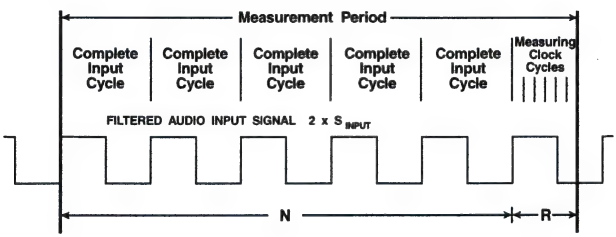


Figure 5: Measurement of an Rx Frequency

5.2.4.2 The Integer (N) - Byte 1

This is a binary number representing twice the number of complete input audio cycle periods. It is counted during the specified measurement period (t), when (t) is:

High Band Decode	=	9.125ms
Mid Band Decode	=	18.250ms
Extended Band Decode	=	9.125ms

Note: See section 5.2.4.4 for calculation of measurement period (t) using a Xtal other than 4.032MHz.

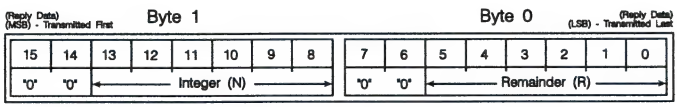
© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

5.2.4.3 The Remainder (R) - Byte 0

This is a binary number representing the remainder part, R, of twice the Input Signal Frequency. R = "the number of specified measuring-clock cycles" required to complete the specified measurement period (See 5.2.4.2). The clock cycle frequency (f) is:

High Band Decode	=	56.00kHz
Mid Band Decode	=	28.00kHz
Extended Band Decode	=	56.00kHz

Note: See section 5.2.4.4 for calculation of clock cycle frequency (f) using a Xtal other than 4.032MHz.


(Reply Data) (MSB) - Transmitted First
Byte 1
Byte 0
(Reply Data) (LSB) - Transmitted Last
15 14 13 12 11 10 9 8
7 6 5 4 3 2 1 0
"0" "0"
Integer (N)
"0" "0"
Remainder (R)

RX Frequency Register

Figure 6: Format of the Rx Tone Frequency Register

5.2.4.4 f_{XTAL} Scaling Factors

The following formulas allow the calculation of the Integer N (see section 5.2.4.2) and the Remainder R (see section 0) using any Xtal value.

$$t\ scaled = t \times \left(\frac{4.032}{f_{XTAL}}\right) \qquad f\ scaled = f \times \left(\frac{f_{XTAL}}{4.032}\right)$$

5.2.5 Frequency Measurement

The following formulas show the derivation of the Rx frequency S_{IN} from the measured data bytes (N and R)

Note: The following measurements are based on a clock frequency of 4.032 MHz. See section 5.2.4.4 for a scaling formula for other Xtal values.

5.2.5.1 High Band Measurement

S_{IN} - High Band

In the measurement period of 9.125ms, there are N cycles at $2S_{IN}$ and R clock cycles at 56.000kHz.

$$\frac{N}{2S_{IN}} + \frac{R}{56000} = 9.125ms$$

$$\text{from which } S_{IN} = \frac{28000 \times N}{(511 - R)}$$

N and R - High Band

The measurement period = 9.125ms.
Clock Frequency = 56.000kHz
The measured frequency = $2S_{IN}$Hz
In the measurement period there are:

$2S_{IN} \times 9.125 \times 10^{-3}$ cycles

N_{HIGH} is the lower integer value of the decimal number:

$N = INT(9.125 \times 10^{-3} \times 2S_{IN})$

R_{HIGH} is the lower integer value of the decimal number:

$$R = INT(9.125 \times 10 - 3 - \frac{N}{2S_{IN}}) \times 56000$$

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

5.2.5.2 Mid Band Measurement

S_{IN} - MID Band

In the measurement period of 18.250ms, there are N cycles at $2S_{IN}$ and R clock cycles at 28.000kHz.

$$\frac{N}{2S_{IN}} + \frac{R}{28000} = 18.250ms$$

$$\text{from which } S_{IN} = \frac{14000 \times N}{(511 - R)}$$

N and R - High Band

The measurement period = 18.250ms.
Clock Frequency = 28.000kHz
The measured frequency = $2S_{IN}$Hz
In the measurement period there are:

$2S_{IN} \times 18.250 \times 10^{-3}$ cycles

N_{MID} is the lower integer value of the decimal number:

$N = INT (18.250 \times 10^{-3} \times 2S_{IN})$

R_{MID} is the lower integer value of the decimal number:

$$R = INT (18.250 \times 10^{-3} - \frac{N}{2S_{IN}}) \times 28000$$

5.2.5.3 Extended Band Measurement

S_{IN} - Extended Band

In the measurement period of 9.125ms, there are N cycles at $2S_{IN}$ and R clock cycles at 56.000kHz.

$$\frac{N}{2S_{IN}} + \frac{R}{56000} = 9.125ms$$

$$\text{from which } S_{IN} = \frac{28000 \times N}{(511 - R)}$$

N and R - High Band

The measurement period = 9.125ms.
Clock Frequency = 56.000kHz
The measured frequency = $2S_{IN}$Hz
In the measurement period there are:

$2S_{IN} \times 9.125 \times 10^{-3}$ cycles

$N_{EXTENDED}$ is the lower integer value of the decimal number:

$N = INT (9.125 \times 10^{-3} \times 2S_{IN})$

$R_{EXTENDED}$ is the lower integer value of the decimal number:

$$R = INT (9.125 \times 10 - 3 - \frac{N}{2S_{IN}}) \times 56000$$

5.2.6 Write to RX Notone Timer Register

A/C 33_H, followed by 1 byte of Command Data

5.2.6.1 Operation of the RX Notone Timer

A NOTONE period is that period when no signal or a consistently bad quality signal is received. The NOTONE Timer is employed to indicate to the µC that a NOTONE situation has existed for a predetermined period.

The NOTONE Timer period is "primed" by writing to the NOTONE Timer Register (33_H) using the instructions and information (1 data byte) given in Table 6. This timer register can be written-to and set in any mode of the MX803A except "Notone Timer Powersave." Priming the timer sets the timing period; this period will not be allowed to start until at least one frequency (tone) measurement has been successfully completed.

The NOTONE Timer is a one-shot timer that is reset only by successful tone measurements.

If the quality of the received signal drops to an unusable level the NOTONE Timer will start its run-down. On completion of this timer period, the NOTONE Timer Period Expired bit in the Status Register and an Interrupt are set.

Upon detection of the Interrupt, the Status Register should be read by the µC to ascertain the source of the Interrupt.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

The NOTONE Timer Period Expired bit is cleared:

1. By a read of the Status Register.
2. New NOTONE Timer Information
3. General Reset Command

The timer is set to 00_H by a General Reset command.

Setting				Function / Period			
MSB							
7	6	5	4	Transmitted Bit 7 first			
0	0	0	0	these 4 bits must be 0			
				period (ms)			
3	2	1	0	High Band	%	Mid Band	%
0	0	0	0	0		0	
0	0	0	1	20	±1	40	±1
0	0	1	0	40	±1	80	±1
0	0	1	1	60	±1	120	±1
0	1	0	0	80	±1	160	±1
0	1	0	1	100	±1	200	±1
0	1	1	0	120	±1	240	±1
0	1	1	1	140	±1	280	±1
1	0	0	0	160	±1	320	±1
1	0	0	1	280	±1	360	±1
1	0	1	0	200	±1	400	±1
1	0	1	1	220	±1	440	±1
1	1	0	0	240	±1	480	±1
1	1	0	1	260	±1	520	±1
1	1	1	0	280	±1	560	±1
1	1	1	1	300	±1	600	±1

Table 6: RX Notone Timer Settings

5.2.6.2 NOTONE TIMER CIRCUITRY

The following situations may be encountered by the Notone Timer Circuitry

5.2.6.2.1 No Signal

The Notone timer can only start its run down on completion of a valid frequency measurement.

5.2.6.2.2 No signal after a valid Tone measurement

The timer will start to run down when the last RX Tone Measurement complete bit is set. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

5.2.6.2.3 Signal fades after a valid Tone measurement

The timer will start to run down when the signal becomes unreadable to the device. At the end of the "primed" period the NOTONE Timer Period Expired bit in the Status Register and the Interrupt will be set.

5.2.6.2.4 Signal appears after the Timer has started

If the frequency measurement is more than 75% complete when the timer period expires, neither the NOTONE bit nor the Interrupt will be set unless that frequency measurement is subsequently aborted.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

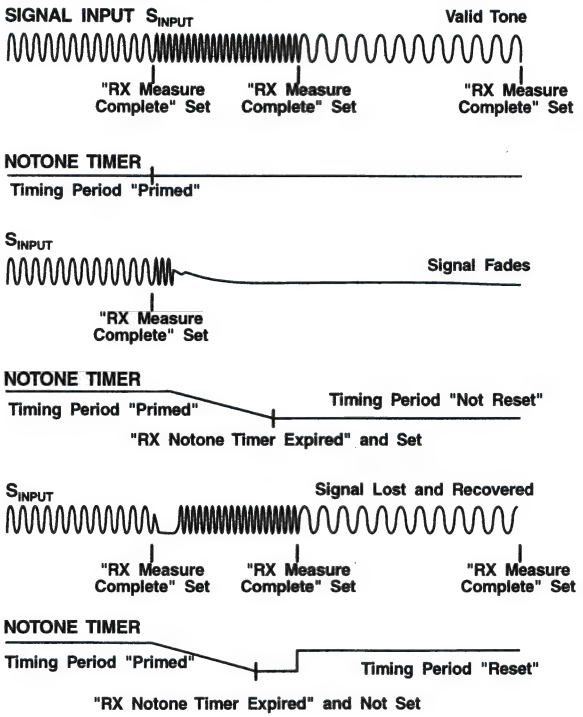


Figure 7: Notone Timing

5.2.7 Write to General Purpose Timer Register

A/C 36_H, followed by 1 byte of Command Data

5.2.7.1 Operation of the General Purpose Timer

This timer, which is not dedicated to any specific function within the MX803A, can be used within the DBS 800 system to indicate time-elapsed periods of between 10-150ms in the High Band or 20-300ms in the Mid Band to the µC. Setting of the timer is by loading a single byte data word via the C-BUS (See Table 7) to the MX803A through the Command Data line.

The timer will be reset and the run-down started on completion of Timer Data Word loading.

When the programmed time period has expired, the General Purpose Timer Expired bit (bit 2) in the Status Register and the Interrupt are set.

The General Purpose Timer Expired bit is cleared:

1. By a read of the Status Register
2. New G/P Timer information
3. General Reset Command.

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

When the programmed time period has expired, this timer will reset, restart itself and continue sequencing until:

1. New G/P Timer information is written
2. A General Reset Command is received.

The General Purpose Timer Expired bit and the interrupt will remain set until cleared.

The timer is set to 00_H (0ms) by a General Reset command.

Setting				Function / Period			
MSB							
7	6	5	4	Transmitted Bit 7 first			
0	0	0	0	these 4 bits must be 0			
				Reset Timer and Start Timing period (ms)			
3	2	1	0	High Band	%	Mid Band	%
0	0	0	0	0		0	
0	0	0	1	10	±1	20	±1
0	0	1	0	20	±1	40	±1
0	0	1	1	30	±1	60	±1
0	1	0	0	40	±1	80	±1
0	1	0	1	50	±1	100	±1
0	1	1	0	60	±1	120	±1
0	1	1	1	70	±1	140	±1
1	0	0	0	80	±1	160	±1
1	0	0	1	90	±1	180	±1
1	0	1	0	100	±1	200	±1
1	0	1	1	110	±1	220	±1
1	1	0	0	120	±1	240	±1
1	1	0	1	130	±1	260	±1
1	1	1	0	140	±1	280	±1
1	1	1	1	150	±1	300	±1

Table 7: General Purpose Timer Settings

5.3 Powersave

Various sections of the MX803A can be placed independently into a power-economical condition. Table 8 gives a summary of these states available to the MX803A.

Powersaved Section	Instruction Source		Table
Tone Encoder 1	TX Tone Gen. 1 Reg. (34_H)	All bits = "0"	Table 4
Tone Encoder 2	TX Tone Gen. 2 Reg. (35_H)	All bits = "0"	Table 5
Input Amplifier	This action is automatic when both Tone Encoders are in the Powersave condition		

Table 8: MX803A Powersave Functions

5.3.1 Powersave Conditions

Xtal/Clock and C-BUS: This circuitry is always active, on all DBS 800 ICs, under any depowered/powersaved conditions

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

5.4 Interrupt Request $\overline{IRQ}$

An Interrupt (IRQ), when enabled, is provided by the MX803A to indicate the following conditions to the µC.

	Notone Timer Period Expired	G/Purpose Timer Period Expired	Rx Tone Measurement Complete
Enabled	By control Resister bit 5	By control Resister bit 6	By control Resister bit 5
Set	When the preset Notone Flag is set	When the General Purpose Timer has timed out.	When an RX Frequency Measurement has been successfully completed
Identified	By Status Register bit 1	By Status Register bit 2	By Status Register bit 0
Cleared	By reading the Status Register	By reading the Status Register	By reading the Status Register

Table 9: Interrupt Request

On recognition of the "Read Status" Command byte, the interrupt output is cleared, the Status bits are transferred to the µC via the C-BUS Reply Data line and the internal Status bits are cleared.

5.5 Operational Recommendations

Following initial system power-up, a General Reset command should be sent.

5.5.1 Receive Sequence

1. Send Control Command for RX: Select Midband/Highband and Digital Filter length.
2. Disable transmitters if desired by writing to Tone Frequency registers.
3. Prime the Notone timer by sending the required period byte.
4. Enable/disable interrupts as desired.
5. When a valid tone has been detected by a successfully completed measurement the Status Register is set to "Tone Measurement Complete" and an interrupt is set to the µC.
6. The µC examines the Status Register. If tone measurement is complete, it reads in the RX Tone Frequency in the form N + R (Figure 6).
7. RX Tone Measurement Complete interrupts are periodically sent to the µC unless Notone is detected, in which case a Notone Interrupt is sent.

5.5.2 Transmit Sequence

1. Set Tone Frequency Generators to Notone during the transmitter initialization period.
2. Send Control Command for TX: Select Sum/Switched Sum Out and Audio Switch states.
3. Send General Purpose (GP) Timer information for the Notone transmitter initialization period. This will initiate the timer.
4. Enable/disable interrupts as desired.
5. µC waits for "GP Timer Expired," reads the Status Register to check interrupts due to timer, and resets the Status Bit. If required, the µC sends the next timer period followed by the next tone(s) frequency information. A new timer period sent will reset the timer, otherwise the timer is self-resetting.
6. The µC monitors the interrupts and repeats steps 5 and 6 as required.
7. After last loaded tone, µC turns off Tone Generator(s).

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

5.6 General Reset

Upon power-up the bits in the MX803A registers will be random (either "0" or "1"). A General Reset Command (01_H) will be required to reset all microcircuits on the C-BUS. It has the following effect on the MX803A:

Control Register	Set as 00_H
Status Register (bits 0, 1, 2)	Set as 00_H
Notone Timer	Set as 00_H
Tone Gen. 1 Reg. (2 bytes)	Set as 0000_H
Tone Gen. 2 Reg. (2 bytes)	Set as 0000_H
Gen. Purpose Reg.	Set as 00_H

Table 10: General Reset effect on MX803A

This sets the MX803A to Encoder High Band (625Hz to 3000Hz) with interrupts disabled and both timers set to 00_H. Both timers should be set up before interrupts are enabled to prevent initial, undesired interrupts.

6. Timing Information

Figure 8 shows timing parameters for two-way communication between the µC and the MX803A on the C-BUS.

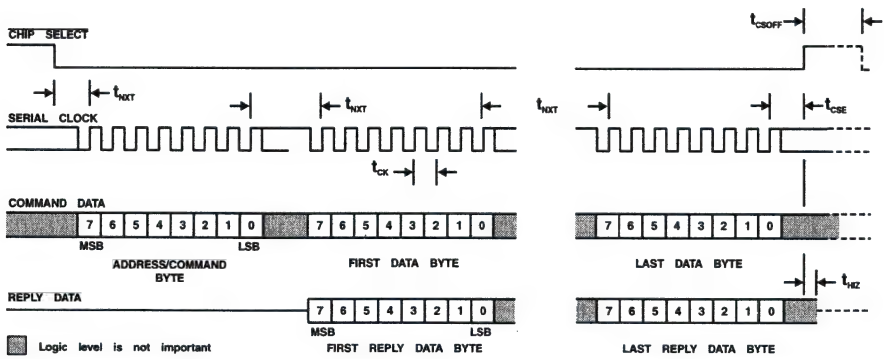


Figure 8: C-BUS Timing

Parameter		Min	Typ	Max	Unit
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0			µs
t_{CSH}	Last Serial Clock Rising Edge to Chip Select High	4.0			µs
t_{CSOFF}	Chip Select High	2.0			µs
t_{NXT}	Command Data Inter-Byte Time	4.0			µs
t_{CK}	Serial Clock Period	2.0			µs
t_{CH}	Decoder or Encoder Clock High	500			ns
t_{CL}	Decoder or Encoder Clock Low	500			ns
t_{CDS}	Command Data Set-Up Time	250			ns
t_{CDH}	Command Data Hold Time	0			ns
t_{RDS}	Reply Data Set-Up Time	250			ns
t_{RDH}	Reply Data Hold Time	50.0			ns
t_{HIZ}	Chip Select High to Reply Data High - Z			2.0	µs

Table 11: Timing Information

Timing Information Notes

1. Command Data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. Reply Data is read from the MX803A MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into the MX803A and into the µC on the rising Serial Clock edge.
3. Loaded data instructions are acted upon at the end of each individual, loaded byte.
4. To allow for differing µC serial interface formats, the MX803A will work with either polarity Serial Clock pulses.

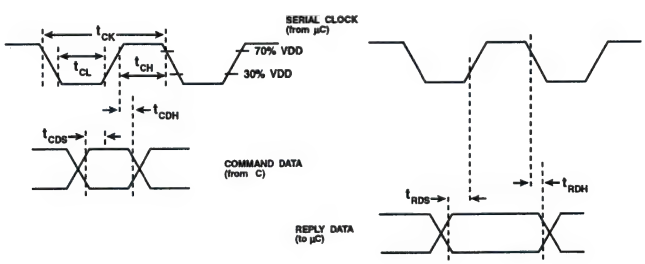


Figure 9: Timing Relationship for C-BUS Information Transfer

7. Performance Specification

7.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device. Operation of the device outside of the operating limits is not suggested.

General	Min.	Max.	Units
Supply Voltage (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / J / LH Packages			
Operating Temperature	-40	85	°C
Storage Temperature	-55	125	°C
Total allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

	Notes	Min.	Max.	Units
Supply (V_{DD}-V_{SS})		4.5	5.5	V
Temperature		-40	85	°C
Xtal/Clock Frequency			4.0	MHz

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = 5.0 @ T_{AMB} = 25°C Xtal = 4MHz (refer to section 5.2.4.4 for Xtal Scaling factor)
Audio level 0dB ref. = 308mV_{RMS} @ 1kHz (60% deviation, FM)
Noise Bandwidth = 5.0kHz Band-Limited Gaussian

	Notes	Min.	Typ.	Max.	Units
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Decoder + Both Timers			2.0		mA
Decoder, Both Timers + One TX only			4.0		mA
All Functions Enabled			5.0		mA
Analog Impedance					
RX Audio Input			20.0		MΩ
Summing Amp Input			20.0		MΩ
Switch			1.0		kΩ
Tones 1 and 2 Outputs			10.0		kΩ
CAL/CUES Output			5.0		kΩ
Summing Outputs			10.0		kΩ
Dynamic Values					
Digital Interface					
Input Logic "1"	1	3.5			V
Input Logic "0"	1			1.5	V
Output Logic "1" (I_{OH} = -120µA)	2	4.6			V
Output Logic "0" (I_{OL} = 360µA)	3			0.4	V
I_{OUT} Tristate (Logic "1" or "0")	3			4.0	µA
Input Capacitance	1			7.5	pF
I_{OX} (V_{OUT} = 5V)	4			4.0	µA
Overall Performances					
RX - Decoding					
High Band					
Sensitivity			-20.0		dB
Tone Response Time					
Good Signal	5,10			30.0	ms
Tone-to-Noise Ratio = 0dB	5,6,10			40.0	ms
Frequency					
Band		625		3000	Hz
Measurement Resolution			0.2		%
Measurement Accuracy	9		0.5		%

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
Doc. # 20480122.003

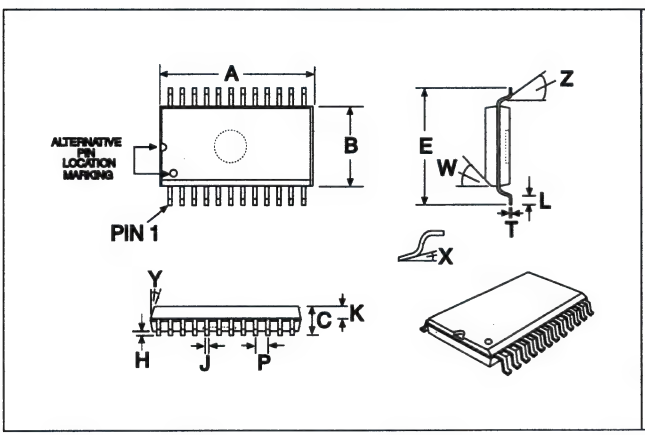
	Notes	Min.	Typ.	Max.	Units
Mid-Band					
Sensitivity			-20.0		dB
Tone Response Time					
Good Signal	7,10			60.0	ms
Tone-to-Noise Ratio = 0dB	6,7,10			80.0	ms
Frequency					
Band		313		1500	Hz
Measurement Resolution			0.2		%
Measurement Accuracy	9		0.5		%
Extended Band					
Sensitivity			-20.0		dB
Tone Response Time					
Good Signal	5,10			20.0	ms
Frequency					
Band		1250		6000	Hz
Measurement Resolution			0.2		%
Measurement Accuracy	9		0.5		%
TX - Encoders 1 and 2					
Tone Frequency		208		3000	Hz
Period ($1/f_{TONE}$) Error				1.0	µs
Tone Amplitude		-1.5		1.5	dB
Total Harmonic Distortion				5.0	%
Rise Time to 90%			$3/f_{TONE}$		ms
Fall Time to 10%	8			5.0	ms
Frequency Change Time			$3/f_{TONE}$		ms
Timers					
General Purpose					
Timing Period Range					
High-Band		10.0		150	ms
Mid-Band		20.0		300	ms
RX Notone					
Timing Period Range					
Hi-Band		20.0		300	ms
Mid-Band		40.0		600	ms
Xtal/Clock Frequency (f_{XTAL})			4.0	6.0	MHz

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Operating Characteristics Notes:

1. Device control pins: Serial Clock, Command Data, and $\overline{CS}$.
2. Reply Data output.
3. Reply Data and $\overline{IRQ}$ outputs.
4. Leakage current into the "Off" $\overline{IRQ}$ output.
5. Measurement period = 9.198ms.
6. Decode Probability = 0.993.
7. Measurement period = 18.396ms.
8. When set to Powersave.
9. For a good input signal.
10. Inversely proportional to Xtal frequency, i.e. Spec. x $\frac{4MHz}{f_{XTAL}}$. So, for a 6MHz clock a 30ms tone response time becomes 20ms.

7.2 Packaging

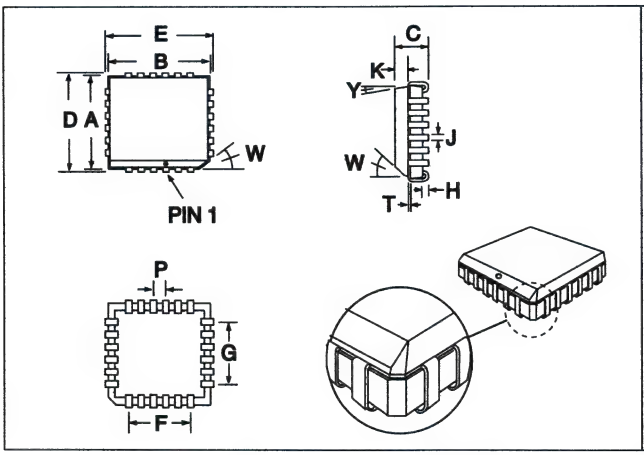


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin SOIC Mechanical Outline: order as part no. MX803ADW

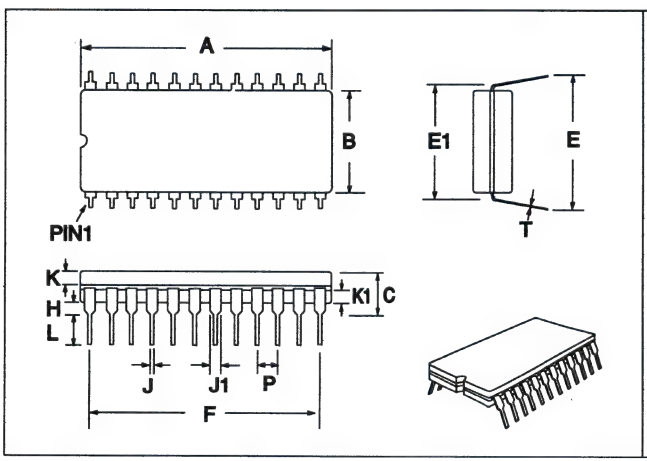


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 24-pin PLCC Mechanical Outline: order as part no. MX803ALH



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 12: 24-pin CDIP Mechanical Outline: order as part no. MX803AJ

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054

Technical Specifications

Section 5:
CVSD CODEC IC's

Device	Description	Page
MX109	Low Voltage Full Duplex CVSD CODEC with Serial Control	3
MX609	PCN/PCS Delta Modulation CODEC	17
MX619/629	Delta Modulation CODEC	25
MX802	DVSR CODEC	39
MX812	VSR CODEC with DRAM Control	55

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX109

Low Voltage, Full Duplex CVSD CODEC with Serial Control

ADVANCE INFORMATION

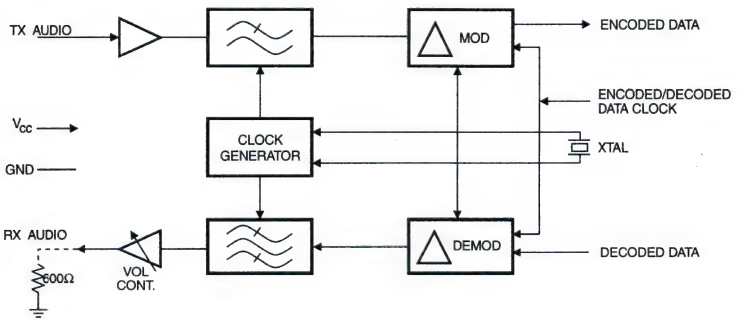
Shipping JUNE 1997

Features

- **Single Chip Full Duplex CVSD CODEC**
- **On-chip Input and Output Filters**
- **On-chip Volume Control**
- **Low Power, Single Supply analog CMOS**
- **Wide Frequency Reference using Ceramic Oscillator**

Applications

- **Digital Cordless Phones**
- **Digital PCN/PCS Systems**
- **Digital Delay Lines**
- **Digital Voice Storage**
- **Multiplexers**
- **Switches and Phones**
- **Time Domain Scramblers**



The MX109 is a CVSD (Continuously Variable Slope Delta Modulation) Codec. A low-power CMOS device, designed for use in cordless telephones, the MX109 is also suitable for applications in delta multiplexers, switches and phones, and Time Domain Scrambling. The encoder input and decoder output switched capacitor filters are incorporated on-chip.

Sampling clock rates can be externally injected in the 8k to 64k bps range. The internal clocks are derived from an on-chip reference oscillator driven by an externally connected crystal or ceramic resonator.

The encoder has an enable function for use in multiplexer applications and when disabled, the encoder output remains in a high-impedance "tri-state" mode.

The MX109 is available in 16-pin PDIP (MX109P), and 16-pin SOIC (MX109DW) packages.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480121.005
All trademarks and service marks are held by there respective companies.

CONTENTS

Section **Page**

1. Block Diagram 5-5

2. Signal List 5-6

3. External Components 5-7

4. General Description 5-7

5. Application 5-8

5.1 Control Data 5-8

5.1.1 Data Word Format 5-8

5.1.2 Bit Settings 5-8

5.2 Serial Interface Timing 5-9

5.3 CODEC 5-10

5.3.1 Timing Information 5-10

5.3.2 CODEC Performance 5-11

6. Performance Specification 5-12

6.1 Electrical Performance 5-12

6.1.1 Absolute Maximum Ratings 5-12

6.1.2 Operating Limits 5-12

6.1.3 Operating Characteristics 5-13

6.2 Packaging 5-15

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480121.005

4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

1. Block Diagram

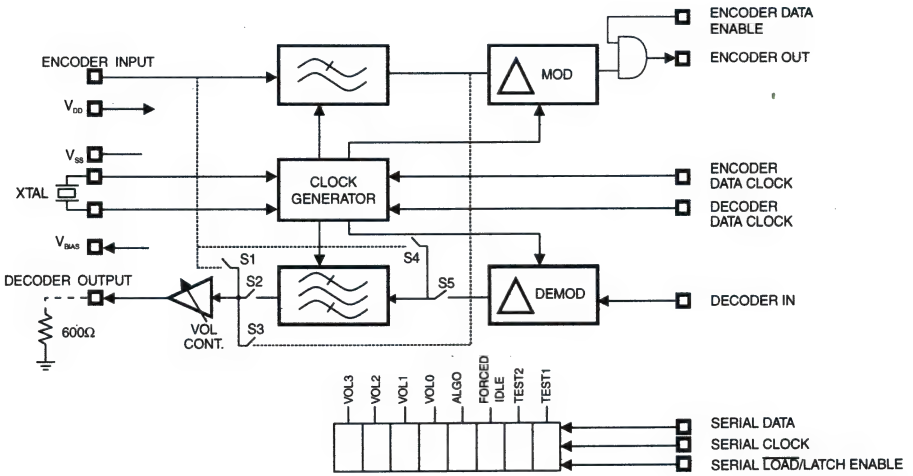


Figure 1: Device Block Diagram

Note: The state of S1-S5 is controlled via Test 1 and Test 2 according to Table 4

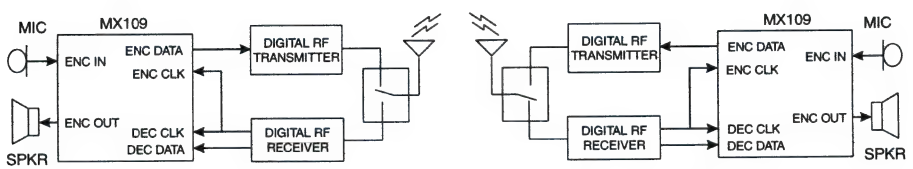


Figure 2: Typical Wireless System Incorporating the MX109

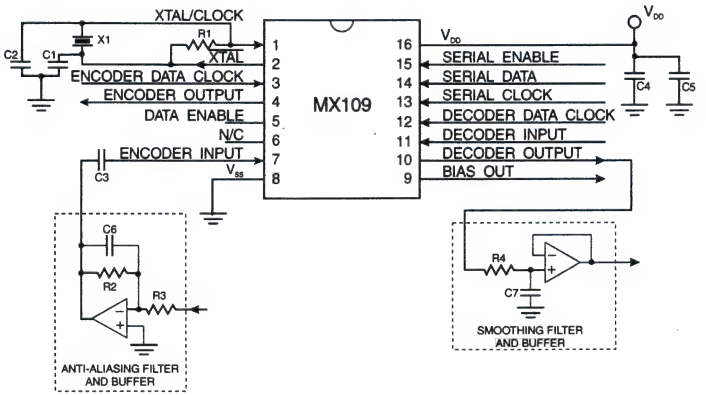
© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc. # 20480121.005

2. Signal List

Pin No.	Name	Type	Description
1	Xtal/Clock	Input	Input to the clock oscillator inverter. A 3.58 MHz Xtal input or externally derived clock is injected here. See Figure 3.
2	$\overline{\text{Xtal}}$	Output	The 3.58 MHz output of the clock oscillator inverter.
3	Encoder Data Clock		A logic port. External encode clock input.
4	Encoder Output	Output	The encoder digital output.
5	Encoder Data Enable	Input	Data is made available at the encoder output pin by control of this input. Internal 1MΩ pullup.
6	N/C		No internal Connection
7	Encoder Input	Input	The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 3.
8	V_{SS}	Power	Negative Supply, normally ground potential
9	V_{BIAS}	Output	Buffered $V_{DD}/2$.
10	Decoder Output	Output	The recovered analog signal is output at this pin. It is the buffered output of a bandpass filter and requires external components
11	Decoder Input	Input	The received digital signal input. Internal 1 MΩ pullup
12	Decoder Data Clock	Input	A logic port. External decode clock input
13	Serial Clock	Output	This is the serial clock input
14	Serial Data	Input	This is the serial data input. Data is loaded in the following order: VOL3, VOL2, VOL1, VOL0, ALGO, FORCE IDLE, TEST 2, TEST 1
15	Serial $\overline{\text{Load}}$ / Latch Enable	Input	A logic 1 applied to this input will enable serial programming
16	V_{DD}	Power	Positive Supply

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480121.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

3. External Components



R1	Note 1	1MΩ	±10%
R2		10kΩ	±10%
R3		10kΩ	±10%
R4		10kΩ	±10%
C1	Note 2	33pF	±20%
C2	Note 2	27pF	±20%

C3	Note 3	1.0µF	±20%
C4	Note 4	0.47µF	±20%
C5		0.001µF	±20%
C6		0.0022µF	±20%
C7		0.0022µF	±20%
X1	Note 5	3.58MHz	

Figure 3: Recommended External Components

External Component Notes:

1. Oscillator inverter bias resistor.
2. Xtal circuit load capacitor.
3. Encoder input coupling capacitor. The drive source impedance to this input should be less than 100Ω. Output idle channel noise levels will improve with an even lower source impedance.
4. V_{DD} decoupling capacitor.
5. Xtal circuitry shown is in accordance with MX-COM's Xtal Oscillator Application Note

4. General Description

The MX109 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in cordless telephones. The device is suitable for applications in delta multiplexers, switches and phones, and Time Domain Scramblers. The encoder input and decoder output switched capacitor filters are incorporated on-chip.

Sampling clock rates can be externally injected in the 8k to 64k bps range. The internal clocks are derived from an on-chip reference oscillator driven by an externally connected crystal or ceramic resonator.

The encoder has an enable function for use in multiplexer applications. When not enabled the encoder output remains in a high-impedance "tri-state" mode.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480121.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

5. Application

5.1 Control Data

Serial data is loaded into the MX109's serial shift register together with the serial clock. When a logic "0" is applied to the Load/Latch input the serial data is loaded into the parallel register. A logic "1" on the Load/Latch input latches the data into the parallel register to be used elsewhere in the chip. The data word format (see section 5.1.1) and bit settings (see section 5.1.2) are shown below. The timing diagram for loading the serial data is shown in Figure 4.

5.1.1 Data Word Format

AMP/ATTENUATION LEVEL							
D7	D6	D5	D4	D3	D2	D1	D0
VOL3	VOL2	VOL1	VOL0	ALG	FORCE IDLE	TEST 2	TEST 1

5.1.2 Bit Settings

GAIN	VOL3	VOL2	VOL1	VOL0
9dB	1	1	1	1
6dB	1	1	1	0
3dB	1	1	0	1
0dB	1	1	0	0
-3dB	1	0	1	1
-6dB	1	0	1	0
-9dB	1	0	0	1
-12dB	1	0	0	0
-15dB	0	1	1	1
-18dB	0	1	1	0
-21dB	0	1	0	1
-24dB	0	1	0	0
-27dB	0	0	1	1
-30dB	0	0	1	0
-33dB	0	0	0	1
MUTE	0	0	0	0

Table 1: Gain/Attenuation Selection

ALG	Algorithm Status
0	3-bit companding
1	4-bit companding

Table 2: Companding Algorithm Settings

FORCE IDLE	Encoder Output
1	1010101010 . . .
0	CVSD encoded signal

Table 3: Forced Idle Settings

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480121.005
All trademarks and service marks are held by there respective companies.

TEST 1	TEST 2	MODE
0	0	Normal Operation
0	1	ENC IN to volume Control
1	0	ENC IN to decode BPF to volume control
1	1	ENC IN to Encode LPF to volume control

Table 4: Test Mode Settings

5.2 Serial Interface Timing

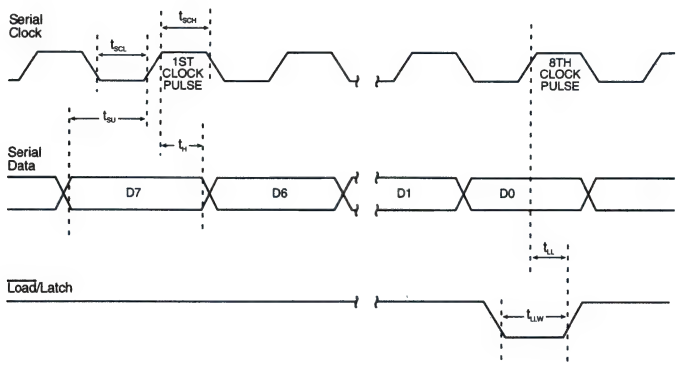


Figure 4: Serial Interface Timing Diagram

Abbreviation	Description	Time
t_{SCH}	Serial Clock high pulse width	50ns min.
t_{SU}	Data set-up time	30ns min.
t_{LL}	$\overline{\text{Load}}$ / Latch set - up time	50ns min.
t_{SCL}	Serial Clock low pulse width	50ns min.
t_H	Data hold time	40ns min.
t_{LLW}	$\overline{\text{Load}}$ / Latch pulse width	80ns min.

Table 5: Serial Interface Timing Specifications

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480121.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

5.3 CODEC

5.3.1 Timing Information

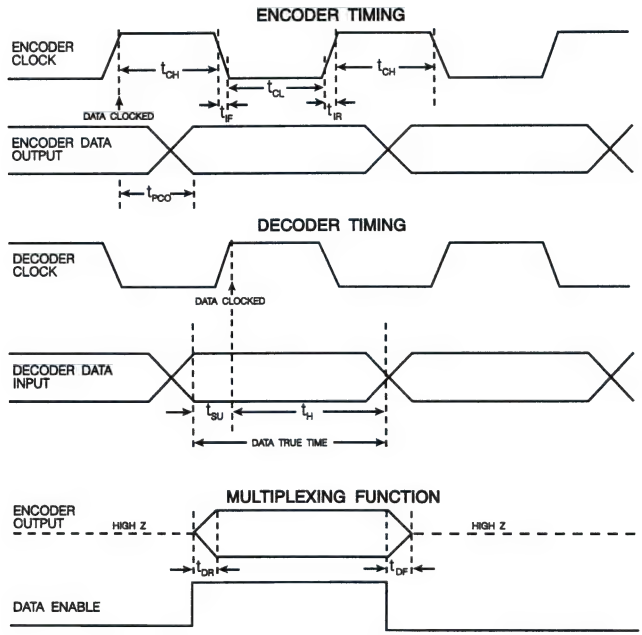


Figure 5: Encode/Decode Timing Diagram

Abbreviation	Description	Time			
		Min.	Typ.	Max.	Units
t_{CH}	Clock pulse width (logic 1)	1.0			µs.
t_{CL}	Clock pulse width (logic 0)	1.0			µs
t_{IR}	Clock rise time		100		ns
t_{IF}	Clock fall time		100		ns
t_{SU}	Data set-up time			450	ns
t_H	Data hold time	600			ns
$t_{SU} + t_H$	Data true time		1.5		µs
t_{PCO}	Clock to output delay time		750		ns
t_{DR}	Data rise time		100		ns
t_{DF}	Data fall time		100		ns
	Xtal input frequency		3.58		MHz

Table 6: Encode/Decode Timing Specifcations

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480121.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

5.3.2 CODEC Performance

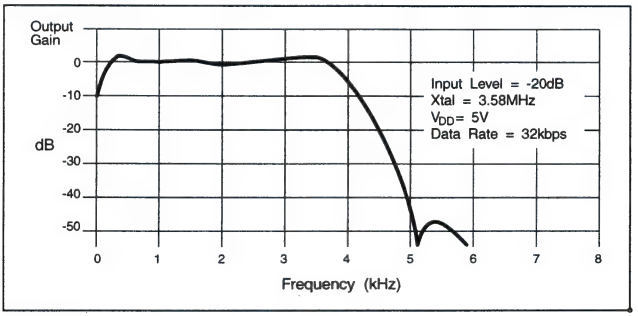


Figure 6: Typical CODEC Frequency Response

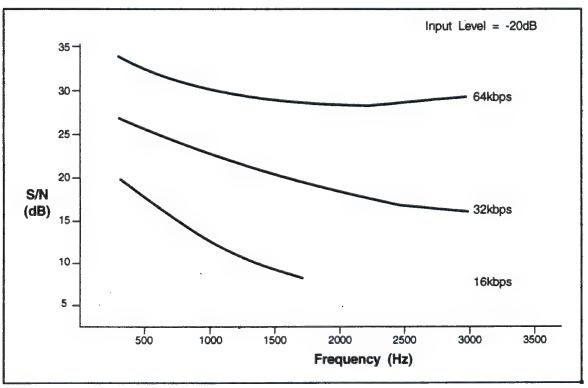


Figure 7: Typical S/N ratio with Input Frequency

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.
Correct operation of the device outside these limits is not implied.

General	Min.	Typ.	Max.	Units
Supply Voltage	-0.3		7.0	V
Input Voltage at any pin to V_{SS}	-0.3		(V_{DD} +0.3)	V
Current				
V_{DD}	-30		30	mA
V_{SS}	-30		30	mA
Any other pins	-20		20	mA
P/DW Packages				
Total Allowable Power Dissipation at T_{AMB} = 25°C			800	mW max.
Derating above 25°C			10	mW/°C above 25°C
Operating Temperature	-30°		70°	°C
Storage Temperature	-40°		85°	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied

	Min.	Max.	Units
V_{DD}	2.7	5.5	V
Operating Temperature	-30	75	°C
Xtal/Clock f_0		3.58	MHz

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480121.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified.

V_{DD} = 5.0V, T_{AMB} = 25°C
Xtal/Clock f_0 = 3.58MHz, Audio Test Frequency = 820Hz
Sample Clock Rate = 32kbps, Audio level 0dB ref. (0dBmO) = 489mV_{RMS}

	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Current			5.0		mA
Logic Levels					
Input Logic "1"		70%V_{DD}			V
Input Logic "0"				30%V_{DD}	V
Output Logic "1"		80%V_{DD}			V
Output Logic "0"				20%V_{DD}	V
Digital Input Impedance					
Logic I/O Pins			10		MΩ
Logic Input Pins, Pullup Resistor	2	300			kΩ
Digital Output Impedance			4		kΩ
Analog Input Impedance			100		kΩ
Analog Output Impedance	5		200		Ω
Insertion Loss	1		0		dB
Dynamic Values V_{DD} = 5.0V					
Encoder:					
Analog Signal Input Levels	5	-30		6	dB
Principal Integrator Frequency			275		Hz
Encoder Filter Passband (3dB)				3800	Hz
Compand Time Constant			4		ms
Decoder:					
Analog Signal Output Levels	5	-33	0	9	dB
Decoder Filter Passband (3dB)	2	250		3800	Hz
Encoder/Decoder (Full Codec):					
Passband		300		3400	Hz
Stopband		6		10	kHz
Stopband Attenuation			60		dB
Passband Gain			0		dB
Passband Ripple		-3		3	dB
Output Noise (Input Short Circuit)	6		-54		dBp
Group Delay Distortion	3				
(1000Hz-2600Hz)				450	µs
(600Hz-2800Hz)				750	µs
(500Hz-3000Hz)				1.5	ms
Xtal/Clock Frequency		3.0	3.58	4.0	MHz

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480121.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Operating Characteristics Notes:

1. All logic inputs except Encoder and Decoder Data Clocks.
2. With passband gain of ±1dB.
3. Group Delay Distortion for the full codec is relative to the delay with an 820Hz, -20dB signal at the encoder input.
4. Relative Timings are shown in Figure 4.
5. Recommended values.
6. Psophometric weighted measurement.

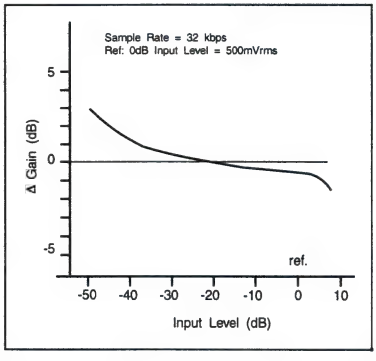


Figure 8: typical Variation of Gain with Input Level

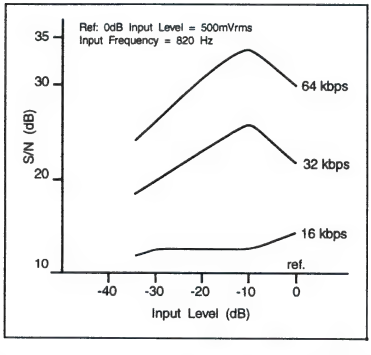
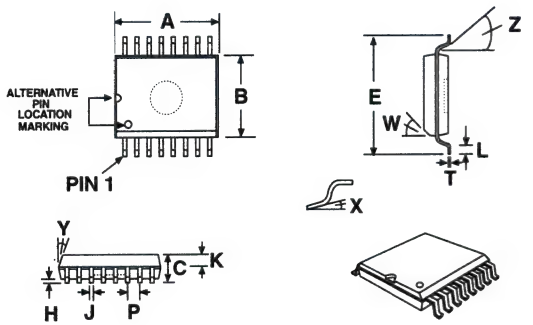


Figure 9: Typical Variation S/N ratio with Input Level

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc. # 20480121.005

6.2 Packaging

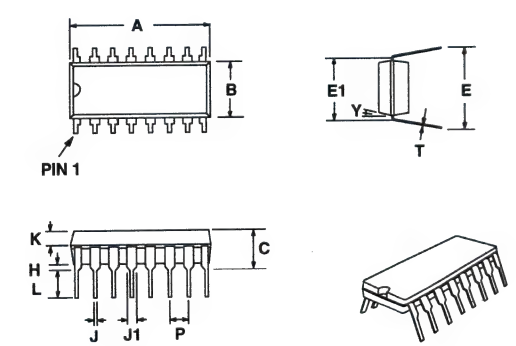


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 16-pin SOIC Mechanical Outline: order as part no. MX109DW



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91)
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 16-pin PDIP Mechanical Outline: order as part no. MX109P

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc. # 20480121.005

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX609

PCN/PCS DELTA MODULATION CODEC

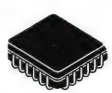
FEATURES

- Single Chip Full Duplex CVSD CODEC
- On-chip Input & Output Filters
- Programmable Sampling Clocks
- 3- or 4-bit Companding Algorithm
- Powersave Capabilities
- Low Power, Single 5V CMOS

APPLICATIONS

- Digital PCN/PCS System
- Digital Cordless Phones
- Digital Delay Lines
- Digital Voice Storage
- Multiplexers, Switches & Phones
- Time Domain Scramblers

MX609J (CDIP)
MX609P (PDIP)
22 pins



MX609LH
24 pin PLCC

MX609DW
16 pin SOIC

Description

The MX609 is a Continuously Variable Slope Delta Modulation (CVSD) Codec designed for use in cordless telephones. The device is suitable for applications in delta multiplexers, switches and phones. Encoder input and decoder output switched capacitor filters are incorporated on-chip.

Sampling clock rates can be programmed to 16, 32 or 64K bits/second from an internal clock generator or externally injected in the 8 to 64K bits/second range. The internal clocks are derived from an on-chip reference oscillator driven by an externally connected crystal. The sampling clock frequency is output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. When not enabled the encoder output remains in a high-impedance "tri-state" mode.

Companding circuits may be operated with an externally selectable 3- or 4-bit algorithm. The device may be put in standby mode when Powersave is selected.

The MX609 is a low-power 5V CMOS device. It is available in PDIP, CDIP, PLCC and SOIC packages.

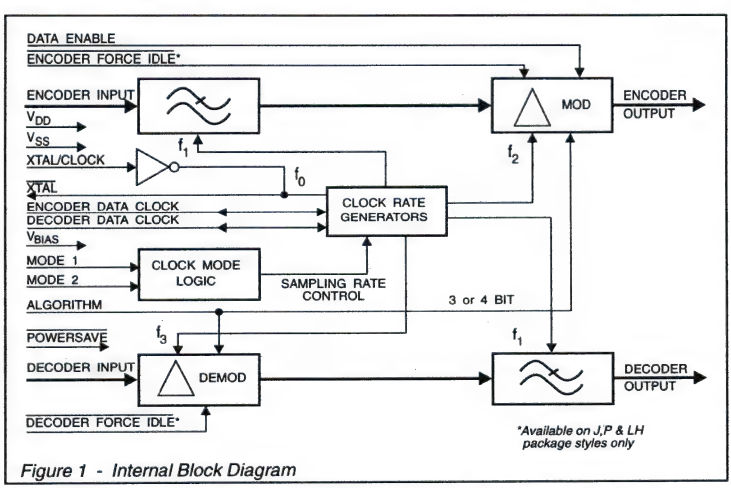


Figure 1 - Internal Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480069.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

PIN FUNCTION CHART

Pin			Function
J/P	LH	DW	
1	1	1	**Xtal/Clock (I/P):** Input to the clock oscillator inverter. A 1.024 MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 3.
	2		N/C
2	3	2	**$\overline{\text{Xtal}}$ (O/P):** The 1.024 MHz output of the clock oscillator inverter.
3	4		N/C
4	5	3	**Encoder Data Clock:** A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependent upon clock mode 1,2 inputs and xtal frequency (see Clock Mode pins).
5	6	4	**Encoder Output:** The encoder digital output. This is a three-state output whose condition is set by the Data Enable and Powersave inputs, as shown below: Data Enable / Powersave / Encoder Output 1 / 1 / Enabled 0 / 1 / High Z (open circuit) 1 / 0 / V_{SS}
6	7	--	**$\overline{\text{Encoder Force Idle}}$:** When this pin is at a logical "0" the encoder is forced to an idle state and the encoder digital output is 0101, a perfect idle pattern. When this pin is a logical "1" the encoder encodes as normal. Internal 1MΩ pullup.
7	8	5	**Data Enable:** Data is made available at the encoder output pin by control of this input. See Encoder Output pin. Internal 1 MΩ pullup.
8	9		N/C
9	10	6	**Bias:** Normally at $V_{DD}/2$ bias, this pin should be externally decoupled by capacitor C_4. Internally pulled to V_{SS} when "Powersave" is a logical "0".
10	11	7	**Encoder Input:** The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 3.
11	12	8	**V_{SS}:** Negative Supply
12	13		N/C
13	14	9	**Decoder Output:** The recovered analog signal is output at this pin. It is the buffered output of a lowpass filter and requires external components. During "Powersave" this output is open circuit.
14	15		N/C
15	16	10	**Powersave:** A logic "0" at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical "1", the codec operates normally. Internal 1 MΩ pullup.
	17		N/C
16	18	--	**$\overline{\text{Decoder Force Idle}}$:** A logic "0" at this pin gates a 0101... pattern internally to the decoder so that the Decoder Output goes to $V_{DD}/2$. When this pin is a logical "1" the decoder operates as normal. Internal 1MΩ pullup.
17	19	11	**Decoder Input:** The received digital signal input. Internal 1 MΩ pullup.
18	20	12	**Decoder Data Clock:** A logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1,2 inputs. See Clock Mode pins.
19	21	13	**Algorithm:** A logic "1" at this pin sets this device for a 3-bit companding algorithm. A logical "0" sets a 4-bit companding algorithm. Internal 1 MΩ pullup.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480069.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Pin			Function
J/P	LH	DW	
20	22	14	**Clock Mode 2:**
21	23	15	**Clock Mode 1:**
			Internal 1 MΩ Pullups.

Clock Mode 1	Clock Mode 2	Facility
0	0	External Clocks
0	1	Internal,64kb/s=f÷16
1	0	Internal,32kb/s=f÷32
1	1	Internal,16kb/s=f÷64

Clock rates refer to f = 1.024MHz Xtal/clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode.

22	24	16	V_{DD}: Positive Supply. A single +5 volt power supply is required.

CODEC INTEGRATION

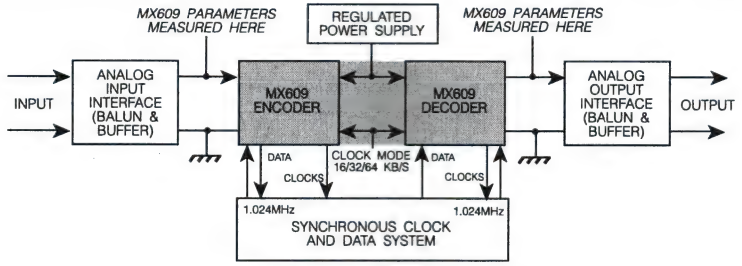
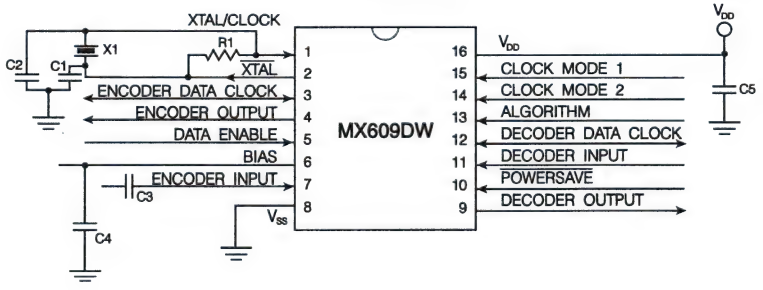


Figure 2 - System Configuration Showing the MX609



Component	Value	Note
R1	1M	Oscillator inverter bias resistor.
C1	33p	Xtal circuit load capacitor.
C2	68p	Xtal circuit load capacitor.
C3	1.0µ	Encoder input coupling capacitor. The drive source impedance to this input should be less than 100Ω. Output idle channel noise levels will improve with an even lower source impedance.
C4	1.0µ	Bias decoupling capacitor.
C5	1.0µ	V_{DD} decoupling capacitor.
X1	1.024MHz	A 1.024 MHz xtal/clock input will yield exactly 16/32/64 kb/s data clock rates. Xtal circuitry shown is in accordance with MX-COM's Xtal Oscillator Application Note (see Appendix).

Figure 3 - Recommeded External Components

Tolerances: Resistors = 10%, Capacitors = 20%.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480069.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

CODEC TIMING INFORMATION

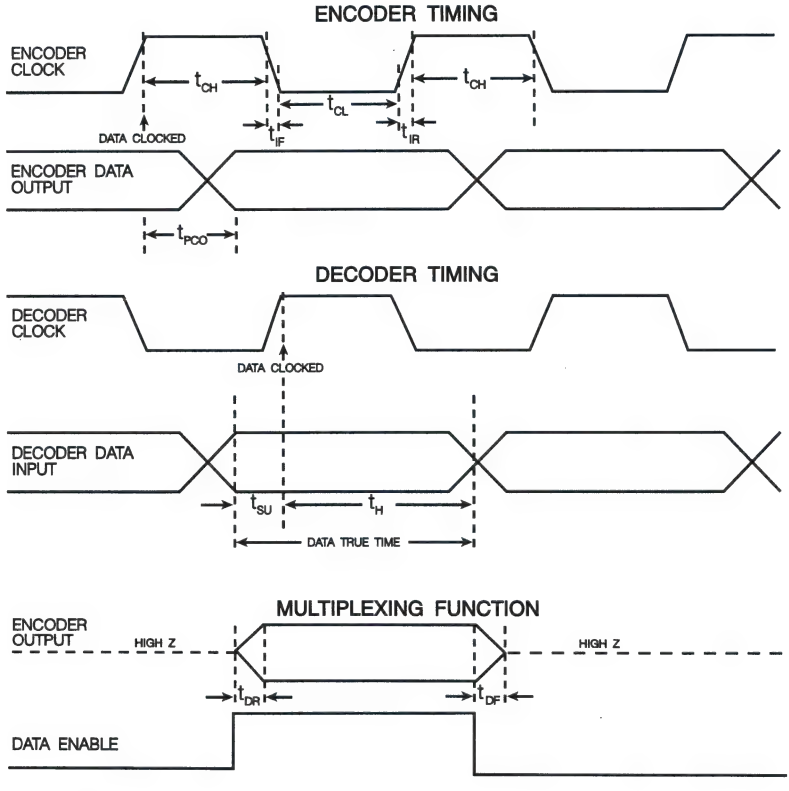


Figure 4 - Codec Timing

Abbreviation	Description	Time
t_{CH}	Clock 1 pulse width	1.0µs min.
t_{CL}	Clock 0 pulse width	1.0µs min.
t_{IR}	Clock rise time	100ns typ.
t_{IF}	Clock fall time	100ns typ.
t_{SU}	Data set-up time	450ns max.
t_H	Data hold time	600ns min.
$t_{SU} + t_H$	Data true time	1.5µs typ.
t_{PCO}	Clock to output delay time	750ns typ.
t_{DR}	Data rise time	100ns typ.
t_{DF}	Data fall time	100ns typ.
	Xtal input frequency	1.024MHz

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480069.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

CODEC PERFORMANCE

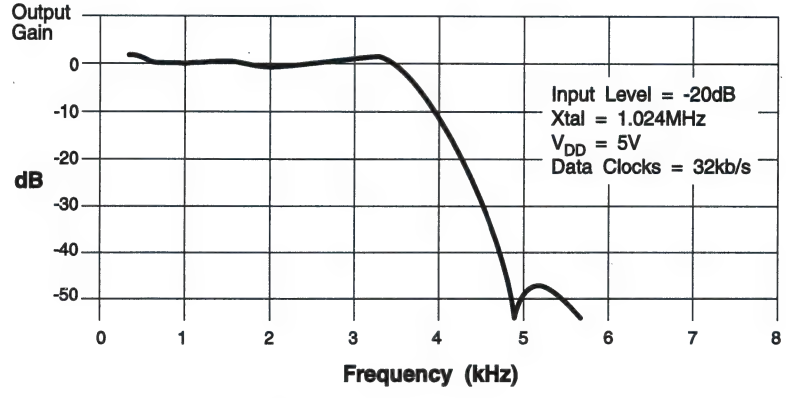


Figure 5 - Typical Codec Frequency Response

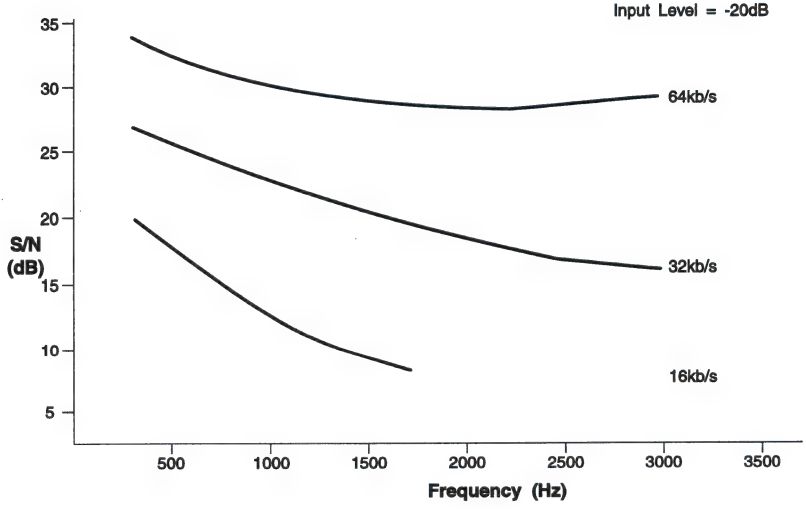


Figure 6 - Typical S/N Ratio with Input Frequency

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480069.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{ss}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current (Supply)	±30mA
(Other Pins)	±20mA
Total Device Dissipation (@ T_{amb}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-30°C to +70°C
Storage Temperature	-40°C to +85°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

Audio Test Frequency = 820Hz

T_{AMB} = 25°C

Sample Clock Rate = 32 kb/sec

Xtal/Clock f_o = 1.024MHz

Audio level 0dB ref (0 dBm0) = 489mVrms

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)		-	3.5	-	mA
Supply Current (Powersave)		-	500	-	µA
Input Logic "1"		3.5	-	-	V
Input Logic "0"		-	-	1.5	V
Output Logic "1"		4.0	-	-	V
Output Logic "0"		-	-	1.0	
Digital Input Impedance					
Logic I/O Pins		-	10	-	MΩ
Logic Input Pins, Pullup Resistor	2	300	-	-	kΩ
Digital Output Impedance		-	4	-	kΩ
Analog Input Impedance		-	100	-	kΩ
Analog Output Impedance	6	-	800	-	Ω
Three State Output Leakage		-	±4	-	µA
Insertion Loss	2	-	0	-	dB
Dynamic Values	1				
Encoder:					
Analog Signal Input Levels	6	-30	-	+8	dB
Principal Integrator Frequency		-	275	-	Hz
Encoder Passband		-	3400	-	Hz
Compand Time Constant		-	4	-	ms
Decoder:					
Analog Signal Output Levels	6	-30	0	+8	dB
Decoder Passband	3	-	3400	-	Hz
Encoder Decoder (Full Codec):					
Passband		300	-	3400	Hz
Stopband		6	-	10	KHz
Stopband Attenuation		-	60	-	dB
Passband Gain		-	0	-	dB
Passband Ripple		-3	-	+3	dB
Output Noise (Input Short Circuit)		-	-60	-	dB
Perfect Idle Channel Noise (Encode Forced)	7	-	-63	-	dB
Group Delay Distortion	4				
(1000Hz-2600Hz)		-	-	450	µs
(600Hz-2800Hz)		-	-	750	µs
(500Hz-3000Hz)		-	-	1.5	ms
Xtal/Clock Frequency		500	1024	1500	kHz

NOTES:

1. Dynamic characteristics specified at 5V only.
2. All logic inputs except Encoder and Decoder Data Clocks.
3. With passband gain of ±1dB.
4. Group Delay Distortion for the full codec is relative to the delay with an 820Hz, -20dB signal at the encoder input.
5. Relative Timings are shown in Figure 4.
6. Recommended values.
7. Forced Idle Encode/Decode not available on DW package.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480069.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

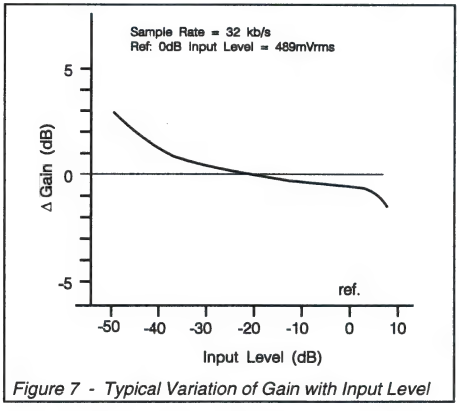


Figure 7 - Typical Variation of Gain with Input Level

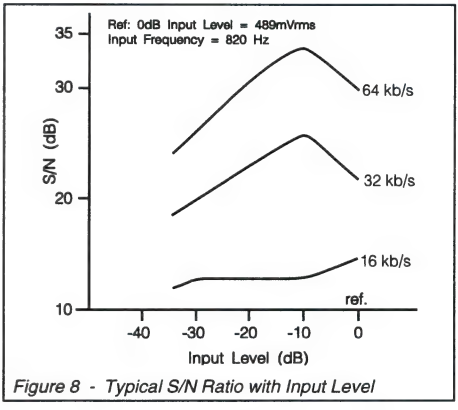
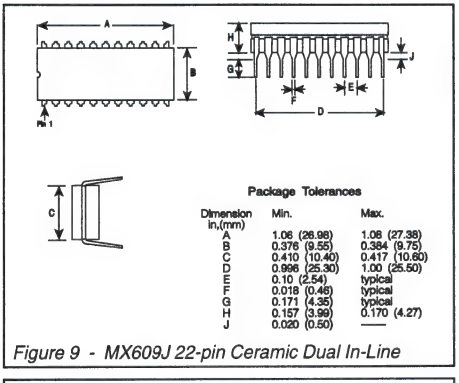


Figure 8 - Typical S/N Ratio with Input Level

Package Outline

The MX609 packages available are shown below. Pin 1 is indicated by an indent spot. Pins number counter-clockwise when viewed from the top.



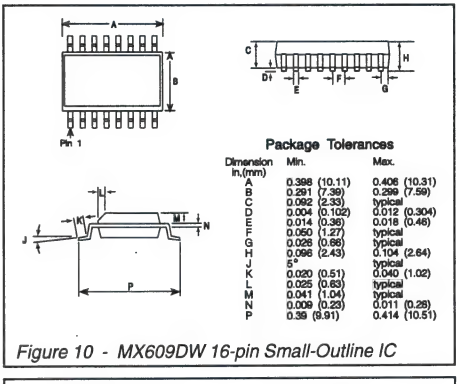
Package Tolerances

Dimension in.(mm)	Min.	Max.
A	1.06 (26.98)	1.08 (27.38)
B	0.376 (9.55)	0.384 (9.75)
C	0.410 (10.40)	0.417 (10.60)
D	0.996 (25.30)	1.00 (25.50)
E	0.10 (2.54)	typical
F	0.018 (0.46)	typical
G	0.171 (4.35)	typical
H	0.157 (3.99)	0.170 (4.27)
J	0.020 (0.50)	—

Figure 9 - MX609J 22-pin Ceramic Dual In-Line

Handling Precautions

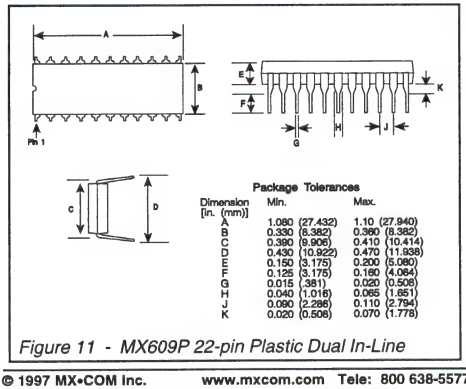
The MX609 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.



Package Tolerances

Dimension in.(mm)	Min.	Max.
A	0.398 (10.11)	0.406 (10.31)
B	0.291 (7.39)	0.299 (7.59)
C	0.092 (2.33)	typical
D	0.004 (0.102)	0.012 (0.304)
E	0.014 (0.36)	0.018 (0.46)
F	0.050 (1.27)	typical
G	0.026 (0.66)	typical
H	0.096 (2.43)	0.104 (2.64)
J	5°	typical
K	0.020 (0.51)	0.040 (1.02)
L	0.025 (0.63)	typical
M	0.041 (1.04)	typical
N	0.009 (0.23)	0.011 (0.28)
P	0.39 (9.91)	0.414 (10.51)

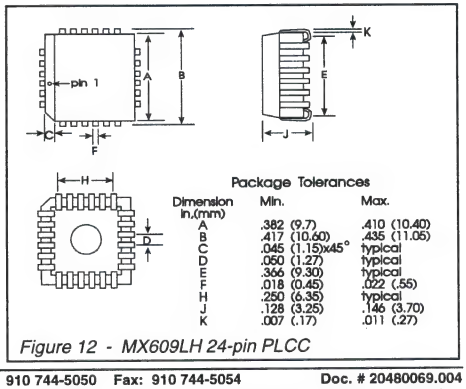
Figure 10 - MX609DW 16-pin Small-Outline IC



Package Tolerances

Dimension [in. (mm)]	Min.	Max.
A	1.080 (27.432)	1.10 (27.940)
B	0.330 (8.382)	0.380 (8.382)
C	0.390 (9.906)	0.410 (10.414)
D	0.430 (10.922)	0.470 (11.938)
E	0.150 (3.175)	0.200 (5.080)
F	0.125 (3.175)	0.160 (4.064)
G	0.015 (.381)	0.020 (0.508)
H	0.040 (1.016)	0.065 (1.651)
J	0.090 (2.286)	0.110 (2.794)
K	0.020 (0.508)	0.070 (1.778)

Figure 11 - MX609P 22-pin Plastic Dual In-Line



Package Tolerances

Dimension in.(mm)	Min.	Max.
A	.382 (9.7)	.410 (10.40)
B	.417 (10.60)	.435 (11.05)
C	.045 (1.15)x45°	typical
D	.050 (1.27)	typical
E	.366 (9.30)	typical
F	.018 (0.45)	.022 (.55)
H	.250 (6.35)	typical
J	.128 (3.25)	.146 (3.70)
K	.007 (.17)	.011 (.27)

Figure 12 - MX609LH 24-pin PLCC

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480069.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX619/629

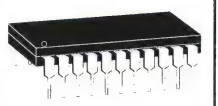
DELTA MODULATION CODEC

FEATURES

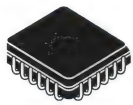
- MX619 Meets EUROCOM D1-IA8
- MX629 Meets Mil-Std-188-113
- Single Chip Full Duplex CODEC
- On-chip Input & Output Filters
- Programmable Sampling Clocks
- 3- or 4-bit Companding Algorithm
- Forced Idle & Powersave

APPLICATIONS

- Military Communications
- Multiplexers, Switches & Phones



MX619J
MX629J
22-pin CDIP



MX619LH
MX629LH
24-lead PLCC

DESCRIPTION

The MX619 and MX629 are Continuously Variable Slope Delta Modulation (CVSD) Codecs designed for use in military communications systems. The device is suitable for applications in military Delta Multiplexers, switches and phones. The MX619 is designed to meet EUROCOM D1-IA8. The MX629 is designed to meet Mil-Std-188-113.

Encoder input and decoder output filters are incorporated on-chip. Sampling clock rates can be programmed to 16, 32 or 64K bits/second from an internal clock generator or externally injected in the 8 to 64K bits/second range. Sampling clock frequencies are output for the synchronization of external circuits.

The encoder has an enable function for use in multiplexer applications. Encoder and Decoder forced idle capabilities are provided forcing a 10101010... pattern in encode and a $V_{DD}/2$ bias in decode. The companding circuits may be operated with an externally selectable 3- or 4-bit algorithm. The device may be put in standby mode by selecting Powersave. A reference 1.024MHz oscillator uses an external clock or crystal. The MX619 and MX629 are low-power 5V CMOS devices available in a 22-pin CDIP package or a 24-lead PLCC package.

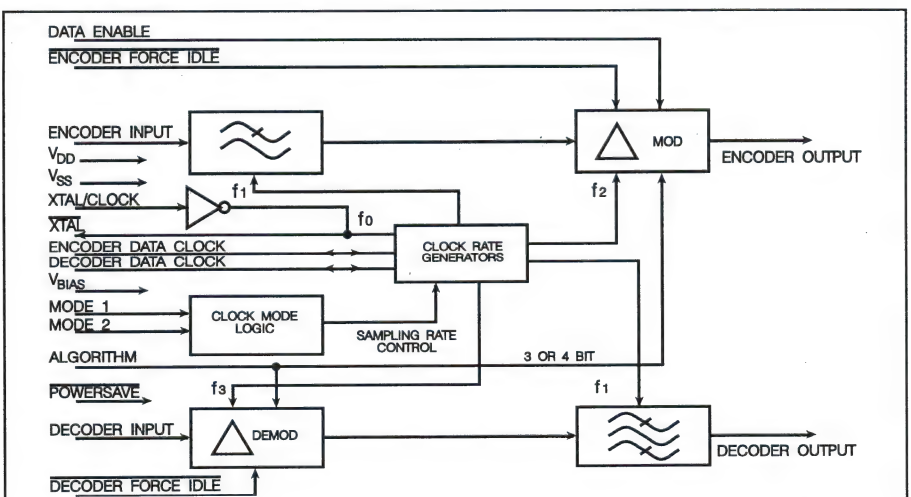


Figure 1 - Internal Block Diagram

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road Winston-Salem, NC 27105-1201 USA
Doc.# 20480008.004
All trademarks and service marks are held by there respective companies.

PIN FUNCTION TABLE

Pin J	Pin LH	Function
1	1	Xtal/Clock (I/P): Input to the clock oscillator inverter. A 1.024 MHz Xtal input or externally derived clock is injected here. See Clock Mode pins and Figure 3.
	2	No Connection.
2	3	$\overline{\text{Xtal}}$ (O/P): The 1.024 MHz output of the clock oscillator inverter.
3	4	No Connection.
4	5	Encoder Data Clock: A logic I/O port. External encode clock input or internal data clock output. Clock frequency is dependent upon clock mode 1 and 2 inputs and xtal frequency (see Clock Mode pins).
5	6	Encoder Output: The encoder digital output. This is a three-state output whose condition is set by the Data Enable and Powersave inputs, as shown below:
6	7	$\overline{\text{Encoder Force Idle}}$: When this pin is a logical "0", the encoder is forced to an idle state and the encoder digital output is 0101..., a perfect idle pattern. When this pin is a logical "1", the encoder encodes as normal. This pin has an internal 1 MΩ pullup.
7	8	Data Enable: Data is made available at the encoder output pin by control of this input. See Encoder Output pin. This pin has an internal 1 MΩ pullup.
8	9	No Connection
9	10	Bias: Normally at $V_{DD}/2$ bias, this pin should be externally decoupled by capacitor C_4. Internally pulled to V_{SS} when "Powersave" is a logical "0".
10	11	Encoder Input: The analog signal input. Internally biased at $V_{DD}/2$, this input requires an external coupling capacitor. The source impedance should be less than 100Ω. Output channel noise levels will improve with an even lower source impedance. See Figure 3.
11	12	V_{SS}: Negative Supply.
12	13	No Connection.
13	14	Decoder Output: The recovered analog signal is output at this pin. It is the buffered output of a bandpass filter and requires external components. During "Powersave" this output is o/c.
14	15	No Connection.
15	16	$\overline{\text{Powersave}}$: A logical "0" at this pin puts most parts of the codec into a quiescent non-operational state. When at a logical "1", the codec operates normally. This pin has an internal 1 MΩ pullup.

Data Enable	$\overline{\text{Powersave}}$	Encoder Output
1	1	Enabled
0	1	High Z (o/c)
1	0	V_{SS}

© 1996 MX•COM,INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480008.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Pin J	Pin LH	Function
	17	No Connection
16	18	Decoder Force Idle: A logical "0" at this pin gates a 0101... pattern internally to the decoder so that the decoder output goes to $V_{DD}/2$. When this pin is at a logical "1", the decoder operates as normal. This pin has an internal 1 MΩ pullup.
17	19	Decoder Input: The received digital signal input. This pin has an internal 1 MΩ pullup.
18	20	Decoder Data Clock: A logic I/O port. External decode clock input or internal data clock output, dependent upon clock mode 1,2 inputs. See Clock Mode pins.
19	21	Algorithm: A logical "1" at this pin sets this device for a 3-bit companding algorithm. A logical "0" sets a 4-bit companding algorithm. This pin has an internal 1 MΩ pullup.
20 21	22 23	Clock Mode 2: Clock Mode 1: *Internal 1 MΩ Pullups.* Clock rates refer to f = 1.024MHz Xtal/clock input. During internal operation the data clock frequencies are available at the ports for external circuit synchronization. Independent or common data rate inputs to Encode and Decode data clock ports may be employed in the External Clocks mode. Optimum performance will be achieved when the applied external clocks are synchronous with the master Xtal/clock, and a sub-multiple of 128kHz.
22	24	V_{DD}: Positive Supply. A single +5 volt power supply is required.

Clock Mode 1	Clock Mode 2	Facility
0	0	External Clocks
0	1	Internal, 64kb/s = f/16
1	0	Internal, 32kb/s = f/32
1	1	Internal, 16kb/s = f/64

Application Recommendations

Due to the very low levels of signal idle channel noise specified for military applications, a noisy or badly regulated power supply could cause instability, putting the overall system performance out of specification. Adherence to the points listed below will assist in minimizing this problem.

(a) Care should be taken in the design and layout of the printed circuit board.

(b) All external components (as recommended in Figure 3) should be kept close to the package.

(c) Tracks should be kept short, particularly the Encoder Input capacitor and the V_{BIAS} capacitor.

(d) Xtal/clock tracks should be kept well away from analog inputs and outputs.

(e) Inputs and outputs should be screened whenever possible.

(f) A "ground plane" connected to V_{SS} will assist in eliminating external pick-up on the input and output pins.

(g) It is recommended that the power supply rails have less than 1mVrms of noise allowed.

(h) The source of impedance to the Encoder Input pin must be less than 100Ω; Output Idle channel noise levels will improve with even lower source impedances.

© 1996 MX•COM,INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480008.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

CODEC Integration

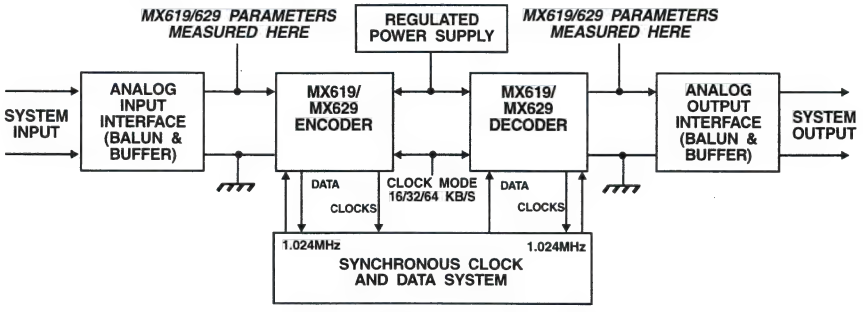
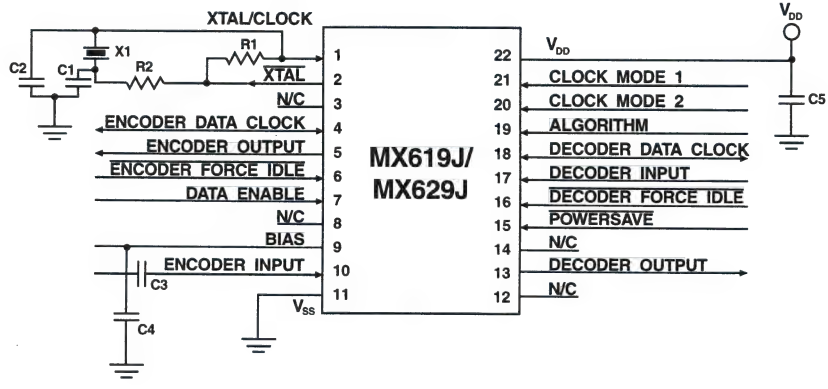


Figure 2 - System Configuration showing the MX619/MX629, which with the indicated interfacing will conform to the EUROCOM D1-IA8 or Mil-Std-188-113 specification, respectively.



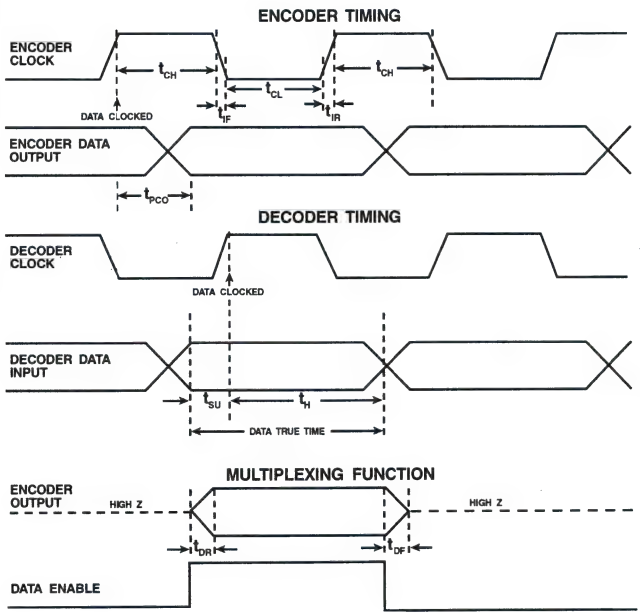
Component	Unit Value	Note
R_1	1M	Oscillator Inverter bias resistor.
R_2	Selectable	Xtal Drive limiting resistor.
C_1	33p	Xtal Circuit load capacitor.
C_2	33p	Xtal Circuit load capacitor.
C_3	1.0µ	Encoder Input coupling capacitor. The drive source impedance to this input should be less than 100Ω. Output Idle channel noise levels will improve with an even lower source impedance.
C_4	1.0µ	Bias decoupling capacitor.
C_5	1.0µ	V_{DD} decoupling capacitor.
X_1	1.024MHz	A 1.024 MHz Xtal/clock input will yield exactly 16/32/64 kb/s data clock rates.

Tolerance: Resistors ± 10%, Capacitors ± 20%

Figure 3 - Recommended External Components

© 1996 MX•COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc.# 20480008.004
All trademarks and service marks are held by there respective companies.

CODEC Timing Information



TIMING

t_{CH}: Clock 1 Pulse Width
1.0µs min.

t_{CL}: Clock 0 Pulse Width
1.0µs min.

t_{IR}: Clock Rise Time
100ns typ.

t_{IF}: Clock Fall Time
100ns typ.

t_{SU}: Data Set-Up Time
450ns max.

t_H: Data Hold Time
600ns min.

$t_{SU} + t_H$: Data True Time

t_{PCO}: Clock to Output
Delay Time. 750ns max.

t_{DR}: Data Rise Time
100ns typ.

t_{DF}: Data Fall Time
100ns typ.

XTAL Input Frequency:
1.024 MHz

Figure 4 - CODEC Timing Diagrams

© 1996 MX•COM,INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480008.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Codec Performance (MX619)

Using the Bit Sequence Tests (a - g) at the Decoder Input pin in accordance with the Eurocom Specification D1-IA8, the decoder output is as shown in Table 1.

Test	Sample Rate	Bit Sequence at Decoder Input	MLA Duty Cycle	Typical Output Level
a.	16kbit/s	1011010010010010 1101	0	-41.5dBm0
	32kbit/s	1011011010101001001001001001010101101101	0	-42.0dBm0
b.	16kbit/s	1101100100100 1101	0.05	-25.0dBm0
	32kbit/s	1011011010101001001000100100101011011011	0.05	-25.0dBm0
c.	16kbit/s	1011010100010010 1011	0.1	-19.0dBm0
	32kbit/s	1101101101010010001000100100101011011101	0.1	-18.5dBm0
d.	16kbit/s	1101100100001001 1011	0.2	-11.0dBm0
	32kbit/s	1101110110010100010000100010011010111011	0.2	-11.5dBm0
e.	16kbit/s	1101101000001001 0111	0.3	-6.5dBm0
	32kbit/s	1110111011001000100000010010011011 10111	0.3	-6.5dBm0
f.	16kbit/s	1101101000000100 1111	0.4	-3.0dBm0
	32kbit/s	1111011101010001000000001000101011101111	0.4	-3.0dBm0
g.	16kbit/s	1110101000000001 0111	0.5	0dBm0
	32kbit/s	1111101110100010000000000100010111011111	0.5	0dBm0

Table 1 - Bit Sequence Test Table

Digital to Analog Performance (MX629)

Using the bit sequence tests shown in Table 2 (below) at the Decoder Input pin, the analog signals measured at the Decoder Output pin are 800 Hz ± 10 Hz at the levels described.

Sample Rate	Bit Sequence at Decoder Input	"Run of Threes" (%)	Output Level (dBm0)
16 kbit/s	1101101101001001 0010	0	-29.2 ± 2
32 kbit/s	1101101101010100100100100100101010110110	0	-30.0 ± 2
16 kbit/s	1111101101000001 0010	30	0 ± 1
32 kbit/s	1111110110101010000100000010010101011110	30	0 ± 1
			at 800 Hz

Table 2 - Bit Sequence Tests and Results (MX629)

© 1996 MX•COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc.# 20480008.004

MX619 Codec Performance...

relative to the EUROCOM D1-IA8 Specification

MX629 Codec Performance...

relative to the Mil-Std-188-113 Specification

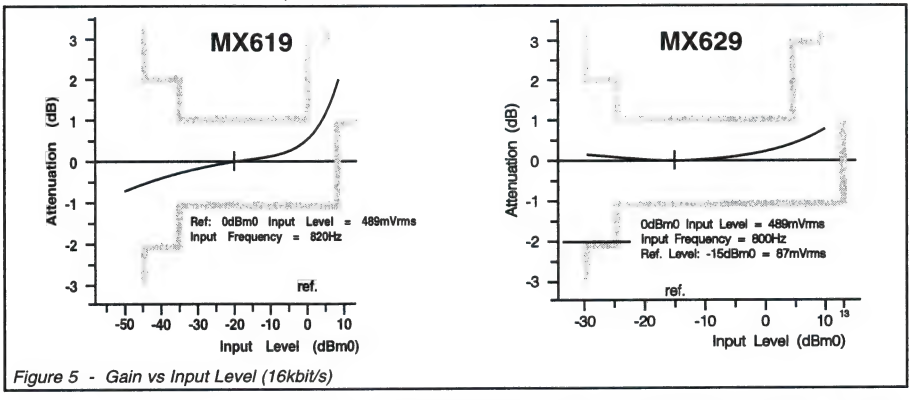


Figure 5 - Gain vs Input Level (16kbit/s)

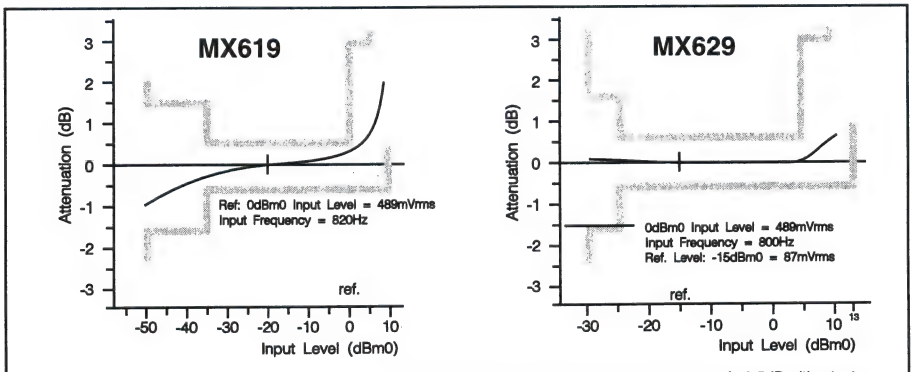


Figure 6 - Gain vs Input Level (32kbit/s)

Note: Spec of ±1dB sums a Mil-Std-188-113 spec of ±0.5dB with a test measurement limitation of ±0.5dB (with 0dB = 87mVrms, 0.5dB = 1.2mVrms).

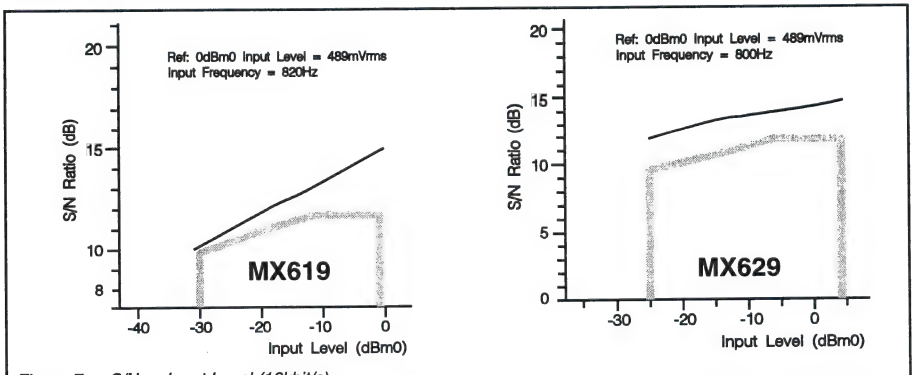


Figure 7 - S/N vs Input Level (16kbit/s)

© 1996 MX•COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc.# 20480008.004
All trademarks and service marks are held by there respective companies.

MX619 Codec Performance...

relative to the EUROCOM D1-IA8 Specification

MX629 Codec Performance...

relative to the Mil-Std-188-113 Specification

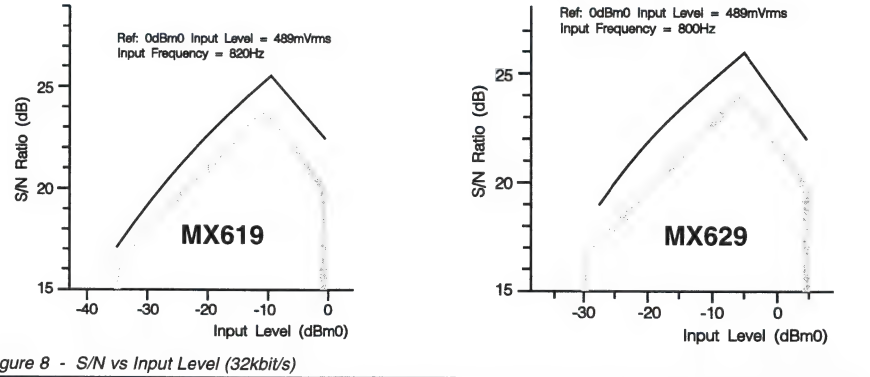


Figure 8 - S/N vs Input Level (32kbit/s)

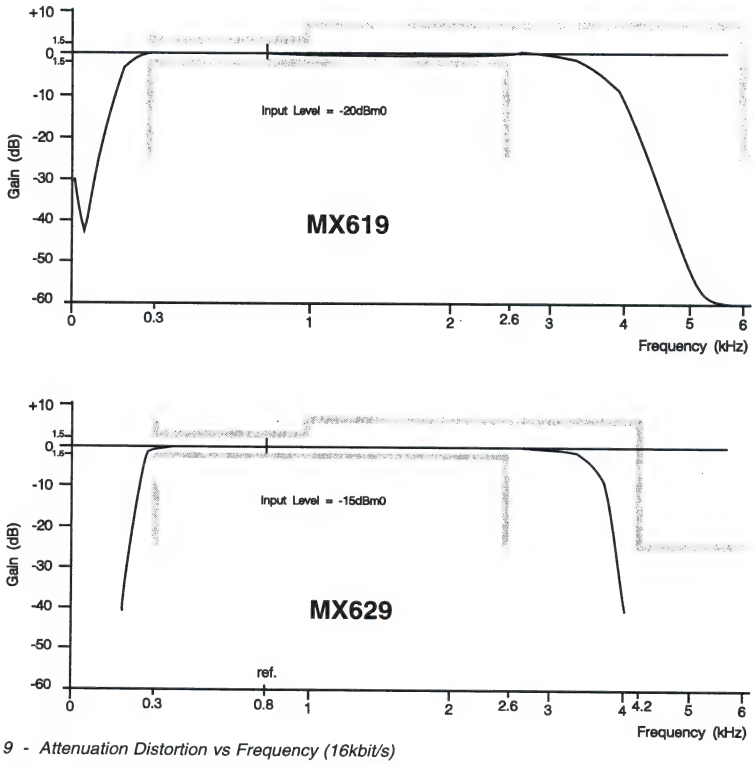


Figure 9 - Attenuation Distortion vs Frequency (16kbit/s)

© 1996 MX•COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc.# 20480008.004
All trademarks and service marks are held by there respective companies.

MX619 Codec Performance...

relative to the EUROCOM D1-IA8 Specification

MX629 Codec Performance...

relative to the Mil-Std-188-113 Specification

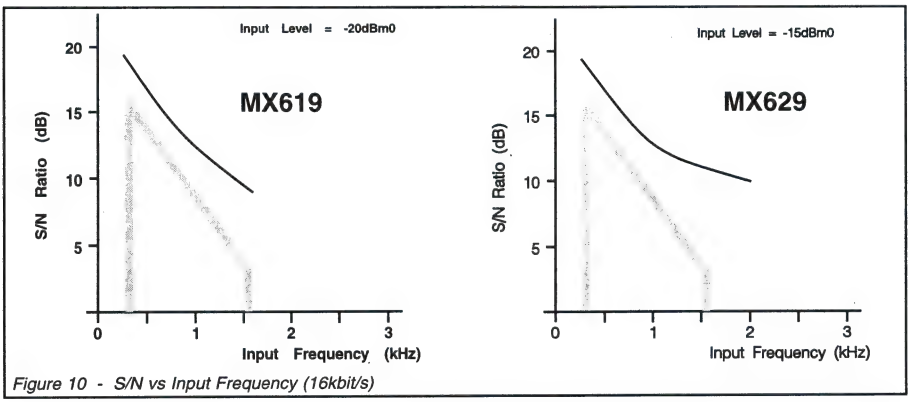


Figure 10 - S/N vs Input Frequency (16kbit/s)

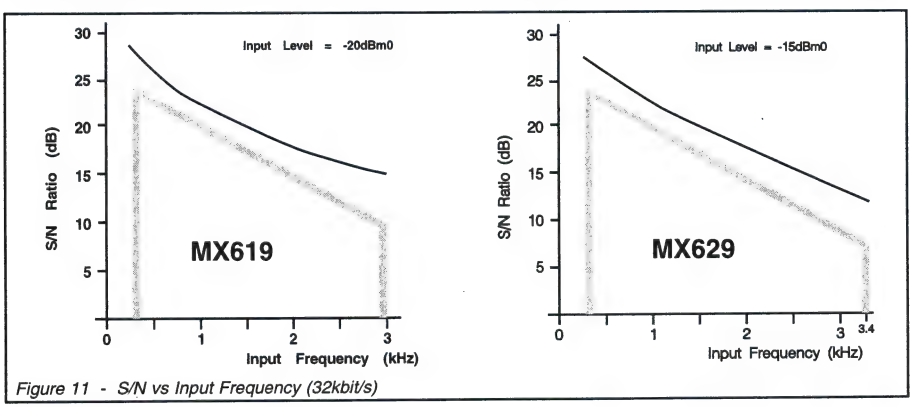


Figure 11 - S/N vs Input Frequency (32kbit/s)

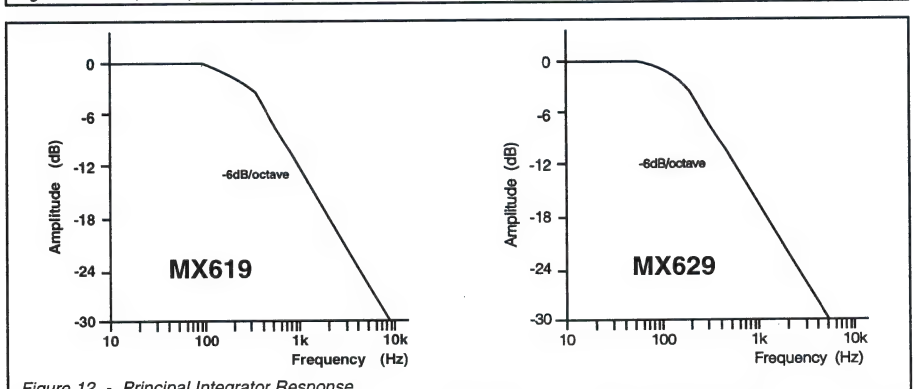


Figure 12 - Principal Integrator Response

© 1996 MX•COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc.# 20480008.004
All trademarks and service marks are held by there respective companies.

MX619 Codec Performance...

relative to the EUROCOM D1-IA8 Specification

MX629 Codec Performance...

relative to the Mil-Std-188-113 Specification

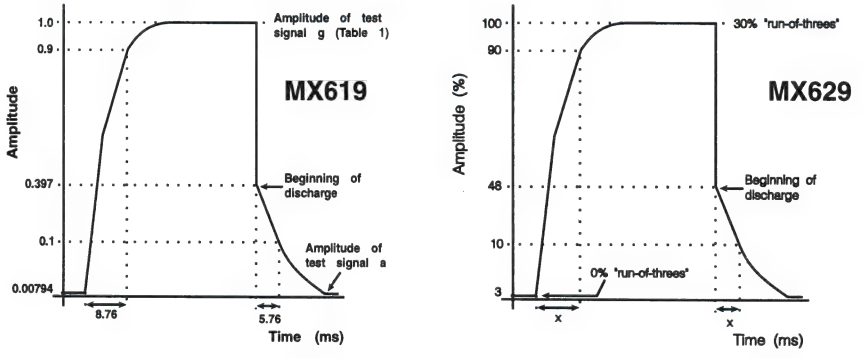


Figure 13 - Compand Envelope

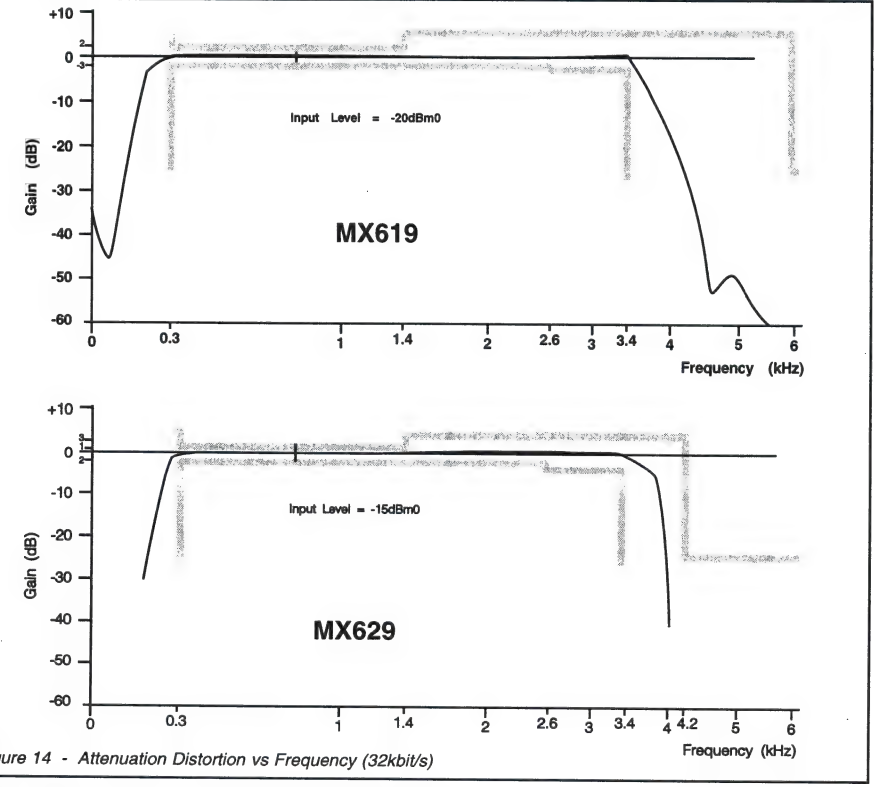


Figure 14 - Attenuation Distortion vs Frequency (32kbit/s)

© 1996 MX•COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc.# 20480008.004
All trademarks and service marks are held by there respective companies.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current: supply pins	±30mA
other pins	±20mA
Total Device Dissipation @ T_{AMB} = 25°C	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Audio Test Frequency = 800 Hz (MX619)
820 Hz (MX629)

Sample Clock Rate = 32kb/sec

Xtal/Clock f_0 = 1.024 MHz

3-bit Compand Algorithm

Audio Level 0dB ref. (0 dBmO) = 489 mVrms

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage	1	4.5	5.0	5.5	V
Supply Current (Enabled)					
MX619		-	4.5		mA
MX629		-	5.5	-	mA
Supply Current (Powersave)					
MX619		-	1.0	-	mA
MX629		-	0.4	-	mA
Input Logic "1"	8	3.5	-	-	V
Input Logic "0"	8	-	-	1.5	V
Output Logic "1"	8	4.0	-	-	V
Output Logic "0"	8	-	-	1.0	
Digital Input Impedance					
Logic I/O Pins		1.0	10	-	MΩ
Logic Input Pins, Pullup Resistor	2	300	-	-	kΩ
Digital Output Impedance					
MX619		-	4	-	kΩ
MX629		-	-	4	kΩ
Analog Input Impedance	4	-	1	-	kΩ
Analog Output Impedance	7	-	-	800	Ω
Three State Output Leakage Current (output disabled)		-4	-	+4	µA
Insertion Loss	3	-2	-	+2	dB
Dynamic Values	1,9				
Encoder:					
Analog Signal Input Levels					
MX619	5,9	-35	-	+6	dBmO
MX629	5,9	-35	-	+12	dBmO
Principal Integrator Frequency					
MX619		-	275	-	Hz
MX629		127	159	212	Hz

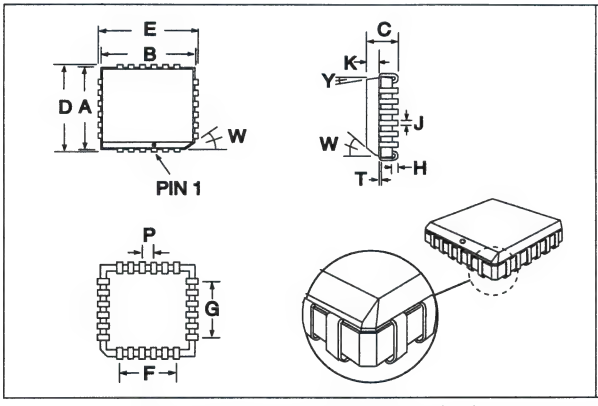
© 1996 MX•COM,INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480008.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Encoder Passband		-	3400	-	Hz
Compand Time Constant					
MX619		-	4	-	ms
MX629		4.0	5.0	6.0	ms
Decoder:					
Analog Signal Output Levels					
MX619	5,9	-35	-10	+6	dBmO
MX629	5,9	-35		+12	dBmO
Decoder Passband		300	-	3400	Hz
Encoder Decoder (Full Codec)					
Compression Ratio					
MX619 (Cd=0.5 to Cd=0.0)		50	-	-	
MX629 (Cd=0.3 to Cd=0.0)		-	16:1	-	
Passband		300	-	3400	Hz
Stopband					
MX619		6	-	10	kHz
MX629		4.2	-	-	kHz
Stopband Attenuation					
MX619		-	60	-	dB
MX629 (4200Hz to 6000Hz)		25	-	-	dB
(>6kHz)		-	60	-	dB
Passband Gain		-	0	-	dB
Passband Ripple (300Hz-1400Hz)		-1	-	+1	dB
(1400Hz-2600Hz)		-1	-	+3	dB
(2600Hz-3400Hz)		-2	-	+3	dB
Output Noise (Input Short Circuit)					
MX619	9	-	-	-60	dBmOp
MX629	9	-	-55	-	dBmO
Perfect Idle Channel Noise (Encoder Forced)					
MX619	-	-	-63	-	dBmOp
MX629	9	-	-57	-	dBmO
Group Delay Distortion (1000Hz-2600Hz)	6	-	-	450	µs
(600Hz-2800Hz)	6	-	-	750	µs
(500Hz-3000Hz)	6	-	-	1.5	ms
Xtal/Clock Frequency		-	1024	-	kHz

NOTES:

1. Dynamic characteristics are specified at 5V unless otherwise specified.
2. All logic inputs except Encoder and Decoder Data Clocks.
3. For an Encoder/Decoder combination, Insertion Loss contributed by a single component is half this figure.
4. Driven with a source impedance of <100 Ω.
5. Recommended values - See Figures 5, 6, 7 and 8.
6. Group Delay Distortion for the full codec is relative to the delay with an 820Hz, -20dB signal at the encoder input.
7. An Emitter Follower output stage.
8. 4V = 80% V_{DD}, 3.5V = 70% V_{DD}, 1.5V = 30% V_{DD}, 1V = 20%V_{DD}.
9. Analog Voltage Levels used: 0dBmO = 489mVrms = -4dBm = 0dB. -15dBmO = 87mVrms. -20dBmO = 49mVrms = -24dBm.

© 1996 MX•COM,INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480008.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

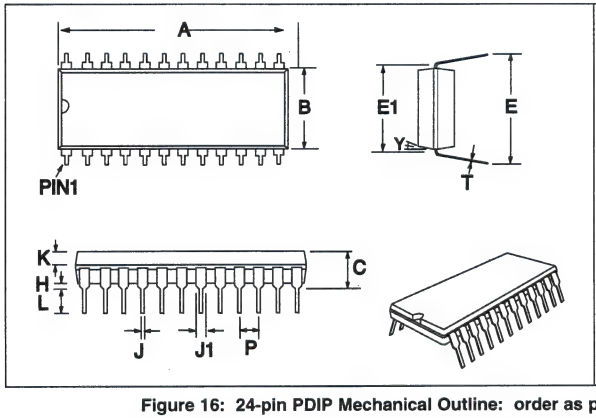


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 24-pin PLCC Mechanical Outline: order as part no. MX619/629LH

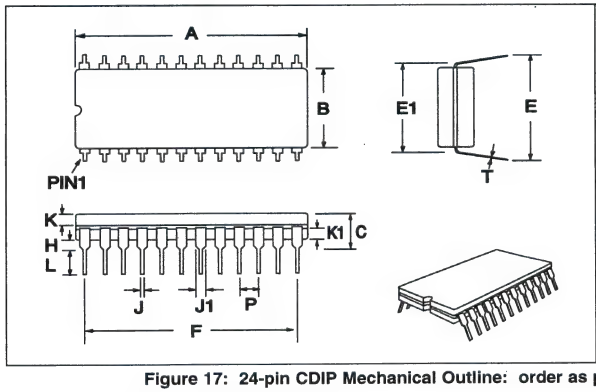


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 24-pin PDIP Mechanical Outline: order as part no. MX619/629P



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 17: 24-pin CDIP Mechanical Outline: order as part no. MX619/629J

© 1996 MX•COM,INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA Doc.# 20480008.004
All trademarks and service marks are held by there respective companies.

MX·COM, INC. MiXed Signal ICs

DATA BULLETIN

MX802 DVSR CODEC

C-BUS COMPATIBLE

Description

The MX802 Data/Voice Storage and Retrieval (DVSR) Codec contains a Continuosly Variable Slope Delta Modulation (CVSD) encoder and decoder, as well as control and timing circuitry for up to 4 Mbits of external DRAM. As a member of the DBS 800 series, it also contains interface and control logic for the "C-BUS" serial interface.

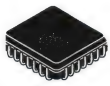
When used with external DRAM, the MX802 has four primary functions:

- **Speech Storage**
  Speech signals present at the Audio Input may be digitized by the CVSD encoder. The resulting bit stream is stored in DRAM. This process also provides readings of the speech signal power level. These readings are used by the system microcontroller for pause reduction.
- **Speech Playback**
  Digitzed speech may be read from DRAM and converted back into analog form by the CVSD decoder.
- **Data Storage**
  Digital data derived via the C-BUS from the Modem or system data may be stored in DRAM.
- **Data Retrieval**
  Digital data may be read from DRAM and sent over the C-BUS to the system microcontroller.

Speech storage and playback may be performed concurrently with data storage or retrieval.

MX802J
28-pin CDIP

MX802LH
PLCC-24



MX802LH8
PLCC-28

The MX802 may also be used without DRAM (as a "stand alone" CVSD codec), in which case direct access is provided to the CVSD Codec digital data and clock signals. All functions are controlled by C-BUS commands from the system microcontroller.

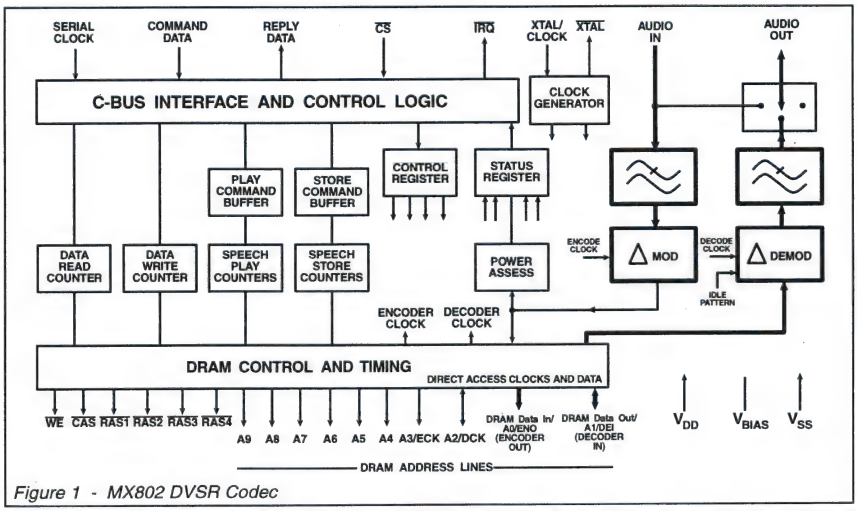


Figure 1 - MX802 DVSR Codec

© 1997 MX-COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480033.007

The storage, recovery and replay functions of the MX802 can be used for:

- •Answering Machine applications, where an incoming speech message is stored for later recall.
- •Busy Buffering, in which an outgoing speech message is stored temporarily until the TX channel becomes free.
- •Automatic transmission of pre-recorded alarm or status announcements.
- •Time Domain Scrambling of speech messages.
- •VOX control of transmitter functions.
- •Temporary Data Storage applications, such as buffering of over-air data transmissions.

On-chip the Delta Codec is supported by input and output analog switched-capacitor filters and audio output switching circuitry. The DRAM control and timing circuitry provides all the necessary address, control and refresh signals to interface to external DRAM.

The MX802 is a low-power 5-volt CMOS LSI device. It is offered in 24- and 28-lead SMT packages, as well as 28-pin DIP packages.

Pin Function Chart

Pin		Function
J/LH8	LH	
1		**Row Address Strobe 2 ($\overline{RAS2}$):** This pin should be connected to the Row Address Strobe input of the second 1 Mbit DRAM chip (if used).
2	1	**Row Address Strobe 1 ($\overline{RAS1}$):** This pin should be connected to the Row Address Strobe input of the first DRAM chip.
3	2	**Write Enable ($\overline{WE}$):** The DRAM Read/Write control pin.
4		**$\overline{Xtal}$:** This is the output of the 4.0 MHz on-chip clock oscillator. External components are required at this output when a Xtal is used. A Xtal cannot be used with the 24-pin version.
5	3	**Xtal/Clock:** This is the input to the on-chip clock oscillator inverter. A 4.0MHz Xtal or externally derived clock should be connected here (see component diagram). This clock provides timing for on-chip elements, filters, etc. A Xtal cannot be used with the 24-pin version. Various Xtal frequencies can be used with this device; see Table 3 for sampling rate variations.
6	4	**Interrupt Request ($\overline{IRQ}$):** The output of this pin indicates an interrupt condition to the microcontroller by going to logic "0." This is a "wire-or able" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin is an open drain output. It therefore has a low impedance pulldown to logic "0" when active and a high impedance when inactive. Conditions indicated by this function are Power Reading Ready, Play Command Complete and Store Command Complete.
7	5	**Serial Clock:** This is the C-BUS serial clock input. This clock, produced by the microcontroller, is used for transfer timing of commands and data to and from the DVSR Codec. See timing diagrams. Clock rate requirements vary for different MX802 functions.
8	6	**Command Data:** This is the C-BUS serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (bit 7) first, and LSB (bit 0) last, synchronized to the Serial Clock. See timing diagrams.
9	7	**Chip Select ($\overline{CS}$):** The C-BUS data transfer control function, this input is provided by the microcontroller. Command Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See timing diagrams.
10	8	**Reply Data:** This is the C-BUS serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Data Clock under the control of the Chip Select input. This 3-state output is held at high impedance when not sending data to the microcontroller. See timing diagrams.

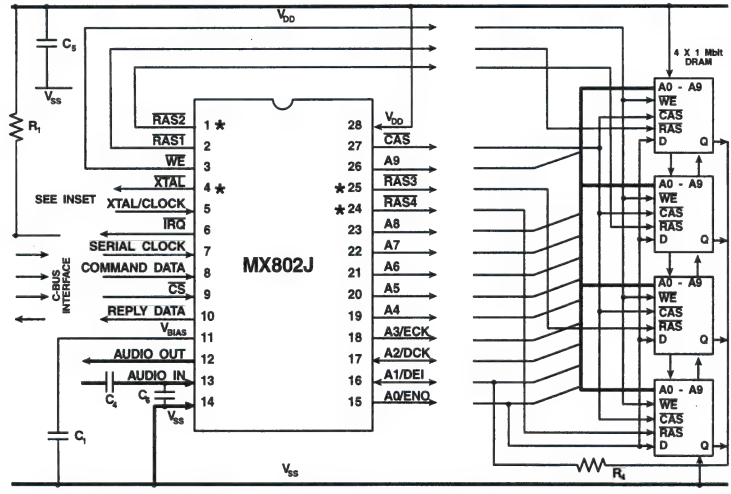
© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Pin Function Chart

Pin		Function
J/LH8	LH	
11	9	V_{BIAS}: This is the output of the on-chip analog circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C_1. See Figure 2.
12	10	**Audio Out:** This is the analog signal output.
13	11	**Audio In:** This is the audio (speech) input. The signal to this pin must be a.c. coupled by capacitor C_4 and decoupled to V_{SS} by HF capacitor C_6. For optimum noise performance this input should be driven from a source impedance of less than 100Ω.
14	12	V_{SS}: Negative Supply (GND).
15	13	**DRAM Data In/A0/Direct Access -- Encoder Out (ENO):** This is connected to the DRAM data input and address line A0. With no DRAM used, this output is available in a Direct Access mode as the Delta Encoder digital data Output. Direct Access control is achieved by Control Register byte 1, bit 7.
16	14	**DRAM Data Out/A1/Direct Access -- Decoder In (DEI):** This is connected to the DRAM data output and address line A1. With no DRAM used, this pin is available in a Direct Access mode as the Delta Decoder Clock input. Direct Access control is achieved by Control Register byte 1, bit 6.
17	15	**DRAM A2/Direct Access -- Decoder Clock (DCK):** This is the DRAM address line A2. With no DRAM employed, this pin is available in a Direct Access mode as the Delta Decoder Clock Input. Direct Access control is achieved by Control Register byte 1, bit 6.
18	16	**DRAM A3/Direct Access -- Encoder Clock (ECK):** This is the DRAM address line A3. With no DRAM employed, this pin is available in a Direct Access mode as the Delta Encoder Clock Output. Direct Access control is achieved by Control Register byte1, bit 6.
19	17	**DRAM A4:** DRAM address line A4.
20	18	**DRAM A5:** DRAM address line A5.
21	19	**DRAM A6:** DRAM address line A6.
22	20	**DRAM A7:** DRAM address line A7.
23	21	**DRAM A8:** DRAM address line A8.
24		**Row Address Strobe 4 ($\overline{RAS4}$):** This pin should be connected to the Row Address Strobe input of the fourth 1 Mbit DRAM chip (if used).
25		**Row Address Strobe 3 ($\overline{RAS3}$):** This pin should be connected to the Row Address Strobe input of the third 1 Mbit DRAM chip (if used).
26	22	**DRAM A9:** This is DRAM address line A9. This pin is not connected when a 256 kbit DRAM is used. Note: To simplify PCB layout, the DRAM address inputs A0-A8 may be connected in any physical order to the DVSR Codec output pins A0-A8.
27	23	**Column Address Strobe ($\overline{CAS}$):** This is the DRAM Column Address Strobe pin. It should be connected to the $\overline{CAS}$ pins of all DRAM chips.
28	24	V_{DD}: Positive supply. A single, stable +5 volt supply is required. Levels and voltages within the DVSR Codec are dependent upon this supply.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

External Components



Component	Value	Component	Value
R_1	22.0kΩ	C_4	1.0µF
R_2	1.0MΩ	C_5	1.0µF
R_3	See Note 1	C_6	.001µF
R_4	1.0kΩ	X_1	4.00MHz
C_1	1.0µF		or 4.032MHz
C_2	33.0pF		or 4.096MHz
C_3	33.0pF		

Tolerance: R = ±10%, C = ±20%

*See Note 3

Figure 2 - Recommended External Component and DRAM Connections

Notes

1. Xtal circuitry shown in Inset is in accordance with the MX-COM Standard and DBS 800 Crystal Oscillator Application Note.

2. External Xtal circuitry is not applicable to the 24 pin/lead versions of this device. Only an externally derived clock input can be used.

3. Functions whose pins are marked with an asterisk* in Figure 2 are not available on the 24-pin/lead versions of this device. Pin numbers illustrated are for 28-pin versions.

4. Table 3 details the actual encoder/decoder sample rates available using the Xtal frequencies recommended above.

5. Resistor R_1 is used as the DBS 800 system common pullup for the C-BUS Interrupt Request ($\overline{IRQ}$) line. The optimum value will depend on the circuitry connected to the $\overline{IRQ}$ line. Up to 8 peripherals may be connected to this line.

6. Recommended DRAM Parameters:
256 kbit x 1 or 1 Mbit x 1 Dynamic Random Access Memory with "$\overline{CAS}$ before $\overline{RAS}$" refresh mode. Maximum Row address access time = .200 µsec.

Example DRAM types:

256kbit (262,144 bits)	
Texas Instruments	TMS4256-20
Hitachi	HM51256-15
1Mbit (1,048,576 bits)	
Texas Instruments	TMS4C1024-15
Hitachi	HM511000-15

7. Figure 2 above shows connections to 4 x 1 Mbit sections of DRAM. If desired, to simplify PCB layout, the DRAM inputs A0-A8 may be connected in any order to the MX802 DVSR Codec output pins A0-A8. Connections to 256 kbit DRAM are similar, but A9 is left unconnected.

8. When using the MX802 "stand alone" (Direct Access), no DRAM sections should be connected.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol

Control of the functions of the MX802 DVSR Codec is by a group of Address/Commands (A/Cs) and appended instructions or data to and from the system microcontroller (See Figure 4). The use and content of these instructions is detailed in the following pages.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB	Data Byte(s)
General Reset	01	0 0 0 0 0 0 0 1	
Write to Control Register	60	0 1 1 0 0 0 0 0	+ 2 byte instruction to Control Register
Read Status Register	61	0 1 1 0 0 0 0 1	+ 1 byte reply from Status Register
Store "N" pages. Start page "X"	62	0 1 1 0 0 0 1 0	+ 2 bytes Command -- Immediate
Store "N" pages. Start page "X"	63	0 1 1 0 0 0 1 1	+ 2 bytes Command -- Buffered
Play "N" pages. Start page "X"	64	0 1 1 0 0 1 0 0	+ 2 bytes Command -- Immediate
Play "N" pages. Start page "X"	65	0 1 1 0 0 1 0 1	+ 2 bytes Command -- Buffered
Write Data. Start page "P"	66	0 1 1 0 0 1 1 0	+ 2 bytes "P" + Write Data
Read Data. Start page "P"	67	0 1 1 0 0 1 1 1	+ 2 bytes "P" + Read Data
Write Data -- Continue	68	0 1 1 0 1 0 0 0	+ Write data
Read Data -- Continue	69	0 1 1 0 1 0 0 1	+ Read data

Table 1 - C-BUS Address/Commands

Address/Commands

Instruction and data transactions to and from this device consist of an Address/Command (A/C) byte followed by further instruction/data or a status/data reply.

Control and configuration is by writing instructions from the microcontroller to the Control Register (60_H). Reporting of MX802 configurations is by reading the Status Register (61_H).

Operation with DRAM

The MX802 can operate with up to 4 Mbits of Dynamic RAM (DRAM). When used with DRAM, the MX802 performs four main functions under the control of commands received over the C-BUS interface from the microcontroller:

Stores Speech: The MX802 stores speech by digitally encoding the analog input signal and writing the resulting digital data into the associated DRAM.

Plays Speech: The MX802 plays back stored speech by reading the digital data stored in the DRAM and decoding it to provide an analog output signal.

Writes Data: The MX802 writes data sent over the C-BUS from the microcontroller to DRAM.

Reads Data: The MX802 reads data from DRAM, sending it to the microcontroller over the C-BUS.

Data is directed to and from DRAM by the on-chip DRAM Controller.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol

Speech

The CVSD encoder and decoder sampling rates are independently set via the Control Register (see Tables 2, 3 & 4) to 16, 25, 32, 50 or 64 kbps. This allows the user to choose between speech quality and storage time while providing for time compression or expansion of the speech signals.

The DVSR Codec can handle from 256 kbits to 4 Mbits of DRAM, giving, in the case of the 32 kbps sampling rate, from 8 to 131 seconds of speech storage.

For speech storage purposes, the memory is divided into "pages" of 1024 bits each, corresponding to 32ms at a 32 kbps sampling rate.

A 256 kbit DRAM contains	256 "pages."
A 1 Mbit DRAM contains	1024 "pages."
A 4 Mbit DRAM contains	4096 "pages."

When used without DRAM, the decoder sampling rate (8-64 kbps) is determined by an external clock source applied to the Decoder Clock pin.

Store and Play Speech Commands

Speech storage and playback may take place simultaneously. These commands are transmitted, via C-BUS, to the MX802 in the following form:

STORE OR PLAY "N" (1024-bit) PAGES (of encoded speech data) STARTING AT PAGE "X."

"N" can be any number between 0 and F (1-16 pages). "X" can be any number from 0 to 4095 (4Mbit DRAM), as shown below. Preceded by A/C, this command writes 16 bits (byte 1 and byte 0) of data from the microcontroller to the Store or Play Command Buffer.

MSB BYTE 1								BYTE 0							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N								X							

Speech Store Commands

62_H STORE "N" PAGES – START PAGE "X" (immediate)

63_H STORE "N" PAGES – START PAGE "X" (buffered)

The digitized speech from the CVSD encoder is stored in consecutive DRAM locations with the Speech Store Counters sequencing through the DRAM addresses and counting the number of complete pages stored since the start of the execution of the command.

As soon as the command has terminated, the following events take place:

1. The Store Command Complete bit in the Status Register (Table 5) is set.

2. An Interrupt Request ($\overline{IRQ}$) is sent, if enabled, to the microcontroller.

3. The next speech storage command (if present) is immediately taken from the Store Command Buffer and execution of the new command commences.

The $\overline{IRQ}$ output is cleared by reading the Status Register:

61_H READ STATUS REGISTER (Table 6).

To provide continuity of speech commands, both Store and Play Commands can be presented to eh MX802 in one of two formats: *immediate or buffered.*

An *immediate* command will be started on completion of its loading, irrespective of the condition of the current command.

A *buffered* command will begin after the completion of the current Store or Play command, unless Speech Synchronization Bits (Control Register) are set.

Buffering of commands lets the DVSR Codec execute a series of commands without intervening gaps even though the microcontroller may take several milliseconds to respond to each "Command Complete" Interrupt Request.

In either case, the Store or Play Command Complete bit of the status register will be cleared.

Speech Playback is controlled by similar commands using the Speech Play Counters and Play Command Buffer:

64_H PLAY "N" PAGES – START PAGE "X" (immediate)

65_H PLAY "N" PAGES – START PAGE "X" (buffered).

As soon as the Play Command has completed, the "Play Command Complete" bit in the Status Register is set, and an Interrupt Request is generated (if enabled).

If no "next" command is waiting in the Play Command Buffer when a speech play command finishes, a continuous idle code (0101....0101) will be fed to the delta decoder.

Speech data is stored or recovered at the selected Encode or Decode sample rate (Table 3). Store or Play Command Complete bits in the Status Register are cleared by the next Store or Play Command received from the microcontroller, or by a General Reset (01_H).

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol

Speech...

Store/Play Speech Synchronization (Table 4)

This capability is provided primarily for Time Domain Scrambling applications.

Speech Synchronization bits in the Control Register will produce the effects described below:

No Speech Sync Set: Store and Play operations may take place completely independently.

Store after Play: The next buffered store command will start on completion of a play command, while the next play command sequence (if any) continues normally.

Play after Store: The next buffered play command will start on completion of a store command, while the next store command sequence (if any) continues normally.

These actions will continue while Speech Sync bits are set.

Data Handling

For the purpose of storing data sent via C-BUS from the microcontroller, the memory (DRAM) is divided into "data pages" of 64 bits (8 bytes).

A 256kbit DRAM contains	4096 data pages.
A 1Mbit DRAM contains	16384 data pages.
4Mbit DRAM contains	65536 data pages.

In accordance with C-BUS timing specifications, data is handled 8 bits (1 byte) at a time, although any number of 8-bit blocks of data may be written to or read from the DRAM by a single command.

Data transfer is terminated by the Chip Select line going to a logic "1."

C-BUS Data Transfer Limitations

For those commands which transfer data over the C-BUS between DRAM and the microcontroller (Write and Read data), the C-BUS serial clock rate is limited to a maximum of:

125kHz if the VSR Codec is executing store and play commands.

250kHz if no speech Store or Play commands are active.

This limitation is due to the rate at which data goes into and out of the DRAM. All other commands and replies (Control, Status, Reset) may use a maximum clock rate of 500kHz. See Figure 4.

Read Data

67_H READ DATA -- START PAGE "P"

This command sets the Data Read Counter to "P," page, and then reads data bytes from successive DRAM locations, sending them to the microcontroller as Reply Data bytes. The Data Read Counter is incremented by 1 for each bit read.

69_H READ DATA CONTINUE

This command reads data bytes from successive DRAM locations determined by the Data Read Counter, incrementing the counter by 1 for each bit read.

Write Data

66_H WRITE DATA -- START PAGE "P"

This command sets the Data Write Counter to "P" page, and then writes data bytes to successive DRAM locations, incrementing the Data Write Counter by 1 for each bit received via the C-BUS.

The Start Page, "P," is indicated by loading a 2-byte word after the relevant Address/Command byte. This 16-bit word allows data page addresses from 0 to 65535 (4Mbits DRAM).

68_H WRITE DATA CONTINUE

This command writes data bytes to successive DRAM locations determined by the Data Write Counter, incrementing the counter by 1 for each bit received over the C-BUS.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Controlling Protocol

DRAM Speech Capacity

28-pin/lead versions of the MX802 may be used with a single 256kbit DRAM, or with up to 4 x 1Mbit of DRAM. 24-pin/lead versions may only be used with a single 256kbit or 1Mbit DRAM. The different encode and decode sampling clock rates available enable the user to set voice store and play times against recovered speech quality. Table 2 gives information on storage capacity and Store/Playback times. Speech data can be replayed at a different sample rate or in a reversed sequence (see Control Register for details).

DRAM Size	Available Bits	Speech Pages	Nominal Sample Rates (kbps) 16	25	32	50	64
256kbps	262144	256	16.0	10.0	8.0	5.0	4.0
1024kbps	1048576	1024	65.0	42.0	32.0	20.0	16.0
2Mbps	2097152	2048	131.0	84.0	65.0	42.0	32.0
3Mbps	3145728	3072	196.0	126.0	98.0	63.0	49.0
4Mbps	4194304	4096	262.0	168.0	131.0	84.0	65.5
			Store and Play Times (seconds)				

Table 2 - Sampling Clock Rates vs Speech Storage/Playback Times

Encoder and Decoder Sampling Clocks

Encoder and decoder sampling clock rates are programmable via the Control Register. Table 3 shows the range of sampling rates available for different Xtal/clock input frequencies and the counter ratios used to produce them. Consideration should be given to the effect of different Xtal/clock frequencies upon the audio frequency performance of the device.

Control Register *Byte 0, Bits* 5 4 3 Dec. 2 1 0 Enc.	Internal Counter Division Ratio	Xtal.clock Frequency (MHz) 4.0	4.032 Sampling Rate kbps	4.096
0 1 1	256	15.625	15.75	16.0
1 0 0	160	25.0	25.20	25.60
1 0 1	128	31.25	31.50	32.0
1 1 0	80	50.0	50.4	51.20
1 1 1	64	62.50	63.0	64.0

Table 3 - Sampling Clock Rates Available

With respect to using a single Xtal/clock frequency for all DBS 800 devices in use, it should be noted that

(a) a 4.032MHz Xtal/clock input will produce an accurate 1200-baud rate for the MX809 MSK Modem.

(b) a 4.096MHz Xtal/clock input will generate exactly 16kbps, 32kbps and 64kbps Codec sampling clock rates.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

"Write to Control Register" - Address/Command 60_H, followed by 2 bytes of Command Data

Setting	Function
Byte 1	***First Byte for Transmission***
(MSB) Bit 7	Not used - Set to "0"
6	**Direct Access**
1	-- Encoder Data out to A0/ENO -- Encoder Clock to A3/ECK -- Decoder Input from A1/DEI -- Decoder Clock from A2/DCK
0	Normal DVSR Operation
5	**Play Counter**
1	Decrement
0	Increment
4	**DRAM Control**
1	Disable DRAM
0	Enable DRAM
3	**Codec Powersave**
1	Powersave MX802
0	MX802 Enable
2	**Store Command Interrupt**
1	Enable Interrupt
0	Disable
1	**Play Command Interrupt**
1	Enable Interrupt
0	Disable
0	**Power Reading Interrupt**
1	Enable Interrupt
0	Disable
Byte 0	***Last Byte for Transmission***
(MSB) 7 6	**Store/Play Speech Sync.**
0 0	No Sync
0 1	No Sync
1 0	Sync - Play after Store
1 1	Sync - Store after Play
5 4 3	**Decoder Control**
0 0 0	Idle (32kbps); Aud O/P from LPF
0 0 1	Idle (32kbps); Aud bypass
0 1 0	Idle (32kbps); Aud O/P at high Z
0 1 1	On - Sampling Rate 16kbps
1 0 0	On - 25kbps
1 0 1	On - 32kbps
1 1 0	On - 50kbps
1 1 1	On - 64kbps
2 1 0	**Encoder Control**
0 0 0	I/P at V_{BIAS}; F/Idle (32kbps)
0 0 1	I/P at high Z; F/Idle (32kbps)
0 1 0	I/P at high Z; F/Idle (32kbps)
0 1 1	On - Sampling Rate 16kbps
1 0 0	On - 25kbps
1 0 1	On - 32kbps
1 1 0	On - 50kbps
1 1 1	On - 64kbps

Table 4 - Control Register

General Reset

Upon power-up the bits in the MX802 registers will be random (either 0 or 1). A General Reset Command (01_H) will be required to reset all devices on the C-BUS. It has the following effect on the MX802:

Control Register	Set to 00_H
Status Register	Set to 00_H
Clear Store and Play Command Bufers	

Direct Access

External circuitry is allowed direct access to the Delta Codec data and sampling clocks, disabling the DRAM timing circuitry. This permits the Delta Codec section of the MX802 to be used as a Delta Modulation voice encoder and decoder.

Input audio is encoded and made available at the Encoder Out (ENO) pin. Speech data input to the Decoder In (DEI) pin is decoded to give voice-band audio at the Audio Output.

Analog output switching remains under the control of the Control Register, but the decoder sampling clock rate (8kbps to 64kbps) must be provided from an external source to the Decoder Clock (DCK) pin. To ensure correct filter setting, Decoder Control bits (byte 0, bits 5, 4, 3) should be set to binary 1,1,1, where the required rate approximates to a multiple of 25kbps.

Both the encoder internal sampling clock rate and input switching (Table 5) remain under the control of the Control Register. The encoder internal sampling clock rate is available to external circuitry at the Encoder Clock Out (ECK) pin.

Play Counter

The Play Counter direction may be set to run backward as well as forward. This can be used in a scrambling system by replaying speech data in reverse order.

DRAM Control

A logic "1" will disable the DRAM Control Timing circuits and associated counters. The C-BUS Interface, Clock Generator, Delta Codec and filters remain active. This bit should be set to logic "1" when the MX802 is used in the Direct Access Mode.

Minimum DVSR Codec power consumption is achieved by setting both DRAM Control and Powersave bits to logic "1."

Codec Powersave

A logic "1" puts the Delta Codec and filters into Powersave Mode with V_{BIAS} maintained. The Clock Generator, C-BUS Interface, and DRAM Control and Timing remain active.

Command Interrupt Enable

A logic "1" set at the relevant bit will enable Interrupt Requests to the microcontroller when that command operation is complete.

Store and Play Speech Synchronization

This is intended primarily for Time Domain Scrambling.

Decoder and Encoder Control

This individually sets decoder and encoder sampling clock rates, as well as the source of the audio output.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Encoder and Decoder Control: Analog Input and Output Switching

The Control Register, Byte 0: bits 0 to 5, are used together with the codec Powersave Bit (Byte 1: bit 3) to control codec input/output conditions and sample rates. Figure 3 shows the codec functional situation.

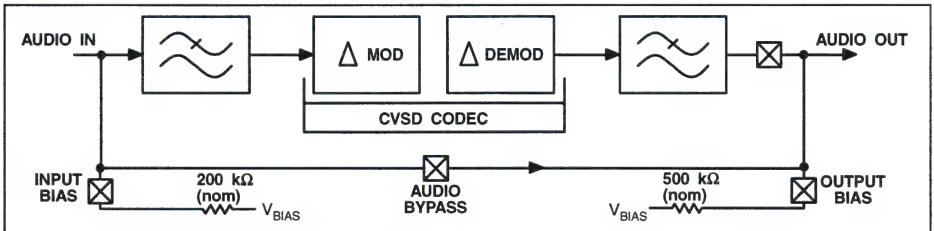


Figure 3 - Analog Control (with reference to Figure 1)

CONTROL REGISTER				CIRCUIT SWITCHES			*OFF = Switch Open* *ON = Switch Closed*	Note
Codec Powersave Bit	Decoder Control 5	4	3	Audio Bypass	Audio Out	Output Bias		
0	0	0	0	OFF	ON	OFF	Decoder idling fed with "1010101..." pattern at 32 kbps	1
0	0	0	1	ON	OFF	OFF		
0	0	1	0	OFF	OFF	OFF		
0	0	1	1	OFF	ON	OFF	Decoder running at the selected sampling rate	1
-	-	-	-	-	-	-		
0	1	1	1	OFF	ON	OFF		
1	0	0	0	OFF	OFF	ON	Decoder circuits powersaved	
1	0	0	1	ON	OFF	OFF		
1	0	1	0	OFF	OFF	ON		
1	0	1	1	OFF	OFF	ON		
-	-	-	-	-	-	-		
1	1	1	1	OFF	OFF	ON		
	Encoder Control 2	1	0	Input Bias				2
0	0	0	0	ON			Encoder running at 32 kbps but Encoder Data O/P forced to idle pattern "01010..."	
0	0	0	1	OFF				
0	0	1	0	OFF				
0	0	1	1	OFF			Encoder running at selected sampling rate	
-	-	-	-	-				
0	1	1	1	OFF				
1	0	0	0	ON			Encoder circuits powersaved	
-	-	-	-	-				
1	1	1	1	ON				

Table 5 - Analog Control (refer to Figure 3)

Notes

1. If the Delta Codec is in the Direct Access mode, these sampling rates will be as provided by the externally applied clock.
2. The input bias switch is operated by the Control Register Codec Powersave and Encoder Control bits to provide a relatively low impedance path for V_{BIAS} to charge the input coupling capacitor whenever the codec is powersaved, or the encoder control bits are set to 0, so that input bias can be established quickly prior to operation.

Time Compression of Speech

The 25 kbps and 50 kbps sampling rate options are provided for time compression and subsequent expansion of speech signals.

For example, 1.0 seconds of speech stored at 50 kbps may be transmitted in 0.8 seconds if played out at 64 kbps, and finally restored to its original speed at the receiver by storing at 64 kbps and playing out at 50 kbps. A similar result (with a degraded SINAD) may be achieved by using 25 kbps and 32 kbps sampling rates.

However, the speech frequencies are raised by time compression, and since the signal transmitted to air must be band limited to 3400 Hz, the effective end-to-end bandwidth is 0.8 x 3400 Hz, which is approximately 2700 Hz.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

"Read Status Register" - Address/Command 61_H, followed by 1 byte of Reply Data

Reading					Function	
MSB Bit 7					Power Reading Ready	
1						
6					Store Command Complete	
1						
5					Play Command Complete	
1						
					Power Register	
4	3	2	1	0	Pwr Compand	Bits/pg.
0	0	0	0	0		0
0	0	0	0	1		1
0	0	0	1	0		2
0	0	0	1	1		3
0	0	1	0	0		4
0	0	1	0	0		5
0	0	1	1	0		6
0	0	1	1	1		7
0	1	0	0	0	-39.0 dB	8
0	1	0	0	1		10
0	1	0	1	0	-36.0	12
0	1	0	1	1		14
0	1	1	0	0	-33.5	16
0	1	1	0	1		18
0	1	1	1	0	-30.0	20
0	1	1	1	1		22
1	0	0	0	0	-28.0	24
1	0	0	0	1		32
1	0	0	1	0	-25.0	40
1	0	0	1	1		48
1	0	1	0	0	-22.0	56
1	0	1	0	1		64
1	0	1	1	0	-19.0	72
1	0	1	1	1		80
1	1	0	0	0	-16.0	88
1	1	0	0	1		128
1	1	0	1	0	-10.0	192
1	1	0	1	1		256
1	1	1	0	0	-6.0	320
1	1	1	0	1		384
1	1	1	1	0	0 dB	448
1	1	1	1	1		512

Table 6 - Status Register

Interrupts

If enabled by the Control Register, an Interrupt Request ($\overline{IRQ}$), is produced by the MX802 to report the following actions:

Power Reading Ready
Store Command Complete
Play Command Complete

When an Interrupt is produced, the Status Register must be read to determine the source of the interrupt. This action will clear the $\overline{IRQ}$ output.

The **Store Command Complete** bit (and an interrupt) is set on completion of a Store Command. This bit is cleared by loading the next Store Command, or by a General Reset Command (01_H).

The **Play Command Complete** bit (and an interrupt) is set on completion of a Play Command. This bit is cleared by loading the next Play Command, or by a General Reset Command (01_H).

The **Power Reading Ready** bit (and an interrupt) is set for every 1024 voice-data bits (1 page) from the Encoder. This bit is cleared after reading the Status Register, or by a General Reset Command (01_H).

Power Register

The power assessment element shown in Figure 1 assesses the input signal power for each encoded "page" (every 1024 encoder output bits) by counting the number of "compand bits" (000 or 111 sequences in the output bit stream) produced during that page (see Table 6) with typical encoder input power levels (dB).

At the end of each "page" the power reading ready bit of the status register is set, and an interrupt request is generated (if enabled). The resulting count is converted to a 5-bit quasi-logarithmic form. The Power Register reading is interpreted as follows:

00000 represents 0 compand bits
00001 represents 1 compand bit
11111 represents 512 compand bits, the maximum.

This power reading is placed in the status register to be read by the microcontroller. Figure 4 shows this output, indicating the input power level.

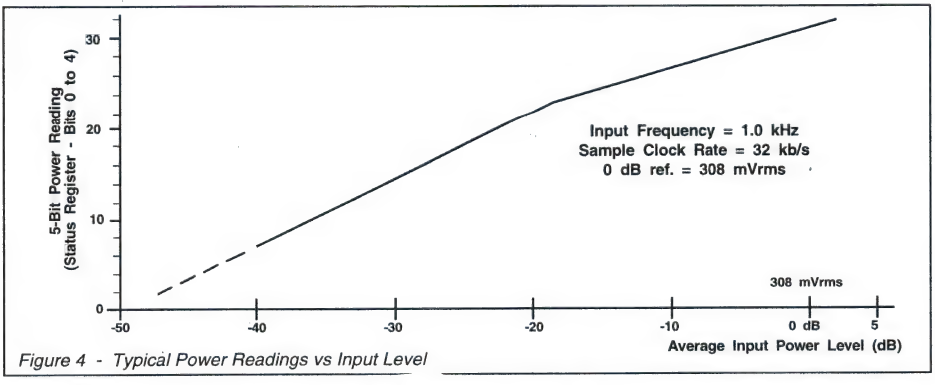


Figure 4 - Typical Power Readings vs Input Level

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Timing Information

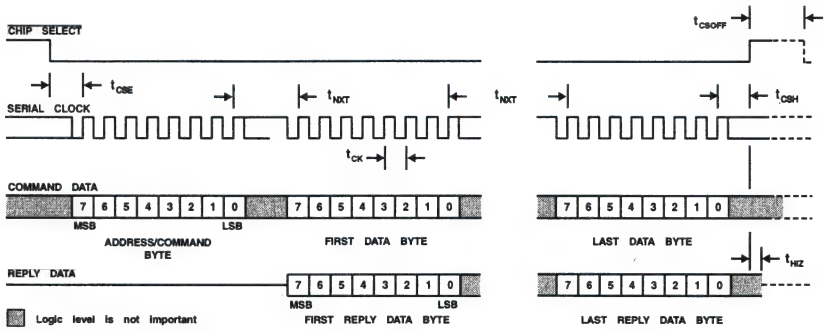


Figure 5 - C-BUS Timing Information

C-BUS Timing (Figure 5)		Min. a	Min. b	Min. c	Max.	Unit
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0	4.0	8.0	-	µs
t_{CSH}	Last Serial Clock Rising Edge to Chip Select High	4.0	4.0	8.0	-	µs
t_{HIZ}	Chip Select High to Reply Data High - Z	-	-	-	2.0	µs
t_{CSOFF}	Chip Select High	2.0	4.0	8.0	-	µs
t_{NXT}	Command Data Inter-Byte Time	4.0	8.0	16.0	-	µs
t_{CK}	Serial Clock Period	2.0	4.0	8.0	-	µs

Direct Address Timing (Figure 6)		Min.	Typ.	Max.	Unit
t_{CH}	Decoder or Encoder Clock High	1.0	-	-	µs
t_{CL}	Decoder or Encoder Clock Low	1.0	-	-	µs
t_{SU}	Decoder Data Set Up Time	.45	-	-	µs
t_H	Decoder Data Hold Time	.60	-	-	µs
t_{PCO}	Encoder Clock High to Encoder Data Valid	-	-	.75	µs
$t_{SU}+t_H$	= Data True Time				

Notes

1. Minimum Timing Values
   (a) For all commands except "Read Data" and "Write Data" commands.
   (b) For "Read Data" and "Write Data" commands when *no* "Speech Store" or "Speech Play" commands are active.
   (c) For "Read Data" and "Write Data" commands when "Speech Store" or "Speech Play" commands are active.
2. Depending on the command, 1 or 2 bytes of Command Data are transmitted to the peripheral MSB (bit7) first, and LSB (bit0) last. Reply data is read from the peripheral MSB (bit7) first, and LSB (bit0) last.
3. To allow for different microcontroller serial interface formats, C-BUS compatible ICs are able to work with either polarity Serial Clock pulses.
4. Data is clocked into and out of the peripheral on the rising Serial Clock edge.
5. Loaded commands are acted upon at the end of each command.

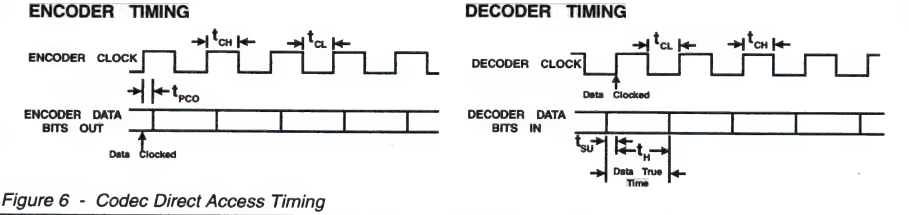


Figure 6 - Codec Direct Access Timing

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Codec Performance

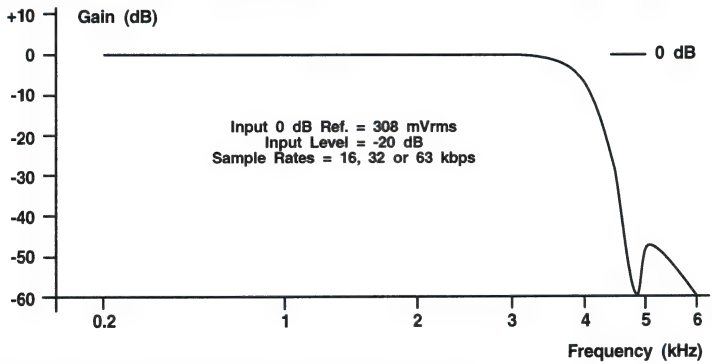


Figure 7 - Typical Overall (Encoder + Decoder) Frequency Response

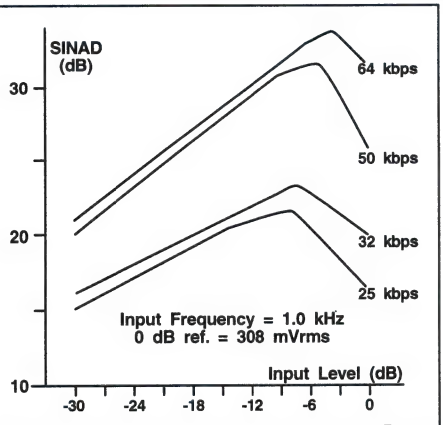


Figure 8 - SINAD vs Input Level at Different Sample Rates

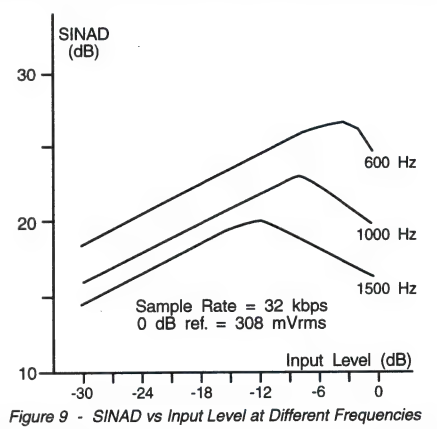


Figure 9 - SINAD vs Input Level at Different Frequencies

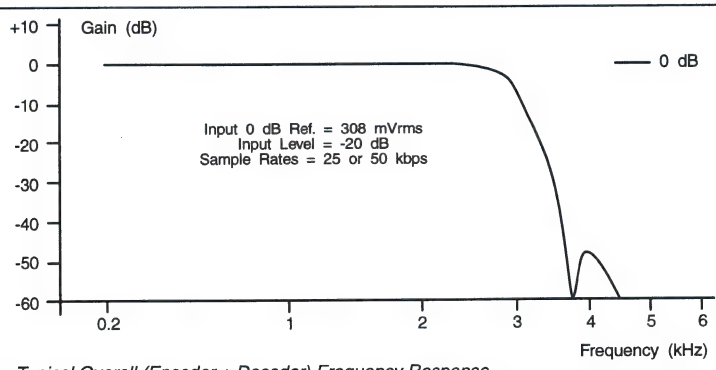


Figure 10 - Typical Overall (Encoder + Decoder) Frequency Response

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin	-0.3V to (V_{DD}+0.3 V)
Sink/source current	
(supply pins)	±30mA
(other pins)	±20mA
Total device dissipation (@T_{AMB} 25°C)	800 mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/clock f_0 = 4.0MHz

Audio level 0dB ref = 308 mVrms

Standard test signal f_0 = 820Hz

Sample Rate = 31.25kbps

Characteristics

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage (V_{DD})			4.5	5.0	5.5	V
Supply current (enabled)		1	-	7.0	10.0	mA
Supply current (powersave)		1	-	2.0	4.0	mA
Digital Interface						
Input Logic "1"		2	3.5	-	-	V
Input Logic "0"		2	-	-	1.5	V
Output Logic "1"	at IOH = -120mA	7	4.6	-	-	V
	at IOH = -50mA	3	4.6	-	-	V
	at IOH = 20mA	9	4.6	-	-	V
Output Logic "0"	at IOL = 20mA	9	-	-	0.4	V
	at IOL = 100mA	3	-	-	0.4	V
	at IOL = 360mA	7,8	-	-	0.4	V
Digital Input Current						
V_{IN} = Logic "1" or "0"		2	-	-	1.0	µA
Leakage Current into $\overline{IRQ}$ "OFF" Output		4	-	-	4.0	µA
Digital Input Capacitance		2	-	-	7.5	pF
Analog Impedance						
Input Impedance		12	-	500	-	kΩ
Output Impedance			-	1.5	-	kΩ
Dynamic Values						
Encoder						
Analog Signal Input Levels		5	-24.0	-	4.0	dB
Passband		10,11	-	3400	-	Hz
Decoder						
Analog Signal Output Levels		5	-24.0	-	4.0	dB
Passband		10,11	300	-	3400	Hz
Encoder/Decoder (Full Codec)						
Passband		10,11	300	-	3400	Hz
Passband Gain		11	-	0	-	dB
Passband Ripple		11	-3.0	-	3.0	dB
Stopband			6.0	-	10	kHz
Stopband Attenuation			-	50.0	-	dB
SINAD Level			-	23.0	-	dB
Output Noise (Input short circuit)			-	-50	-	dBp
Idle Channel Noise (Forced)			-	-55	-	dBp
Xtal/clock Frequency		6	-	4.0	-	MHz

Notes
1. Does not include current drawn by any attached DRAM.
2. Serial Clock, Command Data, Chip Select, A1/DEI and A2/DCK inputs.
3. $\overline{CAS}$, $\overline{WE}$ and A0 to A9 outputs.
4. When the $\overline{IRQ}$ outuput is at V_{DD}.
5. The optimum range of levels for a good Signal-to Noise ratio.
6. Audio frequency responses will vary with respect to Xtal/clock frequency.
7. Reply Data output.
8. $\overline{IRQ}$ output.
9. RAS output.
10. Passband is reduced to (typically) 2700 Hz when a sample rate of 25 kbps or 50 kbps is used.
11. Measured with a -20dB input level to avoid codec slope-overload.
12. For optimum noise performance this input should be driven from a source impedance of less than 100Ω.

© 1997 MX-COM, Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480033.007

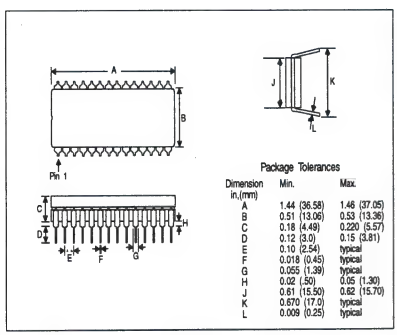
Package Outline

Figure 11 shows the MX802J 28-pin Ceramic Dual In-Line Package. TheMX802LH8 28-lead Plastic Leaded Chip Carrier is shown in Figure 12. TheMX802LH 24-lead Plastic Leaded Chip Carrier is in Figure 13. For identification purposes the MX802LH and LH8 have an ident spot adjacent to pin 1 and a chamfered corner between pins 3 and 4 (LH) or between pins 4 and 5 (LH8).

Handling Precautions

The MX802 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent potentially damaging static discharges.

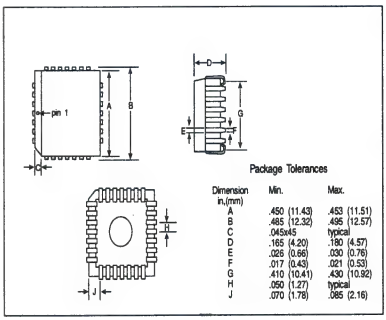
Figure 11 - MX802J 28-pin Cerdip



Package Tolerances

Dimension in.(mm)	Min.	Max.
A	1.44 (36.58)	1.46 (37.05)
B	0.51 (13.06)	0.53 (13.36)
C	0.18 (4.49)	0.220 (5.57)
D	0.12 (3.0)	0.15 (3.81)
E	0.10 (2.54)	typical
F	0.018 (0.45)	typical
G	0.055 (1.39)	typical
H	0.02 (.50)	0.05 (1.30)
J	0.61 (15.50)	0.62 (15.70)
K	0.670 (17.0)	typical
L	0.009 (0.25)	typical

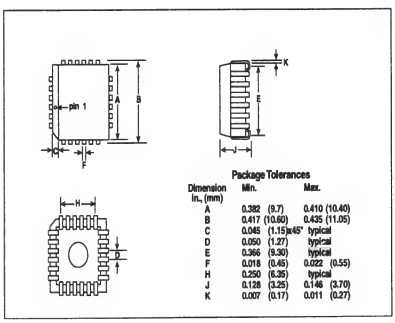
Figure 12 - MX802LH8 PLCC -28



Package Tolerances

Dimension in.(mm)	Min.	Max.
A	.450 (11.43)	.453 (11.51)
B	.485 (12.32)	.495 (12.57)
C	.045x45	typical
D	.165 (4.20)	.180 (4.57)
E	.026 (0.66)	.030 (0.76)
F	.017 (0.43)	.021 (0.53)
G	.410 (10.41)	.430 (10.92)
H	.050 (1.27)	typical
J	.070 (1.78)	.085 (2.16)

Figure 13 - MX802LH PLCC-24 Package



Package Tolerances

Dimension in., (mm)	Min.	Max.
A	0.382 (9.7)	0.410 (10.40)
B	0.417 (10.60)	0.435 (11.05)
C	0.045 (1.15)x45°	typical
D	0.050 (1.27)	typical
E	0.366 (9.30)	typical
F	0.018 (0.45)	0.022 (0.55)
H	0.250 (6.35)	typical
J	0.128 (3.25)	0.146 (3.70)
K	0.007 (0.17)	0.011 (0.27)

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480033.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATABULLETIN

MX812

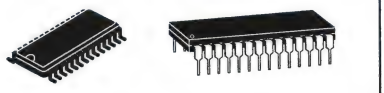
VSR CODEC WITH DRAM CONTROL

C-BUS COMPATIBLE

PRELIMINARY INFORMATION

Features and Applications

- **Half-Duplex Voice Storage and Retrieval**
- **Serial Bus µProcessor Control**
- **On-Chip DRAM Controller**
- **Up To 2 Minutes of High-Quality Recorded Audio**
- **Answering Functions and Voice-Notepad**
- **Low-Power 5-Volt CMOS**
- **Selectable Sample Rates and "Memory Size"**



MX812DW
28-pin SOIC

MX812J
28-pin CDIP

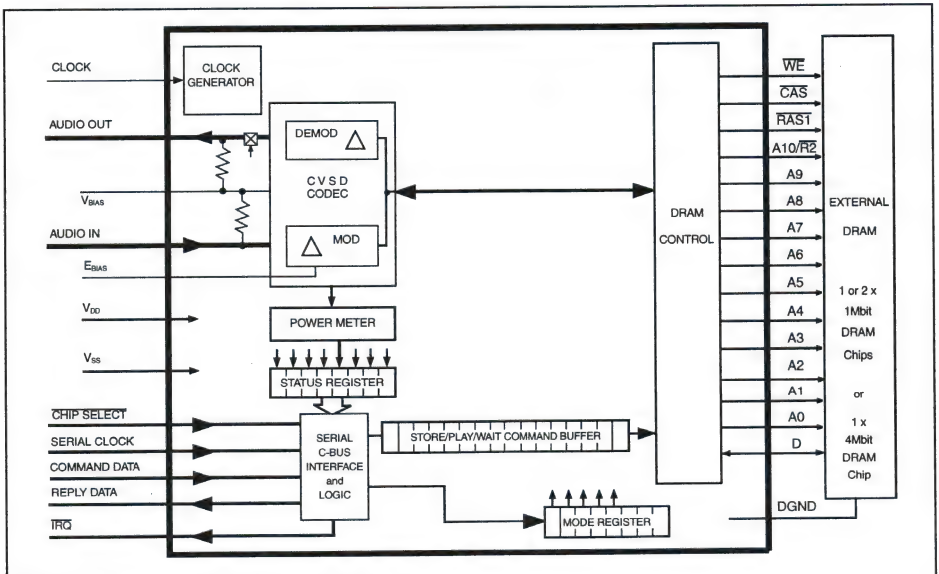


Figure 1 - MX812 Voice Store and Retrieve Codec

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480076.003

DESCRIPTION

The MX812 is a half-duplex VSR Codec, which when connected to an audio processing microcircuit (such as the MX816, 826 or 836), provides the storage and recovery of speechband audio in attached Dynamic RAM. The addition of this device will enhance the communications system by providing cellular radios with Answering Functions, "Message-Notepad" and general announcement cabilities.

The MX812 will enable:

- Storage of a speech message for transmission (replay) at a later time.
- Storage of a received speech message when the operator is not attending.
- The storage and subsequent replay of speech.

All VSR operating functions are controlled by a simple serial µProcessor interface which may operate from the radio's own µProcessor/Controller.

Input audio from the "Store" output of the audio processor is digitized by delta modulation and stored via the DRAM controller, in attached memory.

Audio for replay is recovered from the assigned memory locations and after demodulation made available for supply to the "Play" input of the audio processor. For use with other audio systems, the input/output audio can be connected to relevant points in circuit.

The MX812 has no on-chip input or output audio filtering; this capability must therefore be provided by the host system. Sampling rates and memory capacity are selectable to 32kb/s or 63kb/s and 1 x 4Mbit or 2 x 1Mbit respectively, which when used in conjunction allow control of audio-quality and storage-time.

This low-power CMOS device is available 28-pin plastic SOIC and 28-pin Cerdip packages.

Pin	Function
1	**$\overline{\text{CAS}}$:** This output should be connected to the "Column Address Strobe" input pin(s) of all DRAM devices installed.
2	**$\overline{\text{WE}}$:** This output should be connected to the "Write Enable" input pin(s) of all DRAM devices installed.
3	**D:** Digital (speech) data into and out of the VSR Codec. This pin should be connected to the "Data In" and "Data Out" pins ("D" and "Q") of DRAM devices.
4	**Xtal:** The nominal 4.0MHz clock input to the VSR Codec. The signal applied to this device may be derived from the attached Audio Processor on-chip Xtal Oscillator circuits (see Figures 2 and 3). **Note** that the VSR Codec will be able to function and maintain correct DRAM refresh, with Xtal input frequencies down to 2.0MHz. Compand and Local Decoder time constants will change accordingly and minimum "C-BUS" timings (Figures 6 and 7) would have to be increased pro-rata.
5	**Interrupt Request ($\overline{\text{IRQ}}$):** This Interrupt Request output from the MX812 is 'wire-OR able' allowing the Interrupt Outputs of other peripherals to be commoned and connected to the Interrupt input of the µProcessor (see the C-BUS Interface and System Applications document). This input has a low-impedance pulldown to V_{SS} when active, and a high-impedance when inactive.
6	**Serial Clock:** The C-BUS serial clock input. This clock produced by the µController, is used for transfer timing of commands and data to and from the VSR Codec. See Timing Diagrams.
7	**Command Data:** The C-BUS serial (command) data input from the µController. Data is loaded to this device in 8-bit bytes MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock.
8	**Chip Select ($\overline{\text{CS}}$):** The C-BUS data transfer control function. This input is provided by the µController. Transfer sequences are initiated, completed or aborted by this signal. See Timing Diagrams.
9	**Reply Data:** The C-BUS serial data output to the µController. The transmission of reply bytes is synchronized to the Serial Clock under the control of the Chip Select input. This is a 3-state output which is held at a high-impedance when not sending data to the µController.
10	**V_{BIAS}:** The output of the internal analog circuitry bias line, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C_2 (see Figure 2).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480076.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

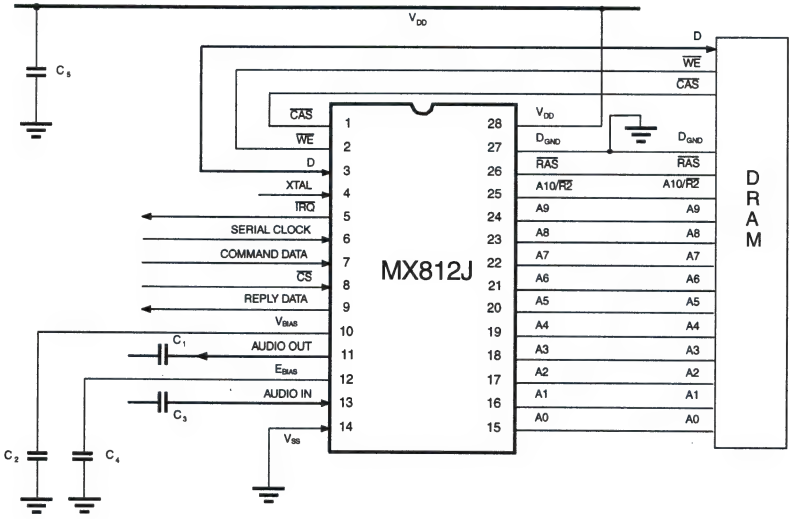
Pin	Function
11	**Audio Out:** The analog output to the Audio Processor "Play" input when the VSR Codec is configured as a Decoder. When configured as an active Decoder but with no Play Page commands (62_H) active, the VSR Codec will play-out an idle pattern of "101010.....10". When not configured as a Decoder, or Powersaved (Mode Register), this output will be held at V_{BIAS} via an internal 500kΩ resistor. The output at this pin is unfiltered; an external speechband filter – such as that included on the MX816/826/836 Audio Processors – will be required. Since this output is centered around $V_{DD}/2$ a coupling capacitor is required.
12	**E_{BIAS}:** The Encoder d.c. internal balancing circuitry line. This pin should be decoupled to V_{SS} by capacitor C_4 (see Figure 2). **Note** that in the 'Encode' mode (Mode Register DE and PS both "0") the Codec drives this pin to approximately $V_{DD}/2$ through a very high impedance; it can take more than one second for the E_{BIAS} voltage to stabilize when power is first applied to this device. A faster start-up can be achieved by setting Bit DE or PS to "1" for 250mS (approx) during power-up. This will cause the E_{BIAS} pin to be connected to V_{BIAS} through a resistance of approximately 100kΩ.
13	**Audio In:** The analog input to the VSR Codec in the Encode mode. When not configured as an Encoder, or Powersaved (Mode Register), this input will be held at V_{BIAS} via an internal 500kΩ resistor. This pin should be coupled via a capacitor, see Figure 2. As this input does not contain an internal audio filter, the audio to this pin should be limited to a 3400Hz "speechband" by an external audio filter – such as included in the MX816/826/836 Audio Processors.
14	**V_{SS}:** The "analog" ground connection. See D_{GND} description.
15	**A0:**
16	**A1:**
17	**A2:**
18	**A3:**
19	**A4:** — DRAM address line outputs from the MX812. These pins should be connected to the corresponding address inputs of the associated DRAM.
20	**A5:**
21	**A6:**
22	**A7:**
23	**A8:**
24	**A9:**
25	**A10/$\overline{R2}$:** A dual function output pin selected by the memory size (MS) bit (Mode Register), as detailed in the table below:

MS bit	DRAMs	Connected To	This Output
"0"	1Mbits'	DRAM No 2 $\overline{RAS}$	RAS2
"1"	4Mbit	DRAM A10	A10 Signal

26	**$\overline{RAS}$:** An output from the VSR Codec which should be connected to the "Row Address Strobe" pin of the 4Mbit DRAM or the first 1Mbit DRAM, see Figure 4, Example DRAM connections.
27	**D_{GND}:** The digital signal ground connection to the VSR Codec. Both D_{GND} and V_{SS} pins should be connected to the negative side of the d.c. power supply. However, a printed circuit board should be laid out so that D_{GND} is connected as closely as possible to the DRAM section ground pins.
28	**V_{DD}:** Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the VSR Codec are dependent upon this supply. This pin should be decoupled to V_{SS} via capacitor C_5, located close to the MX812 pins.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480076.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Application Information



Component	Value
C_1	Dependent upon the input impedance of the driven stage
C_2	1.0µF
C_3	0.1µF
C_4	1.0µF non-electrolytic
	Tolerance: Capacitors = -50/+100%

Figure 2 - Recommended External Components

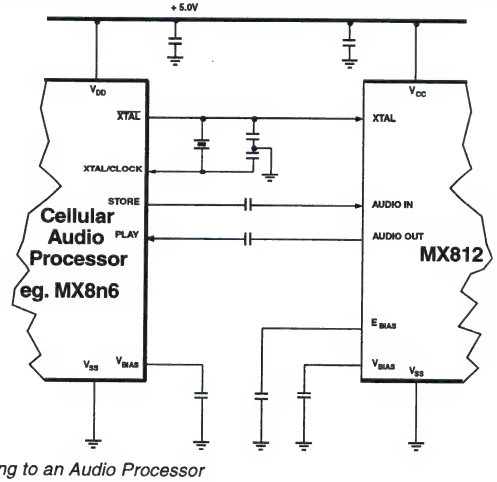


Figure 3 - Interfacing to an Audio Processor

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480076.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Application Information .....

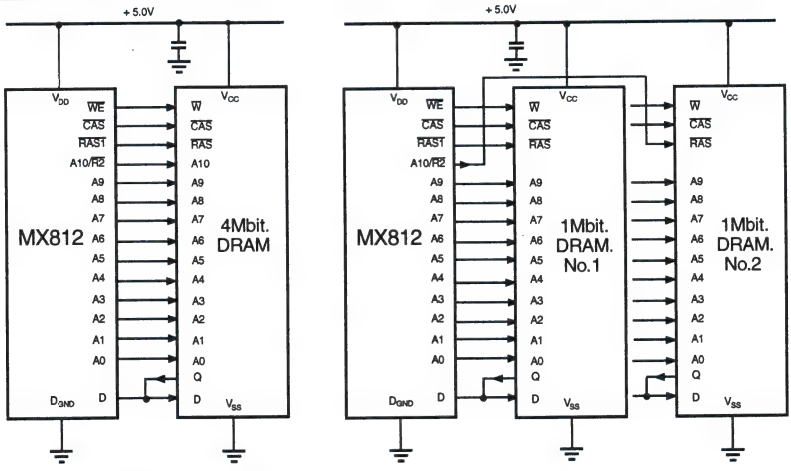


Figure 4 - Example DRAM Connections

Choice of DRAM Devices

DRAM devices chosen should be standard 1,048,576 x 1 or 4,194,304 x 1 Dynamic Random Access memories, with 'CAS before RAS' refresh, and a Row Address access time of 200 nano-seconds or less.

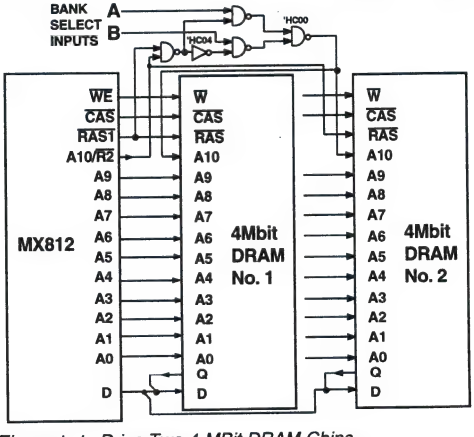


Figure 5 - Use of External Elements to Drive Two 4-MBit DRAM Chips

Driving Two 4-MBit DRAM Sections

By adding external logic circuitry, the MX812 can be configured to drive two 4-MBit DRAM sections. This will have the effect of doubling the available storage time. i.e. 4 minutes at 32kbps.

With reference to the circuitry shown in Figure 5: With the Mode Register **MS** Bit set to "0" the MX812 treats the DRAM sections as two 1-Mbit devices. The external logic makes each 4-MBit DRAM appear as four 1-MBit banks selected by the Bank Select lines '**A**' and '**B**.'

Bank Select Inputs A	B	DRAM No 1 Pages 0 – 1023	DRAM No 2 Pages 1024 – 2047
0	0	■	■
1	0	■	■
0	1	■	■
1	1	■	■

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480076.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

The Controlling System: C-BUS Hardware Interface

C-BUS is MX-COM's proprietary standard for the transmission of commands and data between a µController and MX-COM's New Generation integrated circuits. C-BUS is designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer can choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the MX812 VSR Codec is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the MX812. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex.	Binary MSB LSB	+	Data Byte/s
General Reset	01	0 0 0 0 0 0 0 1		
Write to Mode Register	60	0 1 1 0 0 0 0 0	+	1 byte Instruction to Mode Register
Read Status Register	61	0 1 1 0 0 0 0 1	+	1 byte Reply from Status Register
Store/Play Page	62	0 1 1 0 0 0 1 0	+	2 bytes Command
Wait	63	0 1 1 0 0 0 1 1		

Table 1 – C-BUS Address/Commands

"Write to Mode Register"

– A/C 60_H, followed by 1 byte of Command Data.

Interrupt Output – IE
Controls the MX812 IRQ output driver.

Sampling Rates – SR
The CVSD Codec sampling rates. Accurate rates depend upon the applied Xtal/clock frequency (see Table 5).

Memory Size – MS
The MX812 can operate with 1 x 1Mbit, 2 x 1Mbit or 1 x 4Mbit of DRAM (see Figure 4).

Powersave – PS
Powersaves the CVSD Codec only. Logic functions and DRAM refresh are maintained.

Decode/Encode – DE
The Codec and DRAM operational mode."
"Play" or "Store"

Setting	*Mode Bits*
MSB	***Transmitted to 812 First***
7	**Interrupt Output**
1	Enable
0	Disable
6	**Sampling Rate**
1	63kb/s
0	32kb/s
5	**Memory (DRAM) Size**
1	Single 4Mbit
0	1 or 2 x 1Mbit
4	**Powersave**
1	CVSD Codec Powersaved
0	CVSD Codec Powered
3	**Decode/Encode**
1	Decode – Play Mode
0	Encode – Store Mode
2 1 0	**Not Used**
0 0 0	Set to 'zeros'

Table 2 - Control Register

Interrupts

The MX812's Interrupt Output is driven by the Status Bit 7 (IF) when the Mode Register Bit7 (IE) is set to a "1."

The IF bit and the Interrupt Output (If enabled) are set when the Store/Play/Wait command Buffer is emptied (MT bit) by transferring from the buffer to the DRAM control circuits.

and/or

The IF bit and the Interrupt Output (if enabled) are set when a Store, Play or Wait command has finished **and** the Command Buffer is empty.

The notes below illustrate the $\overline{IRQ}$ pin conditions:

IF Bit	IE Bit	$\overline{IRQ}$
"0" cleared	"0" disable	High Z
"0" cleared	"1" enable	High Z
"1" Interrupt	"0" disable	High Z
"1" Interrupt	"1" enable	V_{ss} (logic "0")

"General Reset" – A/C 01_H

Upon Power-Up the "bits" in the MX812 registers will be random (either "0" or "1"). A General Reset Command (01_H) will be required to "reset" all microcircuits on the C-BUS, and has the following effect upon the MX812.

Clear all Mode Register bits to "0"
Status Register Bit 7 (IF) to "0"
Bits 5 and 6 (MT and I) to "1"
Halt any current Store, Play or Wait execution
Clear the Store/Play/Wait Command Buffer

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480076.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

The Controlling System .....

"Read Status Register" – A/C 61_H, followed by 1 byte of Reply Data.

Reading	Status Bits
MSB	*Received from 812 First*
7	**Interrupt Condition (Flag)**
1	Bit 6 or 5 set to a "1"
0	Cleared condition
6	**Command Buffer**
1	Buffer Empty
0	Cleared condition
5	**Device Condition**
1	Idle
0	Storing, Playing or Waiting
4 3 2 1 0	**Input Power Level**

Table 3 Status Register

Interrupt Condition (Flag) – IF
Set to a logic "1" whenever Bit 6 or Bit 5 goes from "0" to "1" (unless the transition is caused by a General Reset command 01_H). This indication allows monitoring by 'poll' while Interrupts are disabled.
Cleared to a logic "0" by a General Reset command or immediately following a read of the Status Register.

Command Buffer Status – MT
Set to a logic "1" when the Command Buffer is empty or by a General Reset command.
Cleared to a logic "0" by loading a new Store, Play, Wait commands.

Device Condition – I
Set to a logic "1" when **NO** Store, Play or Wait command is being executed or by a General Reset command.
Set to a logic "0" while a Store, Play or Wait command is being executed.

Encode Input Power Level – POWER
Available in the Encode mode, a 5-bit representation of the analog signal input level, updated at the end of every Store or Wait command.

Store/Play/Wait Command Buffer

A buffer used to accept and hold the latest Store, Play or Wait command received over the C-BUS while the MX812 is executing the previous command. The Status Register, bit 6, indicates the condition of this buffer.

When a command is received it is first loaded into this buffer. If the MX812 is already executing a previously loaded Store, Play or Wait command the new command will be stored temporarily in the Command Buffer, from where it will be taken on completion of the previous command.

This permits the MX812 to perform a continuous sequence of Store, Play or Wait commands, without gaps and without requiring an unduly fast response from the mController.

Note that this Command Buffer can only hold one Store, Play or Wait instruction, each new command received into this buffer will overwrite any previously loaded contents.

To Store or Play a sequence of pages the relevant commands should be loaded with sequential page numbers while observing the Status Register – Bit 6.

"Store/Play Page" – A/C 62_H, followed by 2 bytes of Command Data.

For the purposes of storage and replay, the attatched DRAM is divided into 'data-pages' of 1024 bits (1kbit).

One Store/Play command (loaded MSB first) will instruct the MX812 to store or play (depending upon the setting of the Mode Register, Bit-3) to or from 1 x 1024 "page" of DRAM. The Store/Play/Wait command buffer will allow continuity of operation.

The particular page selected is identified by the 12 lowest bits of the 2 x Store/Play bytes as shown below.

If a Store command is loaded and executed whilst the Codec is "Powersaved" in the Encode mode, the selected DRAM page will be filled with an idle pattern ("101010.....").

	MSB – Loaded to MX812 First				Bit Number											*Loaded Last – LSB*	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Bit
Value	x	x	x	x	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Value
Page	"0"	"0"	"0"	"0"	DRAM Page Number												Page

DRAM Size	Valid Page Nos	Bit Nos
4Mbit	0 – 4095	0 – 11
1 + 1Mbit	0 – 2047	0 – 10
1Mbit	0 – 1023	0 – 9

"Wait" – A/C 63_H, — Wait for 1024 bit periods

Causes the MX812 to wait for 1024 bit periods (approximately 16 or 32ms).

If the Codec is set to the Encode mode, a new "Power" reading that is relevant to the input audio level, will be loaded into the Status Register at the end of the Wait period.

If the Codec is set to the Decode mode it will 'Play' a perfect idle pattern ("101010.....") during the Wait period.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480076.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Control Timing Information

Figure 6 shows the timing parameters for two-way communication between the µController and Cellular peripherals on the "C-BUS." Figure 7 shows the timing relationships between the Serial Clock and Data.

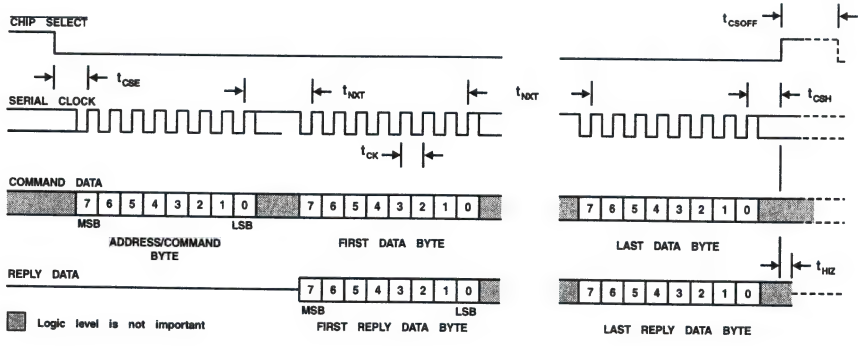


Figure 6 - Control Timing Information

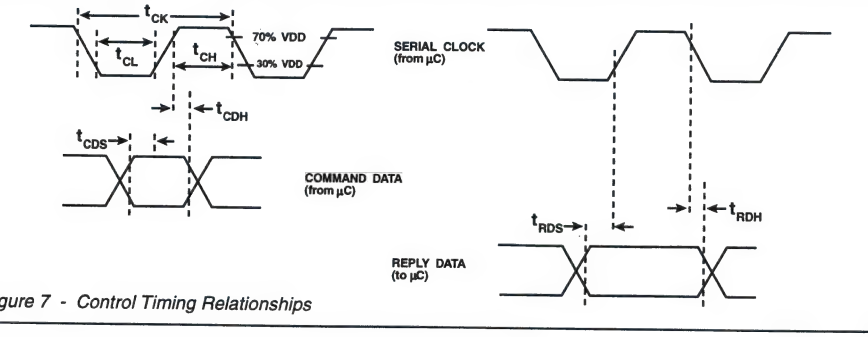


Figure 7 - Control Timing Relationships

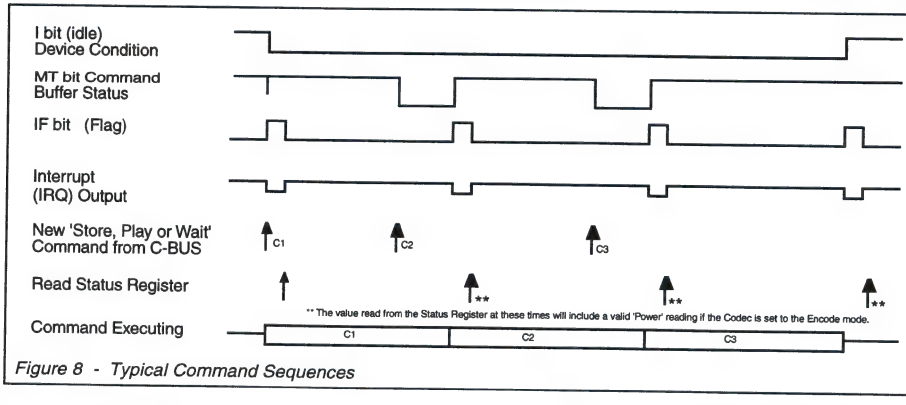

I bit (idle) Device Condition
MT bit Command Buffer Status
IF bit (Flag)
Interrupt (IRQ) Output
New 'Store, Play or Wait' Command from C-BUS
C1
C2
C3
Read Status Register
** The value read from the Status Register at these times will include a valid 'Power' reading if the Codec is set to the Encode mode.
Command Executing
C1
C2
C3

Figure 8 - Typical Command Sequences

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480076.003

Control Timing Information .....

Timing Specification – Figures 6 and 7

Characteristics		See Note	Min.	Typ.	Max.	Unit
t_{CSE}	"CS-Enable to Clock-High"		2.0	–	–	µs
t_{CSH}	Last "Clock-High to CS-High"		4.0	–	–	µs
t_{HIZ}	"CS-High to Reply Output Tri-state"		–	–	2.0	µs
t_{CSOFF}	"CS-High" Time between transactions		2.0	–	–	µs
t_{CK}	"Clock-Cycle" Time		2.0	–	–	µs
t_{NXT}	"Inter-Byte" Time		4.0	–	–	µs
t_{CH}	"Serial Clock-High" Period		500	–	–	ns
t_{CL}	"Serial Clock-Low" Period		500	–	–	ns
t_{CDS}	"Command Data Set-Up" Time		250	–	–	ns
t_{CDH}	"Command Data Hold" Time		0	–	–	ns
t_{RDS}	"Reply Data Set-Up" Time		250	–	–	ns
t_{RDH}	"Repy Data Hold" Time		50.0	–	–	ns

Address Line Decoding

MA0 to MA21 are the outputs of the internal 22-bit DRAM address counter, which are time multiplexed as 'Row' and 'Column' addresses onto the DRAM address lines A0 to A10 etc., as shown below.

Memory Size (MS) Bit = "1" – 4Mbit DRAM

Pin	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10/R2
Row Address	MA0	MA2	MA4	MA6	MA8	MA10	MA12	MA14	MA16	MA18	MA20
Column Address	MA1	MA3	MA5	MA7	MA9	MA11	MA13	MA15	MA17	MA19	MA21

Memory Size (MS) Bit = "0" – 1Mbit DRAM(s)

Pin	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9
Row Address	MA0	MA2	MA4	MA6	MA8	MA10	MA12	MA14	MA16	MA18
Column Address	MA1	MA3	MA5	MA7	MA9	MA11	MA13	MA15	MA17	MA19

MA20	MA21	RAS1	A10/R2	DRAM Selected
0	x	active		"first"
1	x		active	"second"

x = don't care

Table 4 Address Line Decoding

Sample Rate (SR) Bit	Division Ratio	Xtal/clock Frequency (MHz) 4.0	4.032	4.096
SR = "1"	64 kbps	62.5 kbps	63 kbps	64 kbps
SR = "0"	128 kbps	31.25 kbps	31.5 kbps	32 kbps
			Internal Clock Rate	
Local Decoder Clock		125 kHz	126 kHz	128 kHz

Table 5 Sampling Clock Rates Available

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480076.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Performance

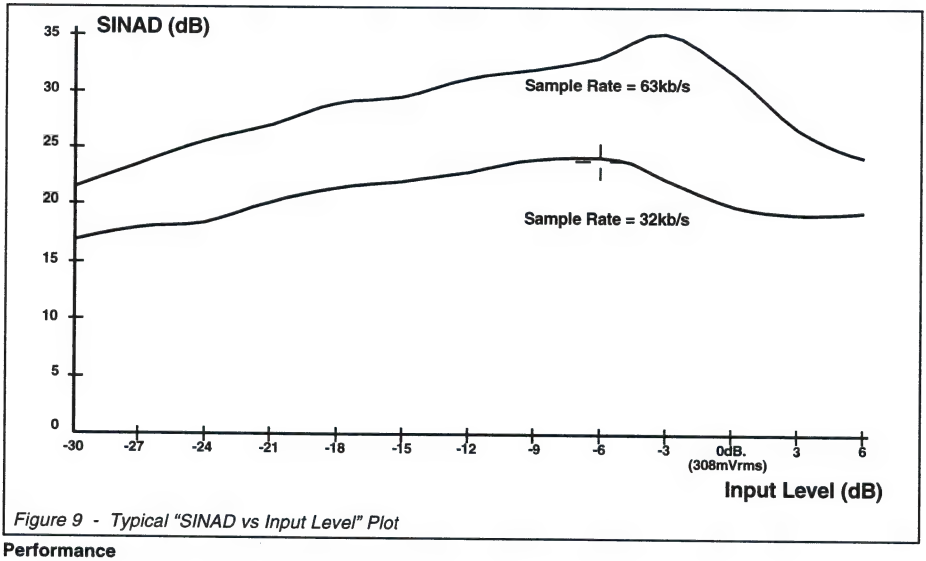


Figure 9 - Typical "SINAD vs Input Level" Plot

Performance

Figure 9 Shows a typical graph of SINAD vs Input Level produced for both 32kbps and 63kbps sample rates at an input frequency of 1.0kHz.

Figure 10 shows a typical graph of the "Power" reading for increasing input signal levels. The "Power" figure (0 to 31) is the binary figure obtained from the 5-bit representation in the Status Register - Bits 0, 1, 2, 3 and 4 while the Codec is selected to the Encode mode.

This reading is updated at the end of every Store or Wait command; Excessive input signal levels will record "11111_2" (31_{10}).

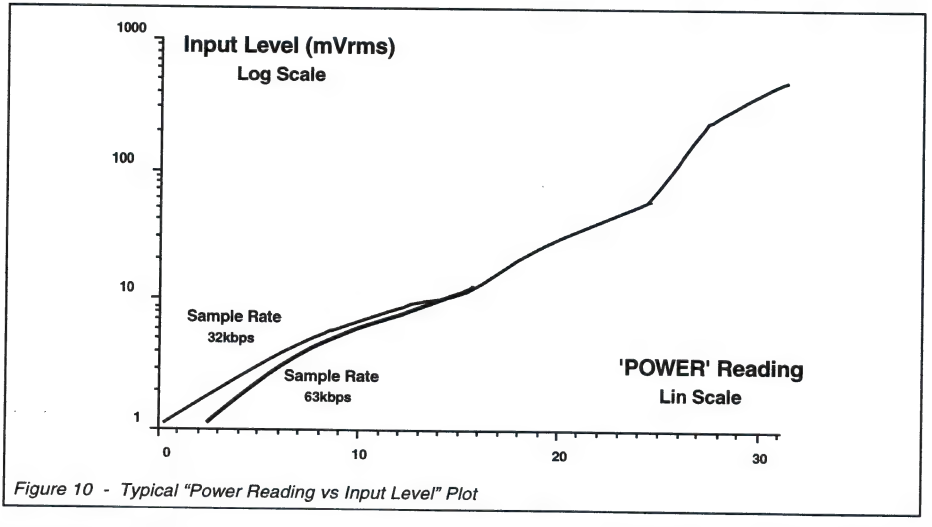


Figure 10 - Typical "Power Reading vs Input Level" Plot

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480076.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD}+0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/Clock f_0 = 4.00MHz

Audio Level 0dB ref = 308mVrms @ 1kHz

Reply Data Line loaded with 50pF/200kΩ to V_{SS}

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Enabled	1	–	3.0	–	mA
Powersaved	1	–	1.0	–	mA
Analog Input Impedance		–	100	–	kΩ
Analog Output Impedance (Decode)		–	1.0	–	kΩ
Analog Output Impedance (Encode or Powersave)		–	500	–	kΩ
DRAM Interface					
Input Logic "1"	2	3.5	–	–	V
Input Logic "0"	2	–	–	1.5	V
Output Logic "1" (at I_o = -120µA)	3	2.7	–	–	V
Output Logic "0" (at I_o = 120µA)	3	–	–	0.4	V
Input Leakage Current (at V_{IN} = 0 to V_{DD})	4	-1.0	–	1.0	µA
Input Capacitance	2	–	10.0	–	pF
Digital Interface					
Input Logic "1"	5	3.5	–	–	V
Input Logic "0"	5	–	–	1.5	V
I_{IN} (logic "1" or "0")	5	-1.0	–	1.0	µA
Output Logic Levels					
Output Logic "1" (-120µA)	6	4.6	–	–	V
Output Logic "0" (360µA)	7	–	–	0.4	V
I_{Out} Tri-state (logic "1" or "0")	6	-4.0	–	4.0	µA
Input Capacitance	5	–	–	7.5	pF
IOX (V_{Out} = 5V)	8	–	–	4.0	µA

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480076.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Dynamic Values					
"Xtal" Pin Input Frequency Range	12	4.0		4.1	MHz
Store Mode					
Analog Input Signal Levels	9	-24.0	–	4.0	dB
Analog Input Signal Frequency Range	9, 10	300		3400	Hz
Recommended Signal Source Impedance	9	–	–	2.0	kΩ
Play Mode					
Analog Output Signal Levels	13	-7.0	–	-5.0	dB
Output Noise (idle)	11	–	-55.0	–	dBp
Overall 'Store to Play' Performance					
Output Noise (Input Short Circuit)	11	–	-50.0	–	dBp
SINAD (**SR** = 32kb/s)					
(Input = 1.0kHz @ -6.0dB)	11	–	23.0	–	dB

Notes

1. Not including DRAM current.
2. D input from DRAM
3. Outputs to DRAM.
4. All digital inputs.
5. Serial Clock, Command Data and Chip Select inputs.
6. Reply Data output.
7. Reply Data and Interrupt ($\overline{IRQ}$) outputs.
8. Leakage current into the "Off" Interrupt ($\overline{IRQ}$) output.
9. For optimum performance.
10. Input filtering must be performed at the source.
11. Measured in conjunction with the FX836 R2000 system Audio Processor.
12. For full C-BUS compatibility.
13. Playback of a stored "-6.0dB 1.0kHz Test Signal."

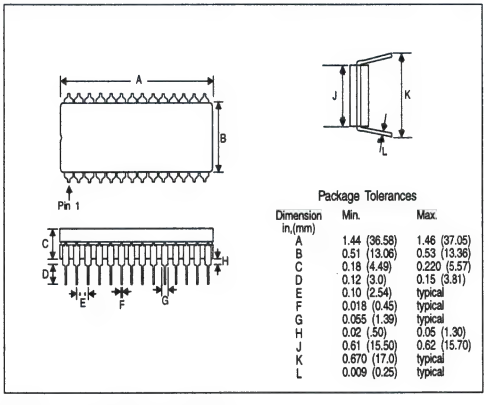
© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480076.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Package Outline

Figure 11 shows the MX812J Ceramic Dual In-Line, or Cerdip, Package. The MX812DW is shown in Figure 12. Pin 1 is marked with an indent spot on each chip. Pins number counter-clockwise when viewed from the top side.

Handling Precautions

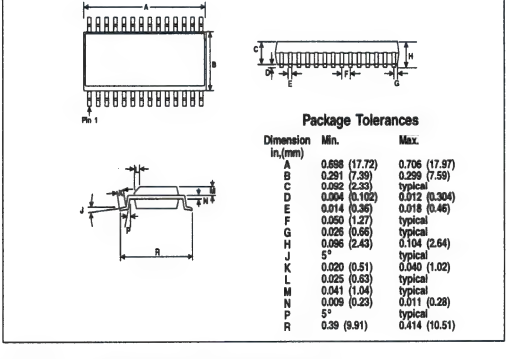
The MX812 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.



Package Tolerances

Dimension in.(mm)	Min.	Max.
A	1.44 (36.58)	1.46 (37.05)
B	0.51 (13.06)	0.53 (13.36)
C	0.18 (4.49)	0.220 (5.57)
D	0.12 (3.0)	0.15 (3.81)
E	0.10 (2.54)	typical
F	0.018 (0.45)	typical
G	0.055 (1.39)	typical
H	0.02 (.50)	0.05 (1.30)
J	0.61 (15.50)	0.62 (15.70)
K	0.670 (17.0)	typical
L	0.009 (0.25)	typical

Figure 11 - MX812J 28-pin Cerdip



Package Tolerances

Dimension in.(mm)	Min.	Max.
A	0.698 (17.72)	0.706 (17.97)
B	0.291 (7.39)	0.299 (7.59)
C	0.092 (2.33)	typical
D	0.004 (0.102)	0.012 (0.304)
E	0.014 (0.36)	0.018 (0.46)
F	0.050 (1.27)	typical
G	0.026 (0.66)	typical
H	0.096 (2.43)	0.104 (2.64)
J	5°	typical
K	0.020 (0.51)	0.040 (1.02)
L	0.025 (0.63)	typical
M	0.041 (1.04)	typical
N	0.009 (0.23)	0.011 (0.28)
P	5°	typical
R	0.39 (9.91)	0.414 (10.51)

Figure 12 - MX812DW SOIC-28 Package

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480076.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Technical Specifications

Section 6:
Voice Processor IC's

Device	Description	Page
MX506	Mobile Radio Audio Processor	3
MX806A	Audio Processor	21
MX829	Baseband Signal Processor	35
MX980	Digital Radio Baseband Processor for π/4 DQPSK TETRA	61

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

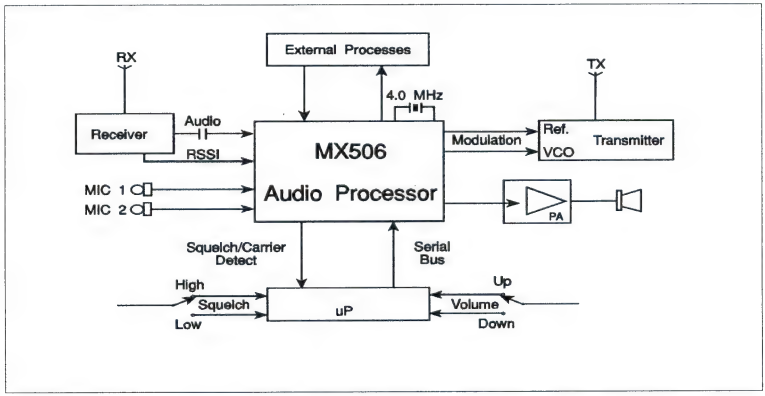
MX506 MOBILE RADIO AUDIO PROCESSOR

C-BUS COMPATIBLE

PRELIMINARY INFORMATION

Features/Applications

- **Rx and Tx Filtering to TIA/CEPT Standards**
- **Digital Level Control for Volume, Noise Squelch, and RSSI**
- **Tx VOGAD Circuitry**
- **Serial µP Control of ALL Chip Functions**
- **Deviation Limiter**
- **Military/Marine and Mobile Radio Application**
- **FM/AM/SSB Applications**
- **16kbps Data and Voice Scrambler Compatible**
- **Low-Power 5-Volt CMOS Process**



Brief Description

The MX506 is a µProcessor-controlled, single-chip device containing ALL the circuit elements necessary to perform the audio functions of a mobile (or portable) radio system.

On-chip signal paths include: speech-band/pre-emphasis filters, variable gain/attenuation stages, voice-compression and deviation limiter circuitry.

Each function in the signal path can be addressed or by-passed - *providing "real-time," dynamic control* -by the µProcessor. This half-duplex device comprises two separate audio signal paths.

The Pre-Process Path performs filtering and level adjustment on audio (Rx or Tx) for use in auxiliary systems such as "Frequency Inversion Scrambling," "Sub-Audio" tone or "In-Band" data signalling. This path is output at the "Pre-Process Audio Output" pin. If no external processes are being used this output should be connected to the "Pre-process Audio Input"pin.

The Post-Process Path can adjust and prepare the input audio for output to the chosen transmitter driver or loudspeaker amplifier.

Suitably software configured, the MX506, which can operate on voice, direct-digital or tone-data and sub-audio frequencies, is compatible with FM, AM and SSB type transceivers. Digital gain elements are provided on-chip for dynamic control and balance of signal-path levels during manufacturing, test and operation.

System Squelch, a separate path, is sourced from either the incoming signal or Received Signal Strength Indication (RSSI) from the radio circuitry.

The MX506, a low-power 5-volt CMOS device, is available in 24-pin/lead plastic DIL and SMD packages.

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.

Packages P/LG/LH	
1	**$\overline{\text{Xtal}}$:** The output of the 4.0MHz on-chip clock oscillator.
2	**Xtal/Clock:** The input to the on-chip 4.0MHz clock oscillator inverter. All oscillator components are included on-chip. A 4.0MHz Xtal or externally derived clock should be connected here. See Figure 2.
3	**V_{DD}:** Positive supply rail. A single, stable +5-volt supply is required. Levels and voltages within the Audio Processor are dependent upon this supply.
4	**Post Process Audio Input:** The analog input to the Post-Process Path from external audio operations. Inputs to this pin should be a.c. coupled via a capacitor C_7. See Figures 2 and 4.
5	**Pre-Process Audio Output:** The analog output to external audio operations. See Figure 4.
6	**Rx Audio Input:** The input from the radio receiver demodulator. This input, which is required to be a.c. coupled via capacitor C_6, is selected by serial data. Audio at this input will be available for use as a signal-squelch noise source. See Figures 2 and 4.
7	**V_{BIAS}:** The output of the on-chip analog bias circuitry, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} via capacitor C_1. See Figure 2.
8	**CTCSS/Data Input:** To allow the introduction of sub-audio tones or data to the VCO drives. By manipulation of bits 17, 18 and 19 this input can be "mixed" into the signal path or added as a burst in between speech segments.
9	**Tx Audio Input:** The pre-process transmit audio input. This input can be driven from an external source or from the MX506 Mic. input circuitry. See Figures 2, 3 and 4.
10	**Mic. Output:** The output of the microphone multiplexer, selected by serial input data. If additional gain is required for the pre-process input, an external amplifier as shown in Figure 3 is recommended.
11	**Mic.1 Input:** These separate microphone audio inputs are individually selected by the serial input data. See Figures 2, 3 and 4.
12	**Mic.2 Input:**
13	**V_{SS}:** Negative supply rail (GND).
14	**Compression Capacitor:** External components connected to this pin provide the required compression time-constant. See Figure 2.
15	**Audio Output (Rx):** The received audio output from the Post-Process path. This output is data selected and when powersaved is held at V_{BIAS}.
16	**VCO Ref. Drive (Tx) Output:** The output to drive the modulation reference oscillator. This output is data selected and when powersaved is held at V_{BIAS}. To prevent any d.c. level at this output causing incorrect frequency selection it is recommended that a.c. coupling components as shown in Figure 2 are employed. For modulation down to near d.c., these components should be by-passed.
17	**VCO Drive (Tx) Output:** The output to drive the modulation VCO. This output is data selected and when powersaved is held at V_{BIAS}.
18	**RSSI:** The input to the Squelch Selection circuitry from the radio's Received Signal Strength Indicator output. A data selected input.
19	**Noise Input:** The noise level can be applied to this pin. This would be the Noise Output integrated by external components, as indicated in Figure 2, or an externally produced noise level.
20	**Noise Output:** The output of the on-chip "squelch noise rectifier". This output is a half-wave rectified d.c. level that can be applied to the Noise Input via external integrating components. This output could also be used by an external signal detector circuit. This output level is at V_{BIAS} for no input. See Figures 2, 3 and 4.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Packages P/LG/LH	
21	**Squelch Drive:** A TTL compatible output. The inputs to the comparator are: the logically selected threshold level from the Digital-to-Analog converter and the selected noise input. A logic "0" signifies that the noise threshold has been exceeded.
22	**Serial Clock:** The externally produced serial data loading clock input. See Figure 5. This input has an internal 1MΩ pullup resistor.
23	**Serial Data:** The controlling, 47-bit serial data input. With $\overline{\text{Chip Select}}$ maintained at a logic "0" the serial data is entered at this pin, loaded bit 46 first, bit 0 last. Detailed information on the allocation and function of serial data bits (0 to 46) is given in tabular form on later pages. Data load timing should be carried out as described in Figure 5. This input has an internal 1MΩ pullup resistor.
24	**$\overline{\text{Chip Select}}$:** The data loading control function. During serial loading this input should be operated as shown in Figure 5. New data is latched on the rising edge of this waveform. This input has an internal 1MΩ pullup resistor.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

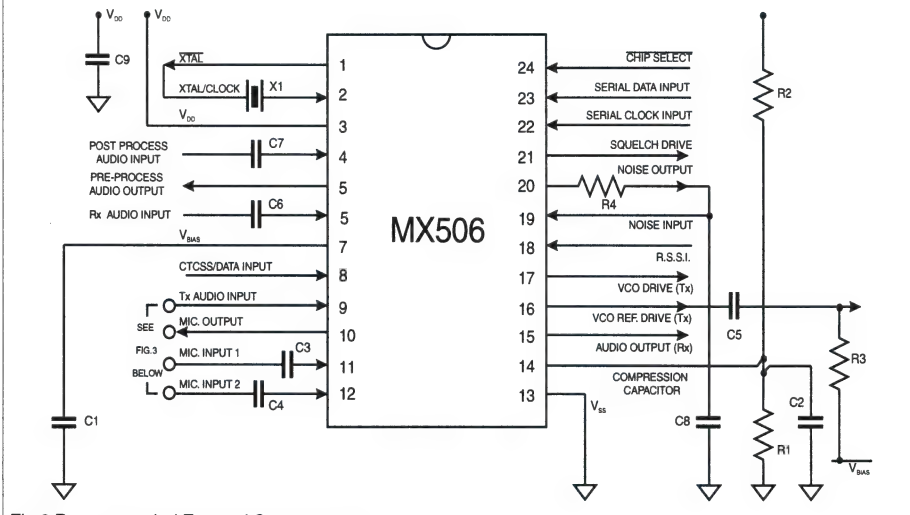


Fig.2 Recommended External Components

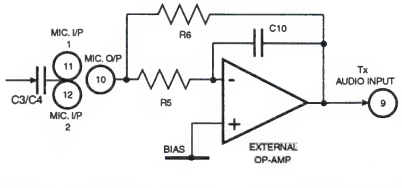


Fig.3 Typical 2nd Order Pre-emphasis Input Circuit

Notes

For dual Tx inputs using both Mic.1 and Mic.2 inputs without pre-emphasis, capacitors C_3 and C_4 will be required as shown in Figure 2.

If pre-emphasis is required, the external circuit shown in Figure 3 is recommended.

The Op-Amp selected for this application should be of a "low noise wide-bandwidth" type i.e. with at least 60dB of gain at 6kHz.

In addition to the components shown in Figure 2, it is recommended that the power and V_{BIAS} lines to the external Op-Amp are decoupled to V_{SS} *physically close to the amplifier*, by a 1.0µF capacitor.

Circuit References

Component	Value	Tolerance						
R_1	100kΩ	± 10%	C_1	1.0µF	± 20%	C_7	0.1µF	± 20%
R_2	390kΩ	± 10%	C_2	6.8µF	± 20%	C_8	0.1µF	± 20%
R_3	100kΩ	± 1%	C_3	1.0nF	± 1%	C_9	1.0µF	± 20%
R_4	10kΩ	± 10%	C_4	1.0nF	± 1%	C_{10}	12.0pF	± 1%
R_5	18.0kΩ	± 1%	C_5	15nF	± 1%			
R_6	2.7MΩ	± 1%	C_6	0.1µF	± 20%	X_1	4.0MHz	

Layout Recommendations

Audio microcircuit performance will be affected by external noise.

All external components should be kept as close to the device as possible.

Tracks to the device should be kept short, particularly the Audio and V_{BIAS} inputs.

A "ground-plane" connected to V_{SS} will help to eliminate external pick-up.

Ensure that all inputs (analog and d.c.) are free from noise.

Xtal/clock and digital tracks should be kept well away from analog circuitry. Analog inputs and outputs should be screened wherever possible with high-level outputs isolated from very low-level inputs.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

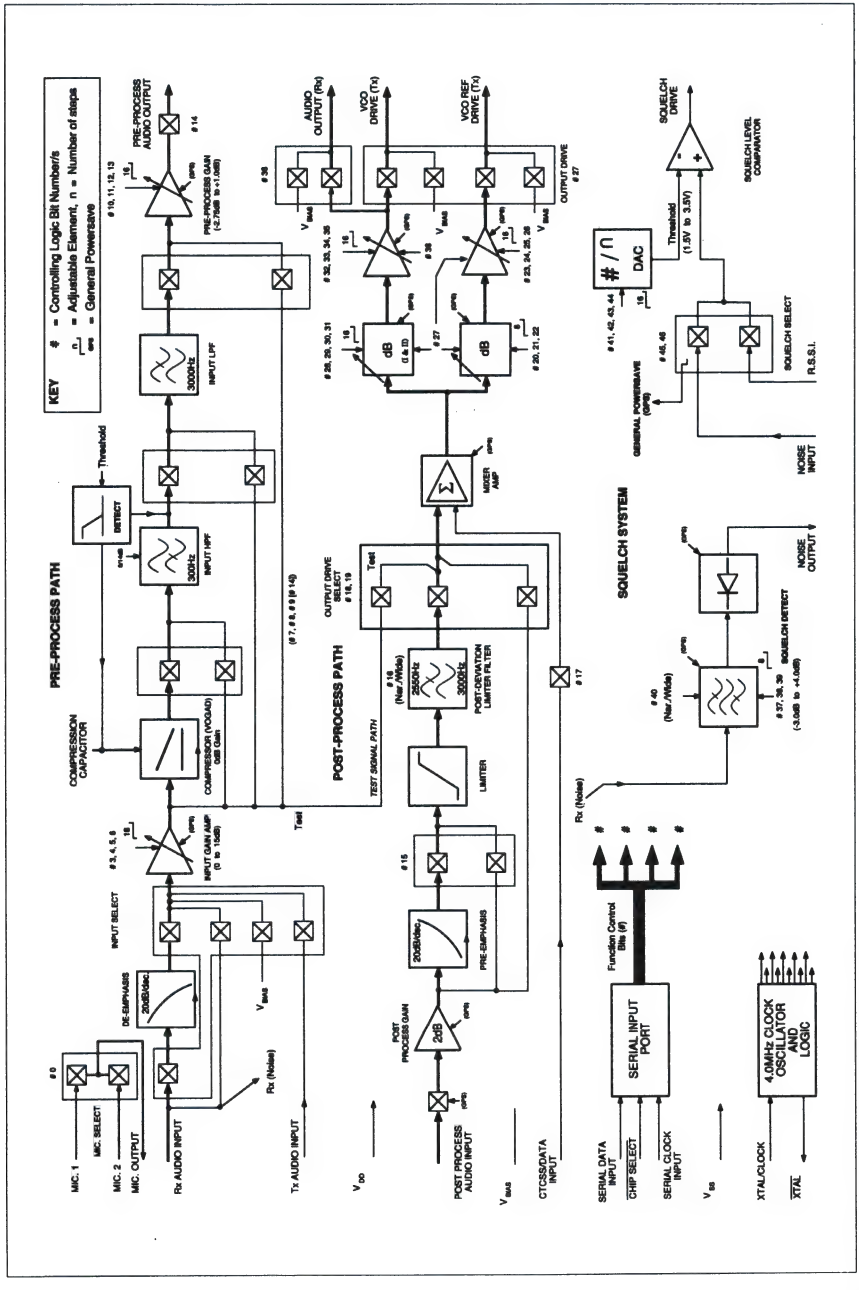


Figure 4: LMR Audio Processor Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Control bits (LSB) loaded last	Function	Notes
0	**Mic. Select**	A multiplexed "microphone" input allowing the use of differing type and level voice inputs.
0	- Microphone Input 1	
1	- Microphone Input 2	
1 2	**Input Select**	Transmit or receive audio sources are selected, inserting the appropriate path gain for the chosen input. The input path can be set to bias whilst allowing receiver noise monitoring.
0 0	- Rx Input De-emphasis Bypass; HPF to 0dB	
0 1	- Rx Input De-emphasis Select; HPF to 0dB	
1 0	- Tx Input Powersave De-emphasis; HPF to 14dB	
1 1	- Path Input to V_{BIAS}; Powersave De-emphasis	
3 4 5 6	**Input Gain Amplifier**	A gain element intended to adjust the drive level to the compressor, catering for differing signal sources and microphone sensitivities.
0 0 0 0	- Gain Set 0.0dB	
1 0 0 0	1.0dB	
0 1 0 0	2.0dB	
1 1 0 0	3.0dB	
0 0 1 0	4.0dB	
1 0 1 0	5.0dB	
0 1 1 0	6.0dB	
1 1 1 0	7.0dB	
0 0 0 1	8.0dB	
1 0 0 1	9.0dB	
0 1 0 1	10.0dB	
1 1 0 1	11.0dB	
0 0 1 1	12.0dB	
1 0 1 1	13.0dB	
0 1 1 1	14.0dB	
1 1 1 1	15.0dB	

7 8 9 14	***Compressor***	***HPF***	***LPF***	***Pre-Process Output***
1 1 1 ***1***	Enabled	Enabled	Enabled	Enabled
0 1 1 ***1***	Powersaved	Enabled	Enabled	Enabled
X 0 1 ***1***	Powersaved	Powersaved	Enabled	Enabled
X X 0 ***1***	Powersaved	Powersaved	Powersaved	Enabled
X X X ***0***	Powersaved	Powersaved	Powersaved	Powersaved

The Pre-Process Path LPF should be selected, when measuring the response to Tx Mod. frequencies exceeding 3kHz.

10 11 12 13	**Pre-Process Gain**	An in-line output drive stage providing adjustable gain or attenuation to compensate for level tolerances in the external audio processes and peripherals. The output of this amplifier stage is available for further voice (audio) processing such as "Frequency Inversion Voice Scrambling."
0 0 0 0	- Gain Set -2.75dB	
1 0 0 0	-2.50dB	
0 1 0 0	-2.25dB	
1 1 0 0	-2.00dB	
0 0 1 0	-1.75dB	
1 0 1 0	-1.50dB	
0 1 1 0	-1.25dB	
1 1 1 0	-1.00dB	
0 0 0 1	-0.75dB	
1 0 0 1	-0.50dB	
0 1 0 1	-0.25dB	
1 1 0 1	0dB	
0 0 1 1	0.25dB	
1 0 1 1	0.50dB	
0 1 1 1	0.75dB	
1 1 1 1	1.00dB	
14	**Pre-Process Output**	Bit 14 is the Enable/Powersave function for the Pre-Process output stages. See *Bits 7 8 9 14 .....*
0	- Disable Pre-Process Output Output at V_{BIAS}	
1	- Enable Pre-Process Audio Output	*Reference ..... Figure 4*

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.

Control bits	Element	Notes
	Post-Process Gain	A fixed 2.0dB gain stage.
15	**Pre-emphasis**	A selectable pre-emphasis stage set around 1.0kHz, with a characteristic of 6dB per octave. It is available for use when transmitting data signals such as MSK. See Table below for Powersave information.
	Deviation Limiter	A pre-set amplitude limiting stage for deviation control.
	and	
16	**Post-Deviation Limiter Filter**	This lowpass filter which is selected with the Deviation Limiter, is adjustable to Narrow (2550Hz) and Wide (3000Hz) bandwidths, allowing for different channel-spacing requirements.
0	- Narrow filter bandwidth, cut-off = 2550Hz.	
1	- Wide filter bandwidth, cut-off = 3000Hz.	
17	**CTCSS/Data Input**	
0	- Disable Input path to Mixer system	
1	- Enable Input path to Mixer system	

15	*18*	*19*	*Pre-Emphasis*	*Limiter and Post-Dev LPF*	*Drive Selected*
X	0	0	Powersaved	Powersaved	Test Path
0	1	0	Powersaved	Enabled	Post-ProcessPath
1	1	0	Enabled	Enabled	Post-Process Path
X	1	1	Powersaved	Powersaved	Post-Process Bypass
X	0	1	Powersaved	Powersaved	Bias

20	*21*	*22*	**VCO Reference Drive Attenuator**	The in-line control attenuator for the VCO reference channel drive output.
0	0	0	- Gain Set -28dB	
1	0	0	-24dB	
0	1	0	-20dB	
1	1	0	-16dB	
0	0	1	-12dB	
1	0	1	-8.0dB	
0	1	1	-4.0dB	
1	1	1	0.0dB	

23	*24*	*25*	*26*	**VCO Reference Drive Amplifier**	The in-line control amplifier/attenuator for the VCO reference channel drive output.
0	0	0	0	- Gain Set -2.75dB	
1	0	0	0	-2.50dB	
0	1	0	0	-2.25dB	
1	1	0	0	-2.00dB	
0	0	1	0	-1.75dB	
1	0	1	0	-1.50dB	
0	1	1	0	-1.25dB	
1	1	1	0	-1.00dB	
0	0	0	1	-0.75dB	
1	0	0	1	-0.50dB	
0	1	0	1	-0.25dB	
1	1	0	1	0dB	
0	0	1	1	0.25dB	
1	0	1	1	0.50dB	
0	1	1	1	0.75dB	
1	1	1	1	1.00dB	

27	**Output Drive Control**	Used in conjunction with Bit 36 to control output functions. *Reference ..... Figure 4*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Control bits	Element	Notes
28 29 30 0 0 0 1 0 0 0 1 0 1 1 0 0 0 1 1 0 1 0 1 1 1 1 1	**VCO Drive Attenuator I** - Gain Set -22.4dB -19.2dB -16.0dB -12.8dB -9.6dB -6.4dB -3.2dB 0dB	An in-line control attenuator for the VCO Tx channel drive output. This channel is also selected as Audio Output (Rx) under the control of bit 36. This attenuator can be used in a volume control application.
31 0 1	**VCO Drive Attenuator II** - Gain Set -25.6dB 0dB	An in-line control attenuator for the VCO Tx channel drive output. As an example, when bits 28 to 31 are set to "0", the gain set is -48.0dB (-22.4 + -25.6).
32 33 34 35 0 0 0 0 1 0 0 0 0 1 0 0 1 1 0 0 0 0 1 0 1 0 1 0 0 1 1 0 1 1 1 0 0 0 0 1 1 0 0 1 0 1 0 1 1 1 0 1 0 0 1 1 1 0 1 1 0 1 1 1 1 1 1 1	**VCO Drive Amplifier** - Gain Set -2.75dB -2.50dB -2.25dB -2.00dB -1.75dB -1.50dB -1.25dB -1.00dB -0.75dB -0.50dB -0.25dB 0dB 0.25dB 0.50dB 0.75dB 1.00dB	The in-line control amplifier/attenuator for the VCO Tx channel drive output. This channel is also selected as Audio Output (Rx) under the control of bit 36. This amplifier can be used in a volume control application.
27 36 0 0 0 1 1 0 1 1	*VCO Drive (Tx) Output*: Bias / Bias / Enabled / Enabled *VCO Ref (Tx) Output*: Bias / Bias / Enabled / Enabled *Audio Output (Rx)*: Bias / Enabled / Bias / Enabled The Drive and Ref. paths are powersaved by Bits 45 and 46 in the "Total Powersave" or "Listening Powersave" conditions. When making internal changes it is recommended that these outputs are disconnected *(placed in a bias condition)* from the relevant output (load) circuitry.	
37 38 39 0 0 0 1 0 0 0 1 0 1 1 0 0 0 1 1 0 1 0 1 1 1 1 1	**Squelch Filter (Gain)** - Gain Set -3.0dB -2.0dB -1.0dB 0dB 1.0dB 2.0dB 3.0dB 4.0dB	The squelch function is set by bits 45 & 46 (Squelch Source Selection). The center frequency gain of this element is 35dB, data selected gain variations (-3.0dB to 4.0dB) are around this value.
40 0 1	**Squelch Filter** (Narrow/Wide) - Narrow ($f_c \approx$ 18kHz ± 6.5kHz). - Wide ($f_c \approx$ 25kHz ± 8.5kHz).	For use in wide or narrow channel systems. The squelch function is set by bits 45 & 46 (Squelch Source Selection).

Reference ..... Figure 4

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.

Control bits				Element		Notes
41	*42*	*43*	*44*	**Squelch Threshold Voltage**		The fine squelch adjustment level from the Digital-to-Analog converter.
0	0	0	0	3.500V d.c.	70.0% V_{DD}	
1	0	0	0	3.366	67.3%	These threshold levels are used as a comparison with the selected input noise voltage (bits 45 and 46).
0	1	0	0	3.233	64.6%	
1	1	0	0	3.100	62.0%	
0	0	1	0	2.966	59.3%	Variation in V_{DD} will produce variation in threshold levels.
1	0	1	0	2.833	56.6%	
0	1	1	0	2.700	54.0%	
1	1	1	0	2.566	51.3%	
0	0	0	1	2.433	48.6%	
1	0	0	1	2.300	46.0%	
0	1	0	1	2.166	43.3%	
1	1	0	1	2.033	40.6%	
0	0	1	1	1.900	38.0%	
1	0	1	1	1.766	35.3%	
0	1	1	1	1.633	32.6%	
1	1	1	1	1.500	30.0%	
	45	*46*		**Squelch Source Selector**		As well as selecting the input to the Noise Comparator, these two bits produce additional General Powersave (GPS) functions which control those elements not having individual serial control.
	0	0		A "Total Powersave" condition		**Powersaved:** Input Gain Amp - Post Process (2dB) Gain Amp - Mixer Amp - Noise BPF - Noise Rectifier - Squelch Comparator
	1	0		Noise Input selected to Comparator		
	0	1		RSSI input selected to Comparator		
	1	1		Powersave but LISTENING condition RSSI input selected to Comparator		**Powersaved:** Input Gain Amp - Post Process (2dB) Gain Amp - Mixer Amp - Noise BPF - Noise Rectifier

Rx Noise Path

Any high-frequency noise (18kHz/25kHz) present at the Rx Audio Input will also be available at the Noise Output pin via the squelch filter and noise rectifier (when enabled) for use as a squelch detection level. This means that the MX506 can be set to "LISTEN" with the majority of circuit elements powersaved until an RSSI level is detected and produces a "Squelch Drive output."

Test Signal Path

This path, when selected, can be used as a direct path, via the Output Drive Selector (bits 18 and 19), to dynamically set and balance the VCO drive and reference output levels.

Reference ..... Figure 4

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

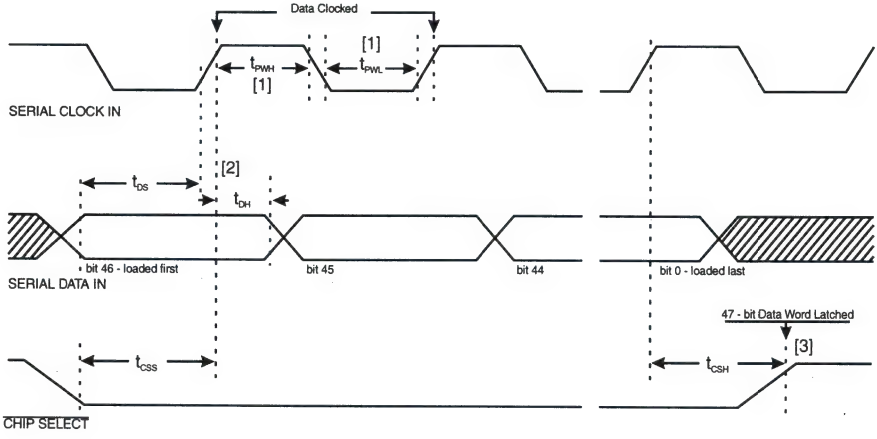


Fig.5 Data Load Timing Diagram

Data Loading

Serial Data bits, whose functions are described on the previous pages, are loaded to the MX506 using the timing format illustrated on this page. All 47 bits must be loaded. Data is loaded bit 46 first, bit 0 last.

Function			Min.	Typ.	Max.	Unit
Serial Clock	[1]					
"High" Pulse Width		t_{PWH}	600	-	-	ns
"Low" Pulse Width		t_{PWL}	600	-	-	ns
Serial Data	[2]					
Data Set-Up Time		t_{DS}	360	-	-	ns
Data Hold Time		t_{DH}	120	-	-	ns
$\overline{\text{Chip Select}}$	[3]					
Select Set-Up Time		t_{CSS}	600	-	-	ns
Select Hold Time		t_{CSH}	600	-	-	ns

[1] The Serial Clock pulses do not have to be symmetrical, as shown above, but pulse lengths must conform to the "minimum" time specification.

[2] Individual data bits (logic "1" or "0") are loaded to the device on the rising edge of the input Serial *Data* Clock pulse. The data hold period (t_{DH}) is to ensure that the data level is steady when it is sampled.

[3] The full 47-bit data word is latched into the device on the rising edge of the $\overline{\text{Chip Select}}$ waveform, at this time the loaded data is acted upon and the circuit configuration/settings will change.

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480014.003

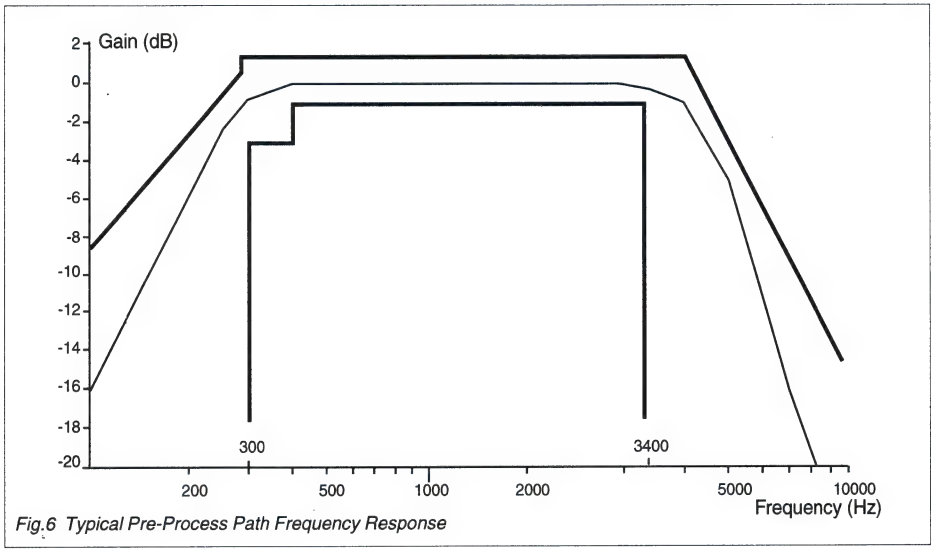


Fig.6 Typical Pre-Process Path Frequency Response

System Frequency Characteristics

Figure 6 shows a typical, response curve of the Pre-Process Path, in receive mode, set against the device specification. The general characteristic shape is produced by the Input Highpass and Lowpass Filters, without the internal pre-emphasis element.

Figure 7 shows a typical response curve of the Post-Process Path set against the device specification. The general characteristic shape is produced by the Post-Deviation Limiter Filter, without the de-emphasis element.

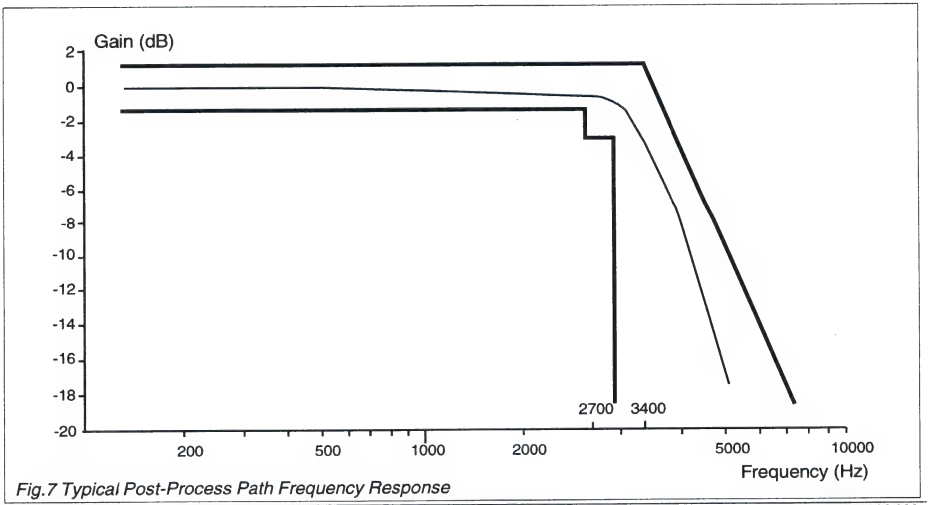


Fig.7 Typical Post-Process Path Frequency Response

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

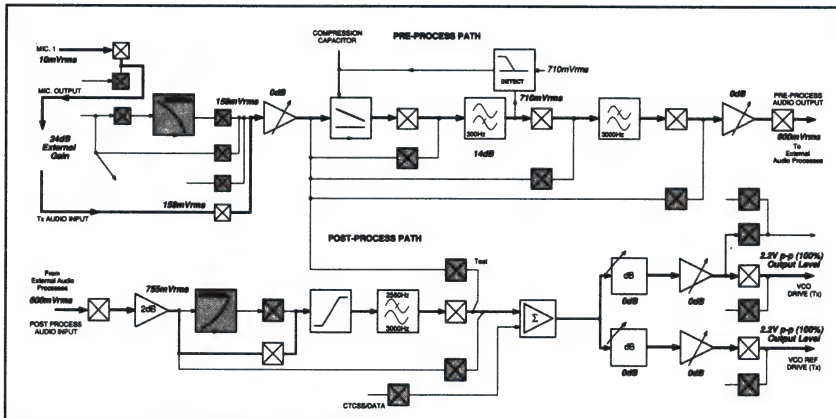


Fig.8 Transmit Path – Suggested Test Settings

☐ Active elements used in the signal path.	■ Powersaved or by-passed elements that are not employed in the signal path.

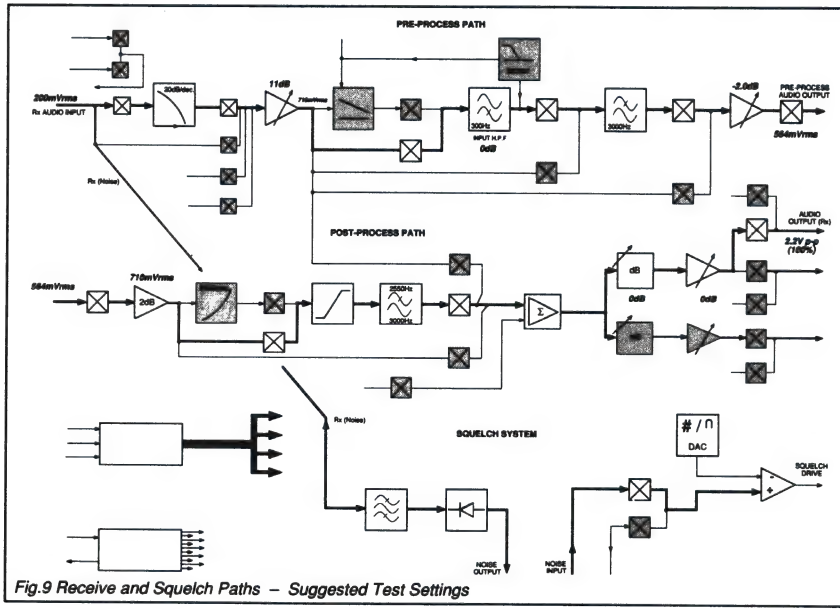


Fig.9 Receive and Squelch Paths – Suggested Test Settings

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Operational Information

The functions of the MX506 are selected and controlled using the 47-bit Serial Data Input. This application section assists in the familiarization of control by providing example operational paths and system confidence tests.

The signal levels employed in these examples are to demonstrate the functions of the device. Maximum and minimum operational signal levels are detailed in the "Specification" pages. A final output signal level of 2.2V p-p is considered, operationally, to be 100% (FM deviation).

Set-up and enter the example data word in accordance with Figures 2 and 4.
Test the MX506 using levels and points detailed in Tables 1, 2 and 3.

Experimentation will indicate the signal element configuration and required control settings for various input and output levels.

Transmit Path - *The Serial Data word below will produce the transmit element configuration shown in Figure 8.*

bit 0 - **01000001 11110110 X0101111 10111111 11010XXX XXXXX10** - bit 46

0 = logic 0 **1** = logic 1 **X** = not important to the example

Step	Input	Level (mV rms @ 1kHz)	Output	Level (mV rms @ 1kHz)	Note	Output Level Ref. to Max.
1	Mic. 1	10	Pre-Process Audio	750	Ext +24.0dB	
2	Ext. Audio Process In	750	VCO Drive/Ref.	1.54≤ V_{OUT} ≤2.2Vp-p		70- 100%
3	Mic. 1	4.8	Pre-Process Audio	410	Ext +24.0dB	60%
4	Ext. Audio Process In	410	VCO Drive and Ref.	466		60%

Table 1 Transmit Path Operational Check

To establish a 100% level for this device inject a large amplitude audio signal into the Post Process Audio Input, with the Limiter enabled.

Receive Path - *The Serial Data word below will produce the receive element configuration shown in Figure 9.*

bit 0 - **X0111010 11110010 X010XXXX XXX01111 11011XXX XXXXX10** - bit 46

0 = logic 0 **1** = logic 1 **X** = not important to the example

Step	Input	Level (mV rms @ 1kHz)	Output	Level (mV rms @ 1kHz)	Note	Output Level Ref. to Max.
1	Rx Audio In	200	Pre-Process Audio	564		
2	Ext. Audio Process In	564	Audio Out (Rx)	1.54≤ V_{OUT} ≤2.2Vp-p		70 -100%
3	Rx Audio In	145	Audio Out (Rx)	466		60%
4	Rx Audio In	145	Audio Out (Rx)	466±	vary bits 28 - 35 for Volume	60%±

Table 2 Receive Path Operational Check

To establish a 100% level for this device inject a large amplitude audio signal into the Post Process Audio Input, with the Limiter enabled.

Squelch Path - *The Serial Data word below will produce the squelch element configuration shown in Figure 9.*

bit 0 - **X00XXXXX XXXXXX0X X010XXXX XXX0XXXX XXXX1110 1110110** - bit 46

0 = logic 0 **1** = logic 1 **X** = not important to the example

Step	Input	Level (mV rms @ 25kHz)	Output	Level	Note
1	Rx Audio In	0	Squelch Drive	logic "1"	No noise - "Noise Out" = V_{BIAS}
2	Rx Audio In	50.0	Squelch Drive	logic "0"	Noise In - "Noise Out"decreases

Table 3 Squelch Path Operational Check

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current	(supply pins)	+/- 30mA
	(other pins)	+/- 20mA
Total device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**MX506P**	-30°C to +70°C (plastic)
	MX506LG/LH	-30°C to +70°C (plastic)
Storage temperature range:	**MX506P**	-40°C to +85°C (plastic)
	MX506LG/LH	-40°C to +85°C (plastic)

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V. T_{AMB} = 25°C. Xtal/Clock f_0 = 4.0MHz. Audio level 0dB ref: = 466mV rms @ 1.0kHz *(60% deviation, FM).*

Characteristics		See Note	Min.	Typ.	Max.	Unit
Static Values						
Supply Voltage			4.5	5.0	5.5	V
Supply Current	(All Elements Enabled)		-	8.0	-	mA
	(Listening Powersave)		-	-	1.0	mA
	(Maximum Powersave)		-	-	1.0	mA
Dynamic Values						
Input Logic "1"		1	3.5	-	-	V
Input Logic "0"		1	-	-	1.5	V
Input Impedances						
Digital			0.1	1.0	-	MΩ
Mic.1 or 2			-	0.5	-	kΩ
Rx Audio			30.0	-	-	kΩ
Tx Audio			30.0	56.0	-	kΩ
CTCSS/Data			50.0	100	-	kΩ
External Audio Process			1.0	-	-	MΩ
Noise, RSSI			1.0	-	-	MΩ
Output Impedances						
Pre-Process Audio			-	-	3.0	kΩ
Audio Out (Rx)			-	-	3.0	kΩ
VCO Drive and Ref. Out			-	-	3.0	kΩ
Squelch Drive	(Logic "1")		-	5.0	-	kΩ
	(Logic '0")		-	500	-	Ω
Noise Output	(Diode conducting)		-	1.0	-	kΩ
	(Diode not conducting)		-	500	-	kΩ
Signal Path Switch Isolation (Disabled)						
Switches			40.0	-	-	dB
Test Path			-	60.0	-	dB
Signal Input Levels		10				
Mic.1 or 2			1.0	-	100	mV rms
Rx Audio			-	145	200	mV rms
Tx Audio			-	-	1414	mV rms
CTCSS/Data			-	-	4.0	V p-p
Post Process			-	-	1123	mVrms
Noise, RSSI		2	-	-	4.0	V p-p
Signal Output Levels		10				
Pre-Process Audio	(Compressor enabled)		-	600	-	mV rms
VCO - (Drive, Ref.)	(Limiter in circuit)		-	2.2	-	V p-p
Audio (Rx	(Limiter in circuit)		-	2.2	-	V p-p
Variable Element Step						
Input Gain Amp			0.7		1.3	dB
Pre-Process Gain			0.2		0.3	dB
VCO Ref. Attenuator			3.5		4.5	dB
VCO Drive Attenuator I			2.7		3.7	dB
VCO Drive Attenuator II			25.0		26.2	dB
VCO Amplifiers (Drive and Ref.)			0.2		0.3	dB

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Characteristics		See Note	Min.	Typ.	Max.	Unit
Output Distortion						
Output Signal-to-Noise Ratio		3, 12, 13	48.0	52.0	-	dBp
Total Harmonic Distortion Level		4, 11	-	-40.0	-30.0	dB
Compressor						
Dynamic Range			-	30.0	-	dB
Attack Time			-	7.0	-	ms
Decay Time			-	1000	-	ms
Deviation Limiter						
Input Thresholds		4	-	2.0	-	V p-p
Frequency Responses						
Pre-Process Path		6				
Passband Frequencies						
-3dB (Lower)			-	240	-	Hz
-3dB (Upper)			-	4.7	-	kHz
Passband Ripple	(300Hz - 400Hz)	5	-3.0	-	1.0	dB
	(400Hz - 3400Hz)	5	-1.5	-	1.0	dB
Stopband Attenuation	(f = 5kHz)		3.0	4.2	-	dB
High Frequency Roll-off	(f = >5kHz, <20kHz)		12.0	-	-	dB/oct.
Stopband Attenuation	(f = 250Hz)		-	2.3	-	dB
Low Frequency Roll-off	(f = <250Hz)		6.0	-	-	dB/oct.
Post-Process Path		7				
Wideband : Lowpass Frequency (-3dB)			-	3.4	-	kHz
Passband Ripple	(< 2700Hz)	8	-1.5	-	1.0	dB
	(2700Hz - 3000Hz)	8	-3.0	-	1.0	dB
Stopband Attenuation	(f = 5kHz)		12.2	17.0	-	dB
High Frequency Roll-off	(f = >3kHz, <20kHz)		18.0	-	-	dB/oct.
Narrowband: Lowpass Frequency (-3dB)			-	2.9	-	kHz
Passband Ripple	(< 2300Hz)		-1.5	-	1.0	dB
	(2300Hz - 2550Hz)		-3.0	-	1.0	dB
Stopband Attenuation	(f = 4.25kHz)		12.2	17.0	-	dB
High Frequency Roll-off	(f = >2.3kHz, <5.1kHz)		18.0	-	-	dB/oct.
Pre-emphasis: Passband Frequencies			300		3000	Hz
Gain at 1kHz			-	0	-	dB
Slope Characteristic			-	6.0	-	dB/oct.
De-emphasis: Passband Frequencies			300		3000	Hz
Gain at 1kHz			-	0	-	dB
Slope Characteristic			-	6.0	-	dB/oct.
Squelch Bandpass Filter						
Center Frequency Gain	(Wide and Narrow)		-	35.0	-	dB
Selectable Gain	(8 x 1.0dB steps)	9	-3.0	-	4.0	dB
Narrow Band:						
Center Frequency	(fc)		-	18.75	-	kHz
Bandwidth	(fc ±)		-	6.5	-	kHz
Wideband:						
Center Frequency	(fc)		-	25.5	-	kHz
Bandwidth	(fc ±)		-	8.5	-	kHz

Notes:

1. A percentage of the applied V_{DD} (70% or 30%)
2. These inputs are compared internally with the Digital-to-Analog converter.
3. With a minimum signal input level of 50mVrms at the Tx I/P or 65mVrms at the Rx I/P and an output level of 466mVrms.
4. Levels at the input of the Limiter element, centered about V_{BIAS} (Note 2).
5. This parameter remains within specification when pre-emphasis is employed.
6. With both Input HPF and LPF in circuit, but without pre-emphasis.
7. With Limiter LPF, but without de-emphasis characteristics.
8. This parameter remains within specification when de-emphasis is employed.
9. The gain variation around the center frequency (fc).
10. See Application Information pages (Suggested Evaluation Tests) for information on gain element settings.
11. Mode: Tx with Compressor "OFF;" or in Rx, signal below limiter thresholds; Output level 466mVrms. Measured in a 30kHz bandwidth.
12. In the Tx mode with the Input Gain Amp set to ≤ 4.0dB.
13. dBp refers to psophometrically weighted measurement.

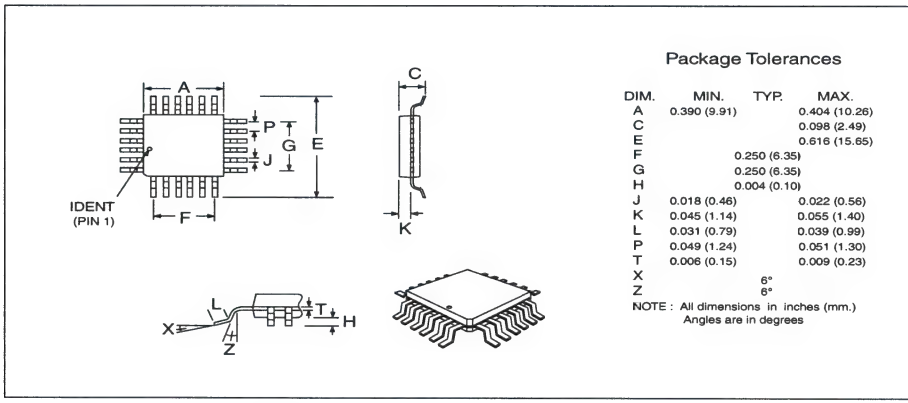
© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Package Outline

The MX506LG, the dual-in-line package is shown in Figure 10. The 'LH' version is shown in Figure 11 and the 'P' version in Figure 12.
To allow complete identification, the 'LG' and 'LH' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins on all three package styles number anti-clockwise when viewed from the top (indent side).

Handling Precautions

The MX506 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

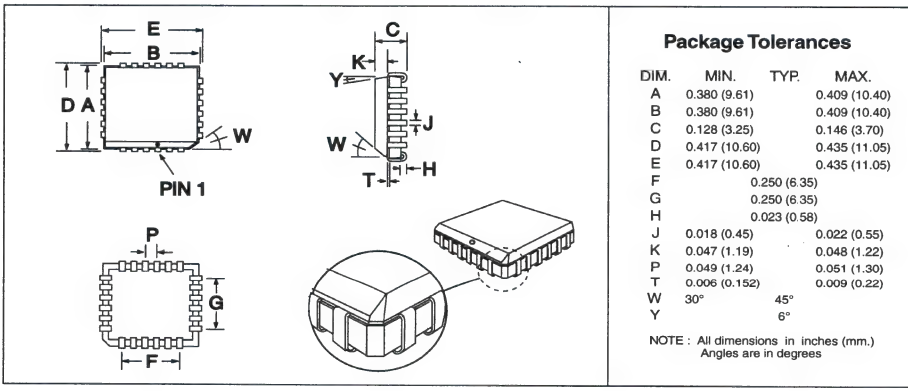


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.390 (9.91)		0.404 (10.26)
C			0.098 (2.49)
E			0.616 (15.65)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.004 (0.10)	
J	0.018 (0.46)		0.022 (0.56)
K	0.045 (1.14)		0.055 (1.40)
L	0.031 (0.79)		0.039 (0.99)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.15)		0.009 (0.23)
X		6°	
Z		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Fig.10 ***MX506LG*** *24-pin PLCC (GullWing) - lead Package*



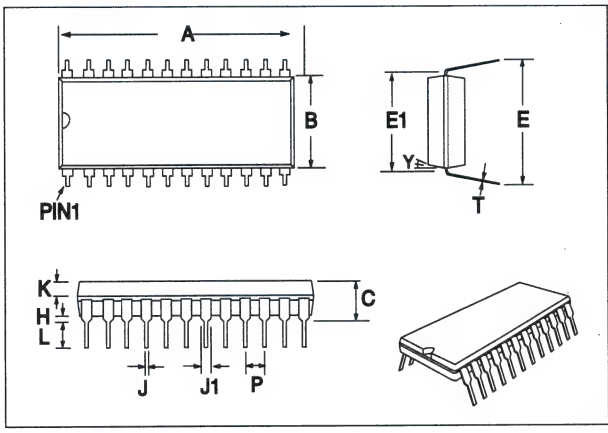
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Fig.11 ***MX506LH*** *24-pin PLCC-lead Package*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.
Doc. # 20480014.003



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm).
Angles are in degrees

Fig.12 ***MX506P*** *24-pin PDIP-lead Package*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480014.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATABULLETIN

MX806A AUDIO PROCESSOR

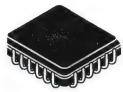
C-BUS COMPATIBLE

Description

The MX806A LMR audio processor is intended primarily to operate as the "Audio Terminal" of radio systems using the DBS 800 Digitally-integrated Baseband Subsystem.

The MX806A half-duplex device has signal paths and level setting elements that are configured and adjusted by digital information sent from the radio microcontroller using C-BUS protocol. (C-BUS is the serial interface for all DBS 800 ICs.)

MX806AJ
24-pin CDIP



MX806ALH
24-lead PLCC

MX806ADW
24-pin SOIC

The signal path of the MX806A can be divided into three sections:

- **Input Process**
  This stage has selectable TX/RX paths. Transmit voice signals pass through microphone pre-amplifier, voltage controlled gain (VOGAD) and highpass filter stages. Received audio is de-emphasized. This initial audio, after in-line gain adjustment, may be switched to external audio processes (such as scrambling) or to the internal Main Process stages.
- **Main Process**
  Conditioning for the input or external process signals is completed in this stage. It is comprised of pre-emphasis, high and lowpass switched-capacitor filters and a deviation limiter.
- **Mixing and Output Drives**
  Main audio for transmission is mixed with signaling and data from external sources (other DBS 800 ICs) to provide the composite signal for the digitally adjustable transmitter modulation drives. Received audio level is adjusted for output to loudspeaker circuitry.

If selected, signal level stability and output accuracy of the MX806A is maintained by a voltage-controlled gain system using selectable signal-level detectors. Signal levels can be dynamically controlled to provide "dynamic compensation" for factors such as temperature drift, VCO non-linearity, etc.

MX806A audio output stages can be completely disabled - or the whole IC can be placed into powersave mode, leaving only clock and C-BUS circuitry active.

The MX806A is a low-power 5V CMOS integrated circuit. It is available in 24-pin CDIP and SMT packages.

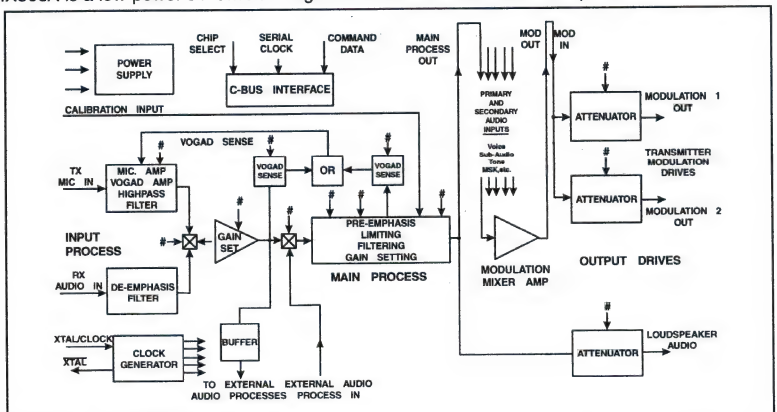


Figure 1 - MX806A Audio Processor

© 1996 MX•COM, INC.
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc.# 20480064.005

PIN FUNCTION CHART

Pin	Function
1	**Xtal:** The output of the 4.032 MHz on-chip clock oscillator. External components are required at this output when a Xtal is used. See Figure 2.
2	**Xtal/Clock:** The input to the on-chip 4.032 MHz clock oscillator inverter. A 4.032 MHz Xtal or externally derived clock should be connected here. See Figure 2. This clock provides timing for on-chip elements, filters, etc.
3	**Serial Clock:** The "C-BUS" serial data loading clock input. This clock, produced by the microcontroller, is used for transfer timing of Command Data to the Audio Processor. See Timing diagrams.
4	**Command Data:** The "C-BUS" serial data input from the microcontroller. Command Data is loaded to this device in 8-bit bytes, MSB (B7) first and LSB (B0) last, synchronized to the Serial Clock. The Command/Data instruction is acted upon at the end of loading the whole instruction. Command information is detailed in Tables 1 - 5. See Timing diagrams.
5	**Chip Select ($\overline{CS}$):** The "C-BUS" data loading control function. This input is provided by the microcontroller. Command Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See Timing Diagrams.
6	**VOGAD Out:** The error-voltage output of the selected VOGAD sensor. This output, with external attack and decay setting components, should be connected as in Figures 2 and 3, to the VOGAD In pin.
7	**RX Audio In:** The audio input to the MX806A from the radio receiver's demodulator circuits. This input, which requires a.c. coupling with capacitor C_{12}, is selected via a Control Command bit.
8	**VOGAD In:** The gain control signal from the selected VOGAD sensor (VOGAD Out) to the Input Process voltage-controlled amplifier. The required sensor is selected via a Mode Command. The choice of two sensors enables gain control from either the Input Process or an External Process. External attack and decay setting components should be applied as recommended in Figures 2 and 3.
9	**V_{BIAS}:** The output of the on-chip analog circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C_{10}. See Figure 2.
10	**Mic In (+):** The non-inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2.
11	**Mic In (-):** The inverting input to the microphone Op-Amp. This input requires external components for Op-Amp gain/attenuation setting as shown in Figure 2.
12	**V_{SS}:** Negative supply (GND).

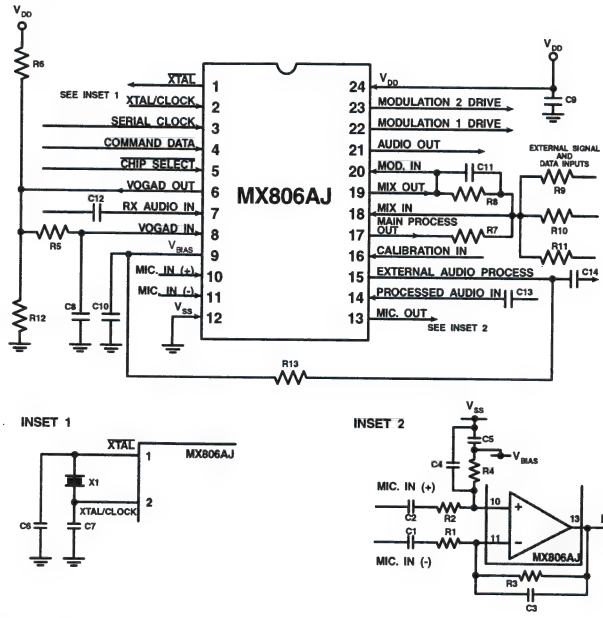
© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480064.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

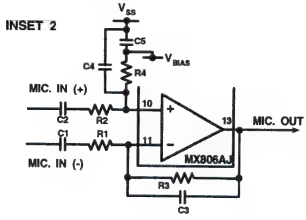
PIN FUNCTION CHART

Pin	Function
13	**Mic Out:** The output of the Microphone Op-Amp, used with the Mic In (-) input to provide the required gain/attenuation using external components as shown in Figure 2. The external components shown are to assist in the use of this amplifier with either inverting or non-inverting inputs. During Powersave (Volume Command) this output is placed at V_{SS}.
14	**Processed Audio In:** The input to the device from such external audio processes as Voice Store and Retrieve or Frequency Domain Scrambling. This input, which requires a.c. coupling with capacitor C_{13}, is selected by a Mode Command bit.
15	**External Audio Process:** The buffered output of the Input Processing Stage. Its purpose is to further external audio processing stages prior to re-introduction at the Processed Audio In pin.
16	**Calibration Input:** A unique audio input to be used for dynamic balancing of the modulator drives and for measuring Deviation Limiter levels. A CUE (beep) input from the MX803 Audio Tone Processor can be entered on this line. This audio input must be externally biased. It is selected via a Mode Command bit.
17	**Main Process Out:** The output of the Main Process stage. This output should be mixed with any additional system audio inputs (Audio, Sub-Audio Signaling, MSK) in the on-chip Modulation Summing Amplifier. External components shown in Figure 2 should be used as required.
18	**Sum In:** The input and output terminals of the on-chip Modulation Summing Amplifier. External components are required for input signals and gain/attenuation setting as shown in Figure 2. For single-signal, no-gain requirements, Main Process Out may be linked directly to Modulation In.
19	**Sum Out:**
20	**Modulation In:** The final, composite modulating signal to VCO (Mod 1) and Reference (Mod 2) Output Drives.
21	**Audio Output**: The processed audio signal output intended as a received audio (volume) output. Though normally used in the RX mode, operation in TX is permitted. The output level of this attenuator is controlled via a Volume Set command. During Powersave this output is placed at V_{SS}.
22	**Modulation 1 Drive:** The drive to the radio modulator Voltage Controlled Oscillator (VCO) from the composite audio summing stage.
23	**Modulation 2 Drive:** The drive to the radio modulator Reference Oscillator from the composite audio summing stage. NOTE: These VCO output attenuators are individually adjustable using the Modulator Level command. During Powersave these outputs are placed at V_{SS}.
24	V_{DD}: Positive supply. A single, stable +5 volt supply is required. Levels and voltages within this Audio Processor are dependent upon this supply.

© 1997 MX-COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480064.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Analog Application Information





Component	Value	Component	Value	Component	Value
R_1	10kΩ	R_{10}	100kΩ	C_6	33pF
R_2	10kΩ	R_{11}	100kΩ	C_7	5-65pF
R_3	20kΩ	R_{12}	2.2MΩ	C_8	1.0µF
R_4	20kΩ	R_{13}	470kΩ	C_9	1.0µF
R_5	10kΩ	C_1	.47µF	C_{10}	1.0µF
R_6	2.2MΩ	C_2	.47µF	C_{11}	22pF
R_7	100kΩ	C_3	270pF	C_{12}	0.1µF
R_8	100kΩ	C_4	270pF	C_{13}	0.01µF
R_9	100kΩ	C_5	0.1µF	C_{14}	0.01µF
				X_1	4.0MHz

Figure 2 - Recommended External Components

Tolerance: R=±10%. C=±20%.

Notes:

Input Op-Amp gain/attenuation components (voltage gain = 6.0dB) are shown in Inset 1 in a differential configuration to demonstrate the versatility of this input. Components for a single (+ or -) input may be used.

Resistor values R_7 to R_{11} (summation components) are dependent upon application and configuration requirements.

Xtal circuit capacitors C_6 (C_D) and C_7 (C_G) shown in Inset 2 are recommended in accordance with MX-COM's Crystal Oscillator Application Note, March 1990. Circuit drive and drain resistors are incorporated on-chip. Operation of any MX-COM IC without a Xtal or clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, you should install a current limiting device (resistor or fast-reaction fuse) on the power input (V_{DD}).

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480064.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Analog Application Information

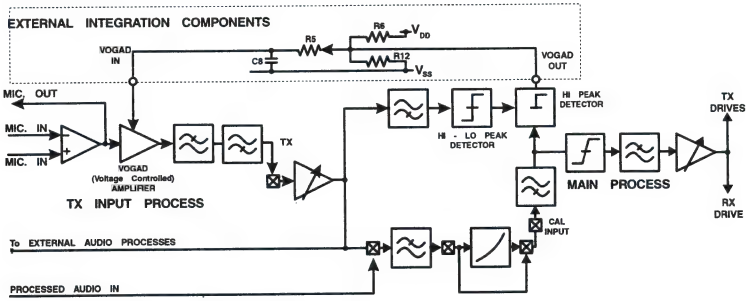


Figure 3 - VOGAD Sensors and Timing Components (from Fig. 5)

The overall Gain Control system of the MX806A consists of 2 selectable signal peak detectors whose output is fed via external integrating components to adjust the gain of the Voltage Controlled Amplifier positioned in the TX Input Process Path. The transmit input signal is presented to Peak Detector 1 or 2. The Peak Detectors are enabled individually by a Mode command. When the input signal exceeds the peak-to-peak threshold of the detector, a 5 volt level is produced at the VOGAD Out pin. This level remains for as long as the signal exceeds the threshold.

The integrated level to the VOGAD In pin causes the Voltage Controlled Amplifier gain to be reduced. As can be seen from Figures 3 and 5, Peak Detector 1 allows control of the audio level to the external audio process and Peak Dector 2 allows control of transmit deviation levels.

VOGAD attack and decay times are set using the external components shown in Figures 2 and 3. They are calculated as described below.

VOGAD Components Calculations - Figures 2 and 5

Provided $R_5 >> 1.0k\Omega$ and $R_6 = R_{12} >> R_5$

Then

$$\text{Attack Time } (T_A) = R_5 \times C_8$$

$$\text{Decay Time } (T_D) = \frac{R_6 \times C_8}{2}$$

Suggested Calibration Methods

To effectively null all internal IC tolerances, the following initial calibration routine is suggested:

TX Calibration: From Mic. In to Modulator Drives Out

Disable Peak Detectors (Mode Command).
Set Transmitter Drives to 0dB (Mod. Levels Set).
Pre-emphasis may be employed as required (Control Command).
Set Input Level Amp to 0dB (Control Command).

1) Mic. In = 250 mVrms at 1kHz. Set Process Gain Amp for output of 1440 mV p-p (100% deviation).
2) With Process Gain Amp set as 1 and with Mic. In = 25 mVrms at 1 kHz, set the Input Level Amp for an output level of 308 mVrms (60% deviation).

RX Calibration: From RX Audio In to Audio Out

Set Audio Output Drive to 0dB (Volume Set)
Leave Process Gain Amp set as 1 (see above).
3) With an RX Audio In level of between 154 mVrms and 308 mVrms (see Specifications) at 1 kHz, set the Input Level Amp for an output level of 308 mVrms.

©1997 MX-COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480064.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

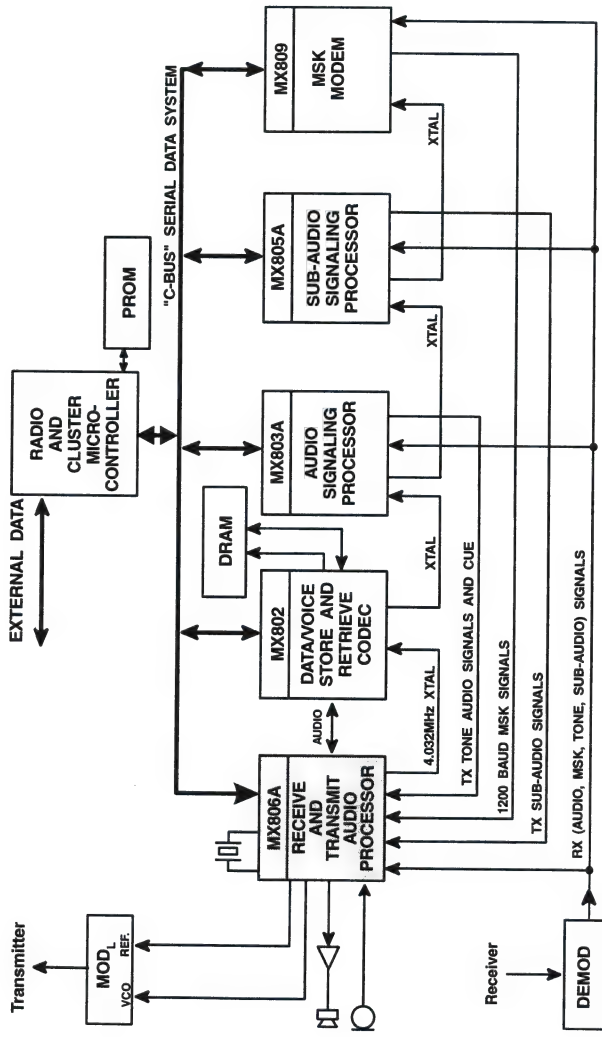


Figure 4 - MX806A Interfaced with Other DBS800 Elements

© 1997 MX-COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc.# 20480064.005

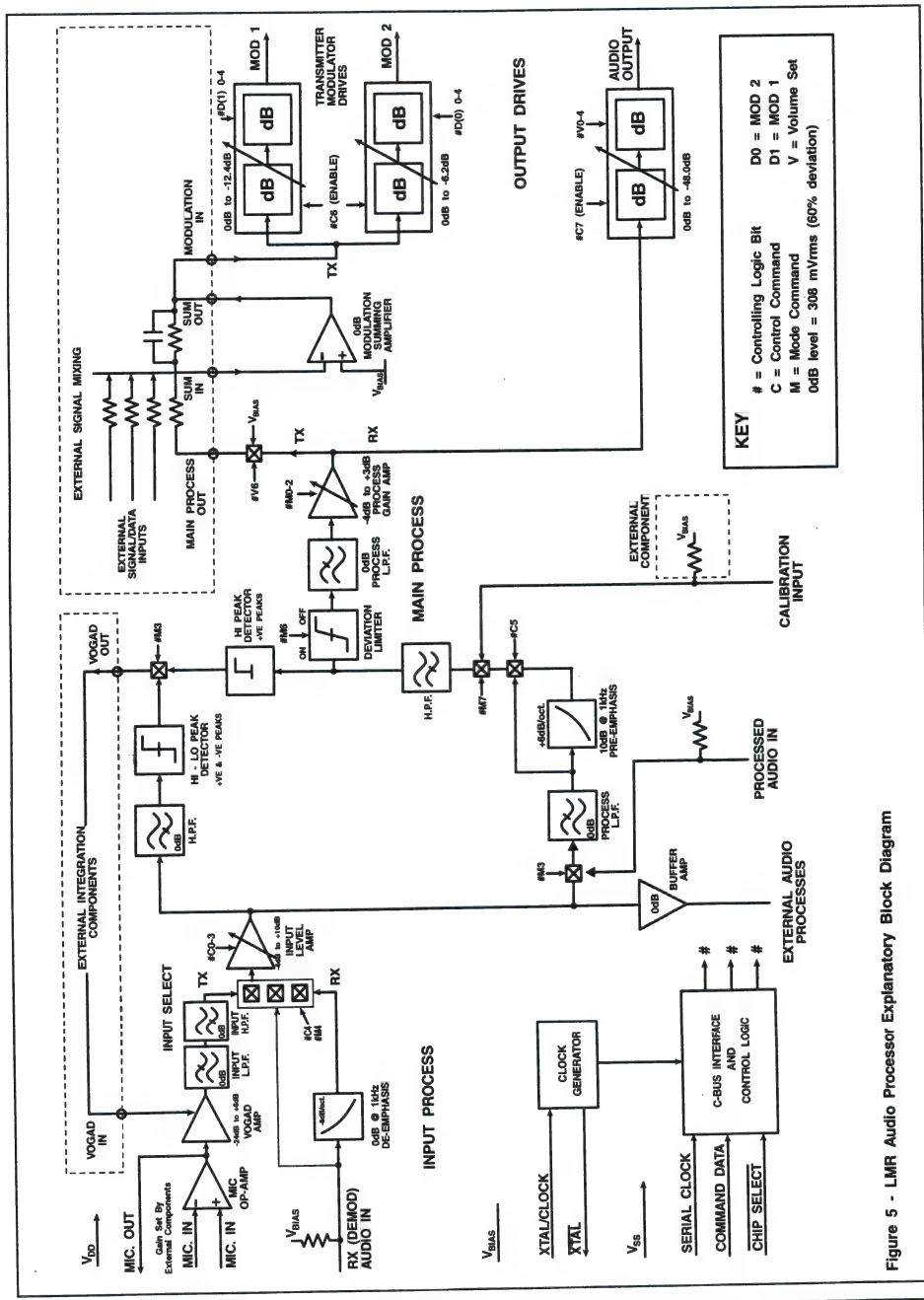


Figure 5 - LMR Audio Processor Explanatory Block Diagram

© 1997 MX-COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc.# 20480064.005

Controlling Protocol

Control of the functions and levels within the MX806A LMR Audio Processor is by a group of Address/Commands and appended data instructions from the system microcontroller. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Hex.	Address/Command Binary MSB LSB		Command Data	Table
General Reset	01	0 0 0 0 0 0 0 1			
Control Command	10	0 0 0 1 0 0 0 0	+	1 byte	2
Mode Command	11	0 0 0 1 0 0 0 1	+	1 byte	3
Mod. Levels Set	12	0 0 0 1 0 0 1 0	+	2 bytes	4
Volume Set	13	0 0 0 1 0 0 1 1	+	1 byte	5

Table 1 - C-BUS Address/Commands

In "C-BUS" protocol the MX806A is allocated Address/Command values 10_H to 13_H. C-BUS Command, Mode, Modulation and Volume assignments and data requirements are given in Table 1 and illustrated in Figure 5.

Commands and Data are only to be loaded in the group configurations detailed since the "C-BUS" interface recognizes the first byte after Chip Select (logic"0") as an Address/Command.

Function or Level control data, which is detailed in Tables 2, 3, 4, and 5, is acted upon at the end of the loaded instruction.

Upon power-up the value of the "bits" in this device will be random (either "0" or "1"). A General Reset Command (01_H) is required. This command is provided to "reset" all devices on the Command Data line and has the following effect on the MX806A:

Control Address Command	Loaded as 00_H
Mode Address Command	Loaded as 00_H
Volume Set	Loaded as 00_H

Control Command *(Preceded by A/C 10_H)*

Setting	Control Bits
(MSB) Bit 7	**Audio Output (RX)**
0	Disabled
1	Enabled
6	**Modulation Drives**
0	Disabled
1	Enabled
5	**Pre-Emphasis**
0	Bypass
1	Enabled
4	**Input Select**
0	RX In
1	Mic. In
3 2 1 0	**Input Level Set**
0 0 0 0	Input Amp Disabled
0 0 0 1	-4.0dB
0 0 1 0	-3.0dB
0 0 1 1	-2.0dB
0 1 0 0	-1.0dB
0 1 0 1	0dB
0 1 1 0	1.0dB
0 1 1 1	2.0dB
1 0 0 0	3.0dB
1 0 0 1	4.0dB
1 0 1 0	5.0dB
1 0 1 1	6.0dB
1 1 0 0	7.0dB
1 1 0 1	8.0dB
1 1 1 0	9.0dB
1 1 1 1	10.0dB

Table 2 - Control Commands

Mode Command *(Preceded by A/C 11_H)*

Setting	Mode Bits
(MSB) Bit 7	**Drive Source**
0	Signals
1	Calibration
6	**Deviation Limiter**
0	Disabled
1	Enabled
5	**VOGAD**
0	Disabled
1	Enabled
4	**De-Emphasis**
0	Enabled
1	Bypassed
3	**Signal Select**
0	Internal
1	External
2 1 0	**Process Gain Set**
0 0 0	-4.0dB
0 0 1	-3.0dB
0 1 0	-2.0dB
0 1 1	-1.0dB
1 0 0	0dB
1 0 1	1.0dB
1 1 0	2.0dB
1 1 1	3.0dB

Table 3 - Mode Commands

© 1997 MX-COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480064.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Modulator Levels *(Preceded by A/C 12_H)*

Setting	Modulator Drives
Byte 1 (MSB)	***First byte for transmission***
7 6 5	
0 0 0	Must be "0"
4 3 2 1 0	**VCO Drive Attenuation**
0 0 0 0 0	12.4dB
0 0 0 0 1	12.0dB
0 0 0 1 0	11.6dB
0 0 0 1 1	11.2dB
0 0 1 0 0	10.8dB
0 0 1 0 1	10.4dB
0 0 1 1 0	10.0dB
0 0 1 1 1	9.6dB
0 1 0 0 0	9.2dB
0 1 0 0 1	8.8dB
0 1 0 1 0	8.4dB
0 1 0 1 1	8.0dB
0 1 1 0 0	7.6dB
0 1 1 0 1	7.2dB
0 1 1 1 0	6.8dB
0 1 1 1 1	6.4dB
1 0 0 0 0	6.0dB
1 0 0 0 1	5.6dB
1 0 0 1 0	5.2dB
1 0 0 1 1	4.8dB
1 0 1 0 0	4.4dB
1 0 1 0 1	4.0dB
1 0 1 1 0	3.6dB
1 0 1 1 1	3.2dB
1 1 0 0 0	2.8dB
1 1 0 0 1	2.4dB
1 1 0 1 0	2.0dB
1 1 0 1 1	1.6dB
1 1 1 0 0	1.2dB
1 1 1 0 1	0.8dB
1 1 1 1 0	0.4dB
1 1 1 1 1	0dB
Byte 0 (MSB)	***Last byte for transmission***
7 6 5	
0 0 0	Must be "0"
4 3 2 1 0	**VCO (Ref.) Drive Attenuation**
0 0 0 0 0	6.2dB
0 0 0 0 1	6.0dB
0 0 0 1 0	5.8dB
0 0 0 1 1	5.6dB
0 0 1 0 0	5.4dB
0 0 1 0 1	5.2dB
0 0 1 1 0	5.0dB
0 0 1 1 1	4.8dB
0 1 0 0 0	4.6dB
0 1 0 0 1	4.4dB
0 1 0 1 0	4.2dB
0 1 0 1 1	4.0dB
0 1 1 0 0	3.8dB
0 1 1 0 1	3.6dB
0 1 1 1 0	3.4dB
0 1 1 1 1	3.2dB
1 0 0 0 0	3.0dB
1 0 0 0 1	2.8dB
1 0 0 1 0	2.6dB
1 0 0 1 1	2.4dB
1 0 1 0 0	2.2dB
1 0 1 0 1	2.0dB
1 0 1 1 0	1.8dB
1 0 1 1 1	1.6dB
1 1 0 0 0	1.4dB
1 1 0 0 1	1.2dB
1 1 0 1 0	1.0dB
1 1 0 1 1	0.8dB
1 1 1 0 0	0.6dB
1 1 1 0 1	0.4dB
1 1 1 1 0	0.2dB
1 1 1 1 1	0dB

Table 4 - Modulator Drive Levels

Volume Set *(Preceded by A/C 13_H)*

Setting	Volume Set
(MSB) 7 6	**Main Process Out**
0 0	Enabled
0 1	Biased
5	**Powersave**
0	Chip Enabled
1	Powersaved
4 3 2 1 0	**Volume Set Attenuation**
0 0 0 0 0	Off
0 0 0 0 1	48.0dB
0 0 0 1 0	46.4dB
0 0 0 1 1	44.8dB
0 0 1 0 0	43.2dB
0 0 1 0 1	41.6dB
0 0 1 1 0	40.0dB
0 0 1 1 1	38.4dB
0 1 0 0 0	36.8dB
0 1 0 0 1	35.2dB
0 1 0 1 0	33.6dB
0 1 0 1 1	32.0dB
0 1 1 0 0	30.4dB
0 1 1 0 1	28.8dB
0 1 1 1 0	27.2dB
0 1 1 1 1	25.6dB
1 0 0 0 0	24.0dB
1 0 0 0 1	22.4dB
1 0 0 1 0	20.8dB
1 0 0 1 1	19.2dB
1 0 1 0 0	17.6dB
1 0 1 0 1	16.0dB
1 0 1 1 0	14.4dB
1 0 1 1 1	12.8dB
1 1 0 0 0	11.2dB
1 1 0 0 1	9.6dB
1 1 0 1 0	8.0dB
1 1 0 1 1	6.4dB
1 1 1 0 0	4.8dB
1 1 1 0 1	3.2dB
1 1 1 1 0	1.6dB
1 1 1 1 1	0dB

Table 5 - Volume Set

Notes

Command Loading: Address/Commands and data bytes must be loaded in accordance with the information given in Figure 6.

The **Powersave** function is enabled by bit 5 of the Volume Set Command (Table 5).

During Powersave all internal elements except the Clock Generator and "C-BUS" interface are off. The Mic Op-Amp and Output Drive stage outputs are connected to V_{SS}.

Modulator Drives are controlled separately, but the whole two-byte Modulator Drive command must be loaded for each requirement adjustment.

$\overline{\text{Chip Select}}$ must be held at a logic "1" for the period "t_{CSOFF}" between transactions.

© 1997 MX-COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480064.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Timing Information

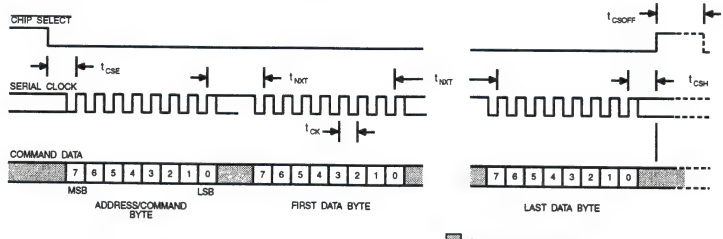


Figure 6 - C-BUS Timing Information

Parameter	Abbreviation	Min.	Typ.	Max.	Unit
"$\overline{CS}$ Enable" to "clock high"	t_{CSE}	2.0	-	-	µs
Last "clock high" to "CS high"	t_{CSH}	4.0	-	-	µs
"$\overline{CS}$ high" time between transactions	t_{CSOFF}	2.0	-	-	µs
Inter byte time	t_{NXT}	4.0	-	-	µs
Serial Clock Period	t_{CK}	2.0	-	-	µs

Notes
Command data is transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last.
Data is clocked into the peripheral on the rising clock edge.
Loaded data instructions are acted upon at the end of each individual, loaded byte.
To allow for different microcontroller serial interface formats, the MX806A is able to work with either polarity Serial Clock pulses.

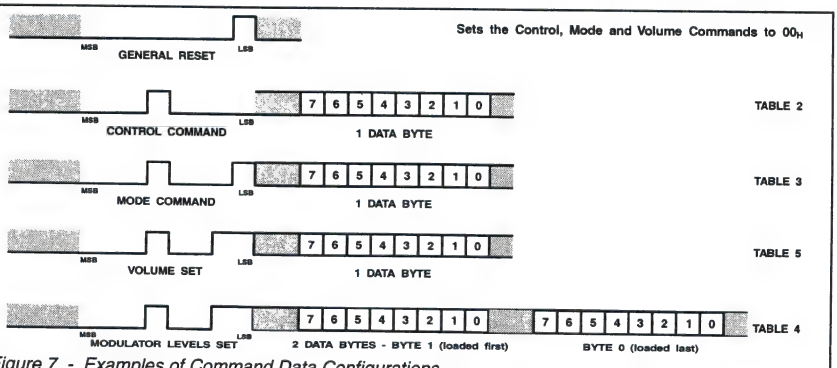


Figure 7 - Examples of Command Data Configurations

Application Information
To assist in rapid setting, this quick-reference list should be used with Figure 5.

Control	A/C = 10_H
7	Audio Out (RX) Enable
6	Modulator Drive Enable
5	Pre-Emphasis Select
4	Input Select (RX/TX)
3-0	Input Level Set (-4dB to 10dB)

Mode	A/C = 11_H
7	Drive Source
6	Deviation Limiter Enable
5	VOGAD Enable
4	De-Emphasis Enable
3	Signal Select
2-0	Process Gain Set (-4dB to 3dB)

Modulator Levels	A/C = 12_H
Byte1	
7-5	"0"
4-0	Mod 1 Attenuation (0 to 12.4dB)
Byte 2	
7-5	"0"
4-0	Mod 2 Attenuation (0 to 6.2dB)

Volume Set	A/C = 13_H
7-6	"0"
5	Powersave
4-0	Volume Set Attenuation (0 to 48dB)

© 1997 MX-COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480064.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD}+0.3V)
Sink/source current (supply pins)	±30mA
(other pins)	±20mA
Total device dissipation @ T_{AMB} 25°C	800mW Max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/Clock f_0 = 4.0MHz

Audio Level 0dB ref = 308mVrms @ 1kHz *(60% deviation, FM)*

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current (All elements enabled)		-	8.0	15.0	mA
(Maximum Powersave)		-	.7	1.5	mA
"C-BUS" Interface					
Input Logic "1"	3.5	-	-	V	
Input Logic "0"	-	-	1.5	V	
Input Current		-1.0	-	1.0	µA
Input Capacitance		-	-	7.5	pF
Overall Performance					
Microphone Input Level	1,2		25		mVrms
Discriminator Input Level	2,3	154	-	308	mVrms
Output Drive Level					
(60% deviation)	2,4	291	308	326	mVrms
(100% deviation)	2,4,5	-	1440	-	mV pk-pk
Passband	6	297	-	3000	Hz
Passband Ripple	7	-2	-	0.5	dB
Stopband Attenuation	6,8				
@150Hz		10	12	-	dB
@3400Hz		-	2	-	dB
@6000Hz		30	36	-	dB
@8000 to 20,000 Hz		-	60	-	dB
Signal Path Noise TX		-	-50	-	dBp
	9	-	-45	-	dB
RX		-	-60	-	dB
	9	-	-55	-	dB
Total Harmonic Distortion (RX or TX, 60% deviation)		-	1.0	-	%
Circuit Elements - Figure 5					
Mic. Amp or Mod. Summation Amp					
Open Loop Gain		-	50.0	-	dB
Bandwidth		20.0	-	-	kHz
Input Impedance		10.0	-	-	MΩ
Output Impedance (Open Loop)		-	6.0	-	kΩ
(Closed Loop)		-	600	-	Ω
De-emphasis					
Slope		-	-6.0	-	dB/oct.
Gain (at 1.0kHz)		-	0	-	dB
Input Impedance		-	1	-	MΩ
Voltage Controlled Gain Amp (VOGAD)					
Gain (Non-Compressing)	2	-	6.0	-	dB
(Full Compression)		-	-24	-	dB

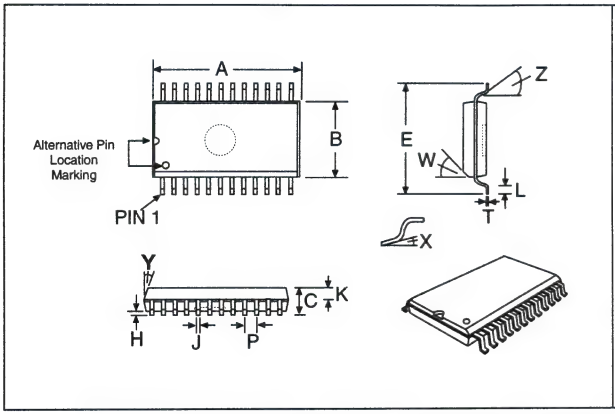
© 1997 MX-COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480064.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Input Impedance		10.0	-	-	MΩ
VOGAD Peak Detectors					
Output Impedance Logic "1" (Compress)		-	1	-	kΩ
Logic "0"		-	10	-	MΩ
Hi/Lo Peak Detector Threshold	10	-	1,300	-	mV p-p
Hi Peak Detector Threshold	10	-	650	-	mV+ve pk
Input (Low + Highpass) Filter					
Gain (at 1.0 kHz)		-1.0	0	1.0	dB
Input Level Amp					
Gain Range		-	0	-	dB
Overall Tolerance		-1.0	-	1.0	dB
Step Size		0.75	1.0	1.25	dB
External Audio Buffer					
Gain		-0.1	0	0.1	dB
Pre-emphasis (Main Process and VOGAD)					
Slope		-	6.0	-	dB/oct.
Gain (at 1.0kHz)		-	10.0	-	dB
Process Highpass Filter					
Gain (at 1.0 kHz)		-0.1	0	0.1	dB
Deviation Limiter					
Threshold		708	1300	1413	mVrms
Gain		-0.5	-	0.5	dB
Process Lowpass Filter					
Gain (at 1.0 kHz)		-0.1	0	0.1	dB
Process Gain Amp					
Gain Range		-4.0	-	3.0	dB
Overall Tolerance		-0.5	-	0.5	dB
Step Size		0.75	1.0	1.25	dB
Output Impedance		-	600	-	Ω
Transmitter Modulator Drives					
Input Impedance		-	15.0	-	kΩ
Mod. 1 Attenuator					
Attenuation Range		0	-	12.4	dB
Overall Tolerance		-1	-	1	dB
Step Size		0.2	0.4	0.6	dB
Output Impedance		-	600	-	Ω
Mod. 2 Attenuator					
Attenuation Range		0	-	6.2	dB
Overall Tolerance		-0.5	-	0.5	dB
Step Size		0.1	0.2	0.3	dB
Output Impedance		-	600	-	Ω
Audio Output Attenuator					
Attenuation Range		0	-	48.0	dB
Overall Tolerance		-1.0	-	1.0	dB
Step Size		1.1	1.6	2.1	dB
Output Impedance		-	600	-	Ω
Miscellaneous Impedances					
Processed Audio Input		-	500	-	kΩ
Calibration Input		-	500	-	kΩ
External Process Out		-	100	-	Ω
RX with De-emphasis Bypass		-	25.0	-	kΩ

Notes

1. Producing an output of 0dB with the Mic. Op-Amp set to 6dB (as shown in Figure 2) and the Modulator Drives set to 0dB.
2. With Output Drives set to 0dB and the system calibrated as described in the Application Notes.
3. Input level range for 0dB output, by adjustment of the Input Level Amp.
4. It is recommended that these output levels will produce 60% or 100% deviation in the transmitter.
5. With the microphone input level 20dB above the level required to produce 0dB at the Output Drives.
6. Between Microphone or RX inputs to Modulator or Audio Outputs.
7. Deviation from the ideal overall response including the pre- or de-emphasis slope.
8. Excluding the effect of pre- or de-emphasis slope.
9. In a 30kHz bandwidth.
10. Using pre-emphasis in the TX path.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480064.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

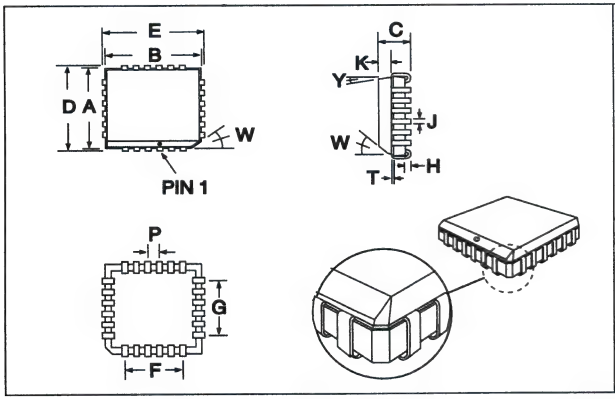


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin SOIC Mechanical Outline: order as part no. MX806ADW

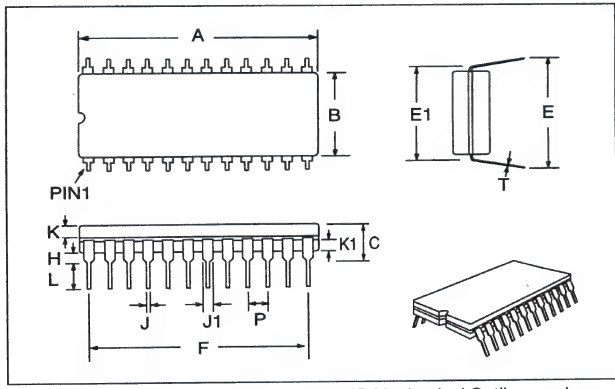


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 24-pin PLCC Mechanical Outline: order as part no. MX806ALH



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin CDIP Mechanical Outline: order as part no. MX806AJ

© 1997 MX-COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480064.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX829 Baseband Signal Processor

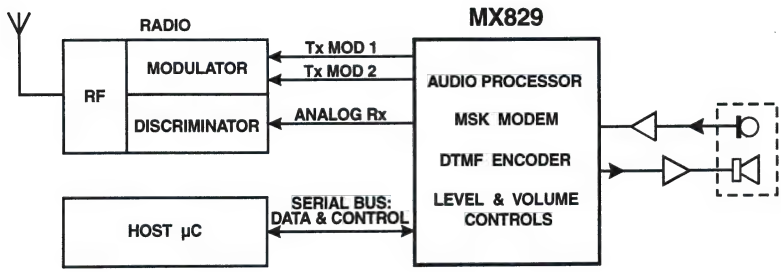
PRELIMINARY INFORMATION

Features

- **Rx Audio Processing**
- **Tx Audio Processing**
- **1200/2400 Baud Modem**
- **DTMF Encoder**
- **Low Voltage Operation**
- **"C-BUS" Compatible**
- **Host µC Interface**

Applications

- **ETS/MPT/PAA Standards Compatible**
- **LMR/PAMR/PMR Trunked Systems**
- **Multi-standard Modem Formats**



The MX829 is a low voltage CMOS integrated circuit, designed to provide baseband audio and system signal-processing functions required for LMR/PAMR/PMR trunked radio applications. The MX829 operates in half-duplex mode under the serial-bus control of a host µC.

The MX829 incorporates a dual-rate 1200/2400bps MSK modem, with a software-flexible choice of synchronization codewords, data run-length and CRC checking to suit a wide range of applications. These features allow very flexible handling of user defined data on traffic channels in addition to the network signaling sent on control channels. A 16 character DTMF encoder is available in the transmit mode. Software programmable output level-adjustment facilitates two-point modulation circuits.

The audio processing stages include transmit and receive filtering (based on standards specified for 12.5kHz and 25kHz LMR/PAMR/PMR channel operation), transmit deviation limiting, and a programmable Rx volume control. Power saving is automatic when audio functions are disabled.

The MX829 is designed for use in radios compatible with MPT1327, PAA1382 and ETS 300 086 trunking standards. The features and flexibility of the MX829 ensure that it is equally suitable for use with modified or proprietary standards.

The MX829 is available in the following packages: 24-pin SSOP (MX829DS), 24-pin SOIC (MX829DW), and 24-pin PDIP (MX829P).

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480160.003

CONTENTS

Section **Page**

1. Block Diagram **6-37**

2. Signal List **6-38**

3. External Components **6-39**

4. General Description **6-40**
4.1 Audio Filtering 6-40
4.2 DTMF Encoder 6-40
4.3 MSK Tx 6-40
4.4 MSK Rx 6-40

5. Software Description **6-41**
5.1 Address/Commands 6-41
5.2 Write Only Register Description 6-42
5.3 Read Only Register Description 6-48
5.4 MSK Checksum Generation and Checking 6-49

6. Application **6-51**

7. Performance Specification **6-52**
7.1 Electrical Performance 6-52
7.2 Packaging 6-59

MX•COM, Inc. reserves the right to change specifications at any time and without notice

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1. Block Diagram

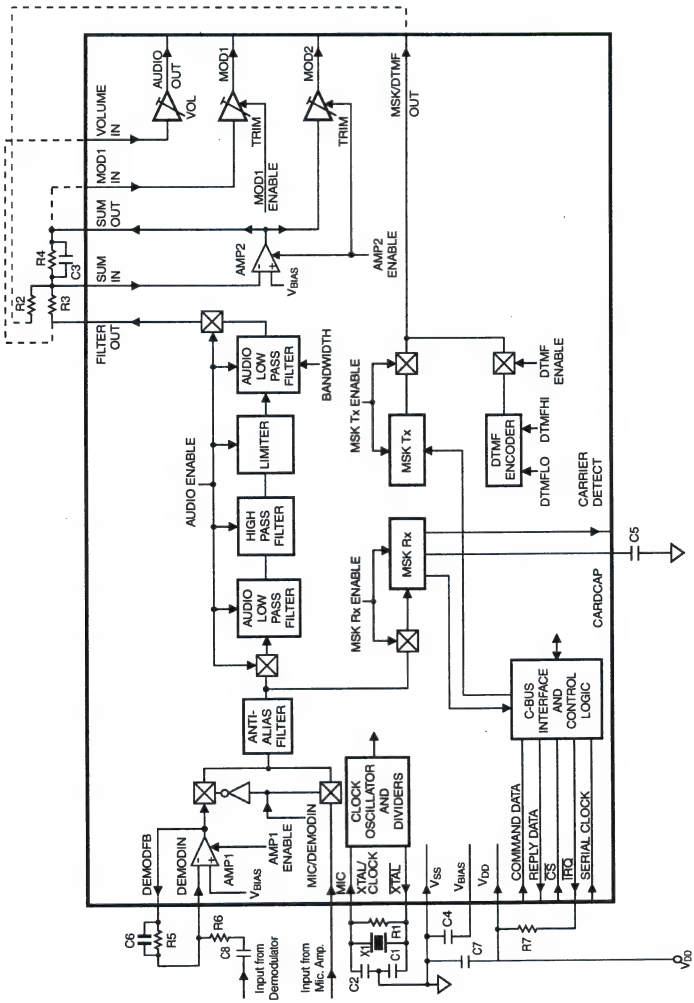


Figure 1: Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. Signal List

PIN NO	SIGNAL	TYPE	DESCRIPTION
1	$\overline{XTAL}$	output	Inverted output of the on-chip oscillator.
2	XTAL/CLOCK	input	Input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	input	"C-BUS" serial clock input. This clock, produced by the µController, is used for transfer timing of commands and data to and from the device. See section 7.1.4
4	COMMAND DATA	input	"C-BUS" serial data input from the µController. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the SERIAL CLOCK. See section 7.1.4.
5	REPLY DATA	output	"C-BUS" serial data output to the µController. The transmission of REPLY DATA bytes is synchronized to the SERIAL CLOCK under the control of the $\overline{CS}$ input. This 3-state output is held at high impedance when not sending data to the µController. See section 7.1.4.
6	$\overline{CS}$	input	"C-BUS" data loading control function: this input is provided by the µController. Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See section 7.1.4.
7	$\overline{IRQ}$	output	This output indicates an interrupt condition to the µController by going to a logic "0". This is a "wire-ORable" output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µController. This pin has a low impedance pulldown to logic "0" when active and a high-impedance when inactive. An external pull-up resistor is required. The conditions that cause interrupts are indicated in the STATUS register and are effective if not masked out by a corresponding bit in the CONTROL register. The reading of the Status Register resets the IRQ to a high impedance and sets the contents of the Status Register to 0.
8	CARRIER DETECT	output	The carrier detect output for the MSK Rx.
9	CD CAP	output	The carrier detect integrating capacitor.
10	V_{BIAS}	output	A bias line for the internal circuitry, held at $V_{DD}/2$. This pin must be bypassed to a capacitor mounted close to the device pins.
11	MIC	input	AC coupled Tx audio input (external amplification is required for use as a microphone input).
12	V_{SS}	Power	Negative supply (ground).
13	DEMOD IN	input	AC coupled inverting input to the Rx input amplifier (AMP1).
14	DEMOD FB	output	Output of the Rx input amplifier (AMP1)
15	FILTER OUT	output	Output of the audio filter/limiter section. In powersave mode this output is connected to V_{BIAS} via a 500kΩ resistor.
16	MSK/DTMF OUT	output	The 1200 or 2400 baud MSK Tx output and the DTMF encoder output. When enabled but not transmitting MSK or DTMF signals, or when in powersave mode, this output is connected to V_{BIAS} via a 500kΩ resistor. On power-up, this output can be any level: a General Reset command is required to ensure that this output attains V_{BIAS} initially.
17	SUM IN	input	Input to the audio summing amplifier (AMP2).
18	SUM OUT	output	Output of the audio summing amplifier (AMP2).
19	MOD1 IN	input	Input to MOD1 audio gain control.
20	VOL IN	input	Input to the audio volume control.
21	AUDIO OUT	output	Output of the audio volume control.
22	MOD1	output	Output of MOD1 audio gain control.
23	MOD2	output	Output of MOD2 audio gain control.
24	V_{DD}	Power	Positive supply. Levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components

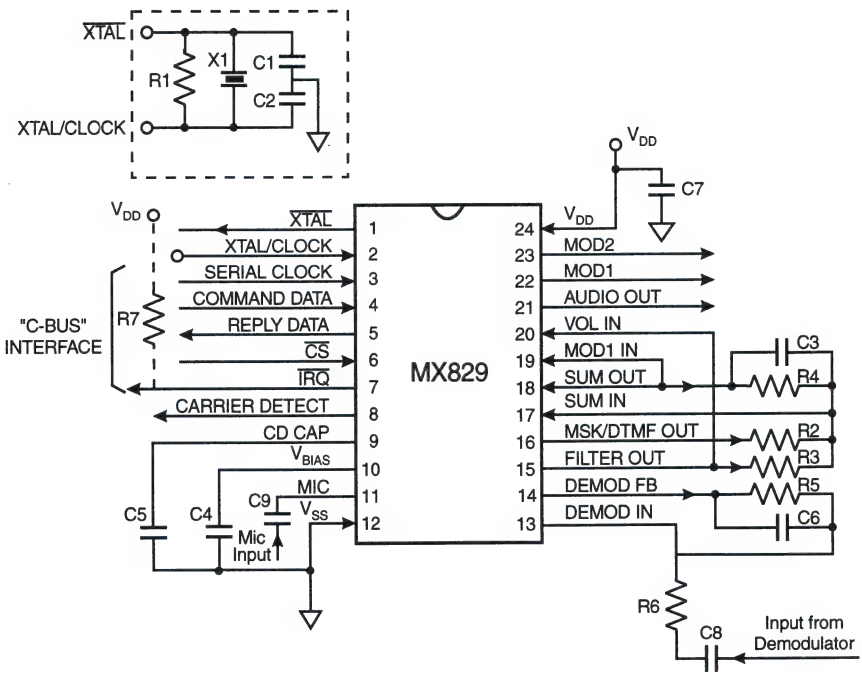


Figure 2: Recommended External Components

C1		22pF	±20%
C2		22pF	±20%
C3		68pF	±20%
C4		0.1µF	±20%
C5		0.1µF	±10%
C6		100pF	±20%
C7		0.1µF	±20%
C8	Note 2		±20%
C9		5.6nF	±20%

R1		1MΩ	±5%
R2	Note 1		±10%
R3	Note 1		±10%
R4		100kΩ	±10%
R5		100kΩ	±10%
R6	Note 2		±10%
R7		22kΩ	±10%
X1	Note 3	4.032MHz	±100ppm

External Component Notes:

1. R2, R3, R4 and C3 form the gain components for the Summing Amplifier (AMP2).
   R2 and R3 should be chosen as required from the system specification, using the following formula:

$$\text{Audio Gain} = -\frac{R4}{R3} \qquad \text{DTMF Gain} = -\frac{R4}{R2}$$

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. R5, R6, C6 and C8 form the gain components for the Rx Input Amplifier (AMP1).
   R6 should be chosen as required by the signal level, using the following formula:

$$\text{Gain} = -\frac{R5}{R6}$$

   C8 x R6 should be chosen so as not to compromise the low frequency performance of this product.
3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

The MX829 consists of four main sections: the Audio Filter, the DTMF encoder, the MSK transmitter, and the MSK receiver. These sections are controlled via a serial ("C-BUS") interface. The four sections are described below.

4.1 Audio Filtering

This consists of an input amplifier and a common audio filter section, which may be switched between Rx and Tx. The filter section comprises an anti-alias filter followed by low-pass and high-pass filtering with an amplitude limiter to set the maximum deviation. Three variable attenuation blocks may be used to set the volume (in Rx) or the modulation level (in Tx). Pre- and de-emphasis can be added externally using resistors and capacitors around AMP1, AMP2 and the microphone amplifiers, see Figure 7,Figure 8, and Figure 9. The anti-alias filter is designed to reduce aliasing effects above 50kHz which is approximately half the internal filter's sample rate.

The filtering is designed to meet the ETS 300 086 specification.

Various powersave modes are incorporated.

4.1.1 MOD1 and MOD2

The MOD1 input can be connected directly to SUM OUT, so that the MOD1 and MOD2 outputs can then be used for two point modulation. Alternatively, the MOD1 attenuator can be used for auxiliary gain adjustment, in which case the input signal must be ac coupled with a suitable capacitor.

4.2 DTMF Encoder

This generates the standard DTMF tones according to the CONTROL 2 Register settings. It also has a powersave mode.

4.3 MSK Tx

The Tx function of the MSK modem permanently operates in a free format mode, which means that the preamble and frame sync have to be programmed like normal data bytes. However, a 2-byte checksum may be generated automatically by simply marking the beginning and end of the data to be used. Any number of whole bytes may be used to generate the checksum.

After the last byte has been transmitted one additional "hang bit" is automatically added to the end. All Tx operations are programmed from the "C-BUS" via an 8-bit buffer.

The modulation output is one cycle of 1200Hz for a "1" and one and a half cycles of 1800Hz for a "0" at 1200 baud, or one half cycle of 1200Hz for a "1" and one cycle of 2400Hz for a "0" at 2400 baud.

4.4 MSK Rx

In Rx, the modem automatically achieves bit sync and then recognizes the previously selected SYNC or SYNT word of the MPT1327, ETS 300 230 or PAA1382 specifications. At the same time as one of the above, it also recognizes a user programmed 16-bit RX SYNC WORD.

On reception of the SYNC, SYNT or RX SYNC WORD, the device will automatically (or manually at any time) start checking the data and checksum. It provides a 1-bit correct/incorrect result every byte, so that any number of bytes can be checked.

The Rx part of the MSK modem operates at 1200 or 2400 baud and has a powersave mode. Both MSK Rx and Tx work in half duplex mode.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. Software Description

5.1 Address/Commands

Instructions and data are transferred, via "C-BUS", in accordance with the timing information given in Figure 12.

Instruction and data transactions to and from the MX829 consist of an Address/Command (A/C) byte followed by either:

1. a further instruction or data (1 or 2 bytes)
2. a status or Rx data reply (1 byte)

5.1.1 8-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
$10	CONTROL 1	AMP1	AMP2	AUDIO	MSKRX	MSKTX	UK/F	MIC	B/W
$11	CONTROL 2	CHKSUM	DTMFEN	DTMFHI	DTMFLO	DTMF3	DTMF2	DTMF1	DTMF0
$13	AUDIO ATTENUATION	0	0	0	<---------- GAIN ----------> BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$40	CONTROL 3/ IRQ ENABLE	0	1200/2400	TXIDLEM	RXDATAM	TXDATAM	RX SYNC WORD PRIME	SYNT PRIME	SYNC PRIME
$43	TXDATA	<---------- TXDATA ----------> BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

5.1.2 16-bit Write Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$12	MOD LEVELS (1)	0	0	MOD 1 ENABLE	<---------- MOD 1 ----------> BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	(2)	0	0	0	<---------- MOD 2 ----------> BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$44	RX SYNC WORD (1)	<---------- RX SYNC WORD ----------> BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
	(2)	<---------- RX SYNC WORD ----------> BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.2 Write Only Register Description

5.2.1 RESET Register (Hex address $01)

The reset command has no data attached to it. It sets the device registers into the specific states as listed below:

REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 D0)
CONTROL 1	0	0	0	0	0	0	0	0
CONTROL 2	0	0	0	0	0	0	0	0
CONTROL 3/IRQ ENABLE	0	0	0	0	0	0	0	0
AUDIO ATTENUATION	0	0	0	0	0	0	0	0
TXDATA	X	X	X	X	X	X	X	X
MOD LEVELS (1)	0	0	0	0	0	0	0	0
MOD LEVELS (2)	0	0	0	0	0	0	0	0
RX SYNC WORD (1)	X	X	X	X	X	X	X	X
RX SYNC WORD (2)	X	X	X	X	X	X	X	X
STATUS	0	0	0	0	0	0	0	0
RXDATA	X	X	X	X	X	X	X	X

X = undefined

5.2.2 CONTROL1 Register (Hex address $10)

This register is used to control the functions of the device as described below:

AMP1	When this bit is "1", AMP1 is enabled.
(Bit 7)	When this bit is "0", AMP1 is disabled (i.e. powersaved).
AMP2	When this bit is "1", both AMP2 and MOD2 are enabled.
(Bit 6)	When this bit is "0", both AMP2 and MOD2 are disabled (i.e. powersaved) and the MOD2 output is pulled to V_{BIAS} via a 1MΩ resistor.
AUDIO	When this bit is "1", the audio filter/limiter section is enabled.
(Bit 5)	When this bit is "0", the audio filter/limiter section is disabled (i.e. powersaved).
MSKRX	When this bit is "1", the MSK Rx is enabled.
(Bit 4)	When this bit is "0", the MSK Rx is disabled (i.e. powersaved).

Note: The MSK Rx and Tx cannot both be enabled at the same time. If both MSKRX and MSKTX are "1", then they will both be disabled (i.e. powersaved).

MSKTX	When this bit is "1", the MSK Tx is enabled.
(Bit 3)	When this bit is "0", the MSK Tx is disabled (i.e. powersaved).

Note: The MSK Tx and Rx cannot both be enabled at the same time. If both MSKTX and MSKRX are "1", then they will both be disabled (i.e. powersaved).

The DTMF Encoder and MSK Tx cannot both be enabled at the same time. If both DTMFEN and MSKTX are "1", then they will both be disabled.

UK/F	When this bit is "1", the SYNC/SYNT is set to the PAA standard of "1011010000110011" (SYNC)
(Bit 2)	When this bit is "0", the SYNC/SYNT is set to the MPT standard of "1100010011010111" (SYNC)
MIC	When this bit is "1", the MIC input is enabled and the AMP1 (DEMODIN) input is disabled.
(Bit 1)	When this bit is "0", the AMP1 (DEMODIN) input is enabled and the MIC input is disabled.
B/W	When this bit is "1", the bandwidth of the audio path is set wide for 20kHz/25kHz RF channel spacing.
(Bit 0)	When this bit is "0", the bandwidth of the audio path is set narrow for 12.5kHz RF channel spacing.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.2.3 CONTROL 2 Register (Hex address $11)

This register is used to control the functions of the device as described below:

CHKSUM (Bit 7)	In the Tx mode, when this bit is "1", the checksum generator is enabled. All complete bytes that are transmitted after this time are used in the checksum calculation. When this bit goes from "1" to "0", the checksum generator will complete its calculations on the current byte and the result will be sent as the next two bytes of transmitted data. In the Rx mode, the "0" to "1" transition of the CHKSUM bit is used at the start of the next byte received to manually reset the Rx checksum calculation, see Figure 4. (It can also be reset automatically by a SYNC, SYNT, or RX SYNC WORD detection - see section 5.2.5). The CHKSUM bit can be reset to "0" at any time. The result of the checksum is made available in the STATUS Register after the reception of every complete byte (See section 5.3.1). Note that the device is designed to work with any message length, and as a consequence it is not aware of the position of the checksum within the incoming data message. It thus performs a checksum assessment after every received byte. The controlling software should use its knowledge of the system message length in order to determine which RXSUMF reading is valid, i.e. after the second of the two checksum bytes has been received. The timing of data bytes relative to the checksum bit is shown in Figure 3 and Figure 4.

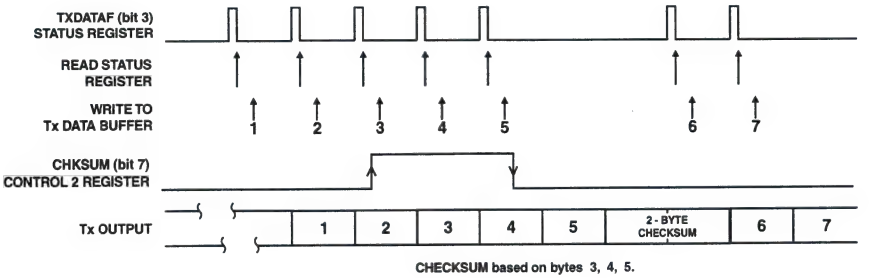


Figure 3: Checksum Generation in Tx Mode

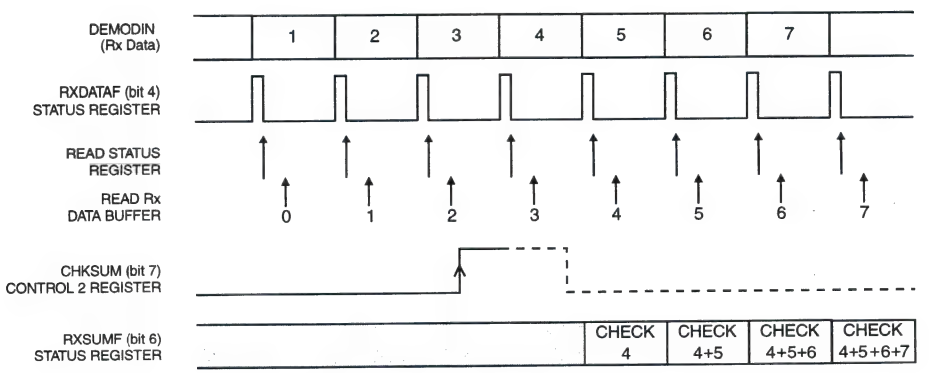


Figure 4: Checksum Calculation in Rx Mode

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

DTMFEN (Bit 6)	When this bit is "1", the DTMF output is enabled. When this bit is "0", the DTMF output is disabled. As the powersave of the DTMF is performed in the DTMFHI and DTMFLO registers, this bit allows a fast start up time for the tones.

Note: The DTMF Encoder and MSK Tx cannot both be enabled at the same time. If both DTMFEN and MSKTX are "1", then both will be disabled.

DTMFHI (Bit 5)	When this bit is "1", the DTMF high frequency tone generator is enabled. It will not appear on the output pin unless or until the DTMFEN is "1". When this bit is "0", the DTMF high frequency tone generator is disabled (i.e. powersaved).
DTMFLO (Bit 4)	When this bit is "1", the DTMF low frequency tone generator is enabled. It will not appear on the output pin unless or until the DTMFEN is "1". When this bit is "0", the DTMF low frequency tone generator is disabled (i.e. powersaved).
DTMF3, DTMF2, DTMF1, DTMF0 (Bit 3, Bit 2, Bit 1, Bit 0)	These four bits define the DTMF tones according to the table below:

Bit 3	Bit 2	Bit 1	Bit 0	DTMF Tones	DTMF 'Digit'
0	0	0	0	1209Hz + 697Hz	1
0	0	0	1	1209Hz + 770Hz	4
0	0	1	0	1209Hz + 852Hz	7
0	0	1	1	1209Hz + 941Hz	*
0	1	0	0	1337Hz + 697Hz	2
0	1	0	1	1337Hz + 770Hz	5
0	1	1	0	1337Hz + 852Hz	8
0	1	1	1	1337Hz + 941Hz	0
1	0	0	0	1478Hz + 697Hz	3
1	0	0	1	1478Hz + 770Hz	6
1	0	1	0	1478Hz + 852Hz	9
1	0	1	1	1478Hz + 941Hz	#
1	1	0	0	1634Hz + 697Hz	A
1	1	0	1	1634Hz + 770Hz	B
1	1	1	0	1634Hz + 852Hz	C
1	1	1	1	1634Hz + 941Hz	D

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.2.4 AUDIO ATTENUATION Register (Hex Address $13)

The five least significant bits in this register are used to set the attenuation of the audio volume control according to the table below:

4	3	2	1	0		Audio Attenuation
0	0	0	0	0		Off
0	0	0	0	1		48.0dB
0	0	0	1	0		46.4dB
0	0	0	1	1		44.8dB
0	0	1	0	0		43.2dB
0	0	1	0	1		41.6dB
0	0	1	1	0		40.0dB
0	0	1	1	1		38.4dB
0	1	0	0	0		36.8dB
0	1	0	0	1		35.2dB
0	1	0	1	0		33.6dB
0	1	0	1	1		32.0dB
0	1	1	0	0		30.4dB
0	1	1	0	1		28.8dB
0	1	1	1	0		27.2dB
0	1	1	1	1		25.6dB
1	0	0	0	0		24.0dB
1	0	0	0	1		22.4dB
1	0	0	1	0		20.8dB
1	0	0	1	1		19.2dB
1	0	1	0	0		17.6dB
1	0	1	0	1		16.0dB
1	0	1	1	0		14.4dB
1	0	1	1	1		12.8dB
1	1	0	0	0		11.2dB
1	1	0	0	1		9.6dB
1	1	0	1	0		8.0dB
1	1	0	1	1		6.4dB
1	1	1	0	0		4.8dB
1	1	1	0	1		3.2dB
1	1	1	1	0		1.6dB
1	1	1	1	1		0dB

Note: Bits 5, 6 and 7 should always be set to "0".

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.2.5 CONTROL 3 / IRQ ENABLE Register (Hex address $40)

This register is a mixture of control bits and interrupt mask bits, as detailed below:

Bit 7	Not used, set to zero.
1200/2400 (Bit 6)	When this bit is "1", the MSK Rx and Tx are set to operate at 1200 baud. When this bit it "0", the MSK Rx and Tx are set to operate at 2400 baud.
TXIDLEM (Bit 5)	When this bit is "1", the TXIDLE interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is "0", the TXIDLE interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
RXDATAM (Bit 4)	When this bit is "1", the RXDATA interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is "0", the RXDATA interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
TXDATAM (Bit 3)	When this bit is "1", the TXDATA interrupt will be gated out to the $\overline{IRQ}$ pin. When this bit is "0", the TXDATA interrupt will be inhibited. This bit has no effect on the contents of the STATUS register.
RX SYNC WORD PRIME (Bit 2)	When this bit is set to "1", it enables the RX SYNC WORD detection. It is cleared/disabled when a SYNC, SYNT, or RX SYNC WORD is detected. It may also be cleared/disabled by writing "0" directly to this bit.
SYNT PRIME (Bit 1)	When this bit is set to "1", it enables the SYNT detection. It is cleared/disabled when a SYNC, SYNT, or RX SYNC WORD is detected. It may also be cleared/disabled by writing "0" directly to this bit.
SYNC PRIME (Bit 0)	When this bit is set to "1", it enables the SYNC detection. It is cleared/disabled when a SYNC, SYNT, or RX SYNC WORD is detected. It may also be cleared/disabled by writing "0" directly to this bit.

5.2.6 TXDATA Register (Hex Address $43)

This is the Tx data output register. It is double buffered, thus giving the user up to 8 bit periods to load in the next 8 bits. MSK data is transmitted immediately it is loaded if the transmitter is idle. Data is transmitted in 8-bit bytes, bit 7 (MSB) will be transmitted first.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.2.7 MOD LEVELS Register **(Hex address $12)**

The six least significant bits of the first byte in this register are used to set the attenuation of the Modulator 1 amplifier and the five least significant bits of the second byte in this register are used to set the attenuation of the Modulator 2 amplifier, according to the tables below:

5	4	3	2	1	0	Mod. 1 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	12.0dB
1	0	0	0	1	0	11.6dB
1	0	0	0	1	1	11.2dB
1	0	0	1	0	0	10.8dB
1	0	0	1	0	1	10.4dB
1	0	0	1	1	0	10.0dB
1	0	0	1	1	1	9.6dB
1	0	1	0	0	0	9.2dB
1	0	1	0	0	1	8.8dB
1	0	1	0	1	0	8.4dB
1	0	1	0	1	1	8.0dB
1	0	1	1	0	0	7.6dB
1	0	1	1	0	1	7.2dB
1	0	1	1	1	0	6.8dB
1	0	1	1	1	1	6.4dB
1	1	0	0	0	0	6.0dB
1	1	0	0	0	1	5.6dB
1	1	0	0	1	0	5.2dB
1	1	0	0	1	1	4.8dB
1	1	0	1	0	0	4.4dB
1	1	0	1	0	1	4.0dB
1	1	0	1	1	0	3.6dB
1	1	0	1	1	1	3.2dB
1	1	1	0	0	0	2.8dB
1	1	1	0	0	1	2.4dB
1	1	1	0	1	0	2.0dB
1	1	1	0	1	1	1.6dB
1	1	1	1	0	0	1.2dB
1	1	1	1	0	1	0.8dB
1	1	1	1	1	0	0.4dB
1	1	1	1	1	1	0dB

4	3	2	1	0	Mod. 2 Attenuation
0	0	0	0	0	>40dB
0	0	0	0	1	6.0dB
0	0	0	1	0	5.8dB
0	0	0	1	1	5.6dB
0	0	1	0	0	5.4dB
0	0	1	0	1	5.2dB
0	0	1	1	0	5.0dB
0	0	1	1	1	4.8dB
0	1	0	0	0	4.6dB
0	1	0	0	1	4.4dB
0	1	0	1	0	4.2dB
0	1	0	1	1	4.0dB
0	1	1	0	0	3.8dB
0	1	1	0	1	3.6dB
0	1	1	1	0	3.4dB
0	1	1	1	1	3.2dB
1	0	0	0	0	3.0dB
1	0	0	0	1	2.8dB
1	0	0	1	0	2.6dB
1	0	0	1	1	2.4dB
1	0	1	0	0	2.2dB
1	0	1	0	1	2.0dB
1	0	1	1	0	1.8dB
1	0	1	1	1	1.6dB
1	1	0	0	0	1.4dB
1	1	0	0	1	1.2dB
1	1	0	1	0	1.0dB
1	1	0	1	1	0.8dB
1	1	1	0	0	0.6dB
1	1	1	0	1	0.4dB
1	1	1	1	0	0.2dB
1	1	1	1	1	0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte)	When this bit is "1" the MOD1 attenuator is enabled. When this bit is "0" the MOD1 attenuator is disabled (i.e. powersaved). Bits 6 and 7 in the first byte and bits 5, 6 and 7 in the second byte should always be set to "0". MOD LEVELS (1) register is loaded first.

Note: The MOD2 attenuator is enabled by the AMP2 ENABLE signal (bit 6 of CONTROL1 register).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.2.8 RX SYNC WORD Register (Hex $44)

This is a two byte register that defines the 16-bit programmable synchronization word. This word is compared with the incoming Rx data and, if a match is found, it is indicated in the STATUS register and an interrupt is generated. Bit 15, the MSB of the first byte, is loaded first.

8-bit Read Only Registers

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$41	STATUS	0	RXSUMF	TXIDLEF	RXDATAF	TXDATAF	RX SYNC WORDF	SYNTF	SYNCF
$42	RXDATA	<---------- RXDATA ---------->							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

5.3 Read Only Register Description

5.3.1 STATUS Register (Hex address $41)

This register is used to indicate the status of the device as described below:

Note: After reading the contents of the Status Register, all bits in the Status Register are reset to a zero state and the IRQ, externally generated by the MX829, is cleared.

Bit 7	Not used, always set to zero.
RXSUMF (Bit 6)	When this bit is "1", the Rx checksum is correct. When this bit is "0", the Rx checksum is incorrect. This bit is updated and latched in, after reception of every eight bits (see section 5.2.3).
TXIDLEF (Bit 5)	When all the Tx data and any checksum and one "hang-bit" have been transmitted, this bit will be set to "1" to indicate that the transmitter is idle. This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt may be generated depending on the state of the TXIDLEM bit in the CONTROL 3 / IRQ ENABLE register.
RXDATAF (Bit 4)	When a full byte of data is received and is available in the RXDATA register, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1" an interrupt may be generated depending on the state of the RXDATAM bit in the CONTROL 3 / IRQ ENABLE register.
TXDATAF (Bit 3)	When the Tx data buffer is empty this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt may be generated depending on the state of the TXDATAM bit in the CONTROL 3 / IRQ ENABLE register.
RX SYNC WORDF (Bit 2)	This bit is only defined when RX SYNC WORD PRIME is enabled. When the data sequence specified in the RX SYNC WORD register has been successfully matched to the Rx incoming data, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt will be generated, the checksum generator and byte counter will be reset and SYNC PRIME, SYNT PRIME and RX SYNC WORD PRIME will be reset.
SYNTF (Bit 1)	This bit is only defined when SYNT PRIME is enabled. When the data sequence specified by SYNT has been successfully matched to the Rx incoming data, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt will be generated, the checksum generator and byte counter will be reset and SYNC PRIME, SYNT PRIME and RX SYNC WORD PRIME will be reset.
SYNCF (Bit 0)	This bit is only defined when SYNC PRIME is enabled. When the data sequence specified by SYNC has been successfully matched to the Rx incoming data, this bit will be set to "1". This bit is reset to "0" immediately after reading the STATUS register. When this bit is set to "1", an interrupt will be generated, the checksum generator and byte counter will be reset and SYNC PRIME, SYNT PRIME and RX SYNC WORD PRIME will be reset.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.3.2 RXDATA Register **(Hex address $42)**

This register contains the last byte of data received. It is updated every 8 bits at the same time as the RXSUMF bit in the STATUS register is updated.

The RXDATA register is double buffered, thus giving the user up to 8 bit periods to read the data before it is overwritten by the next byte.

5.4 MSK Checksum Generation and Checking

5.4.1 Generation

The checksum generator takes the m x 8 bits from the m bytes of information, sequentially loaded into the TXDATA register and divides them modulo-2, by the generating polynomial:

$$X15 + X14 + X13 + X11 + X4 + X2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial m x 8 bits and the 15-bit remainder (with the last bit inverted).

This 16-bit word is used as the "CHECKSUM". See Figure 5.

(m = the number of bytes in the information to be sent)

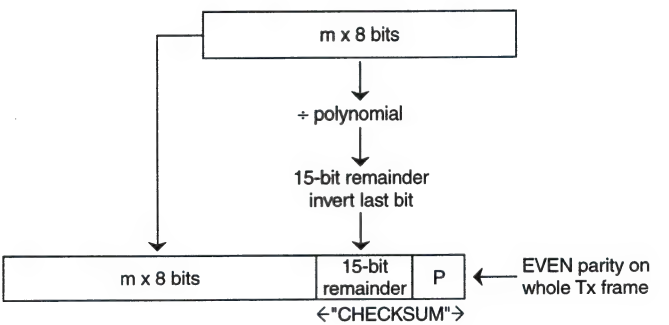


Figure 5: Checksum Generation

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.4.2 Checking

The checksum checker performs two tasks:

It takes the first n-1 bits of a received (n = 8m + 16 bits) message, inverts bit n-1, and divides them modulo-2, by the generating polynomial:

X15 + X14 + X13 + X11 + X4 + X2 + 1

The 15 bits remaining in the polynomial divider are checked for all zero.

Secondly, it generates an EVEN parity bit from the first n-1 bits of a received message and compares this bit with the received parity bit (bit n). See Figure 6.

If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the RXSUMF bit (STATUS register bit 6) is set. This is updated and latched every 8 bits, starting at the bit immediately after the initialization of the bit counter. This initialization takes place on detection of frame synchronization, i.e. the matching of received data to the SYNC, SYNT or RX SYNC WORD.

Note that the checksum is calculated on the received data before it is double buffered (see Figure 4).

n = the number of bits in the received message

m = the number of bytes of transmitted data, excluding checksum

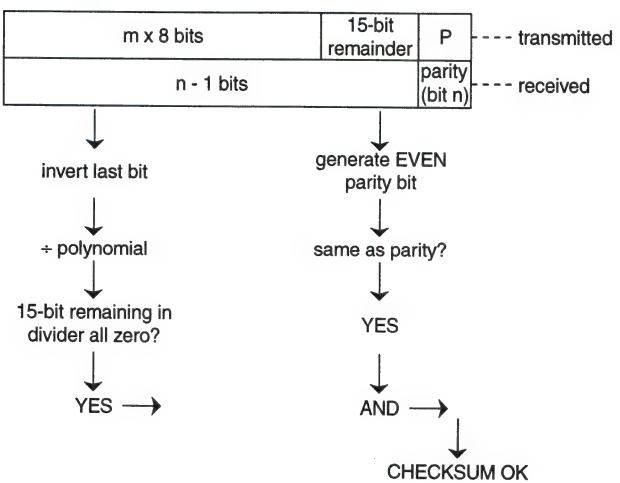


Figure 6: Checksum Checking

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6. Application

The following block diagrams show the possible arrangements for the pre- and de-emphasis required by PAA1382 and MPT1327 specifications.

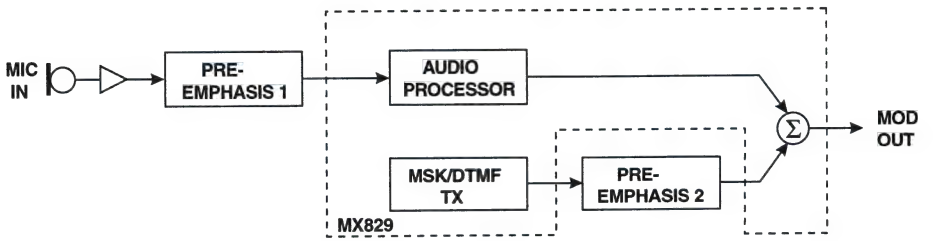


Figure 7: Transmitter Pre-emphasis

Note: Both pre-emphasis positions shown, as required by the PAA1382 specification. Remove pre-emphasis 2 for the MPT1327 specification requirement.

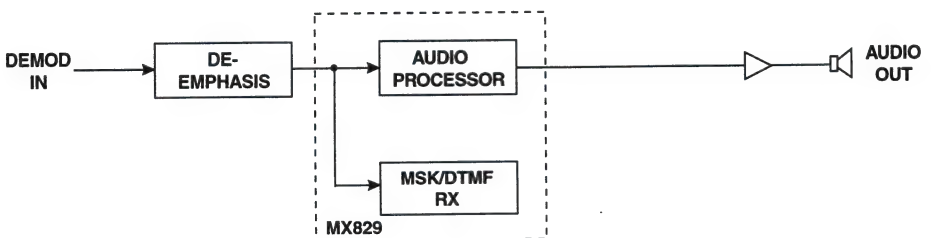


Figure 8: PAA1382 Receiver De-emphasis

Note: De-emphasis shown in all paths, as required by the PAA1382 specification.

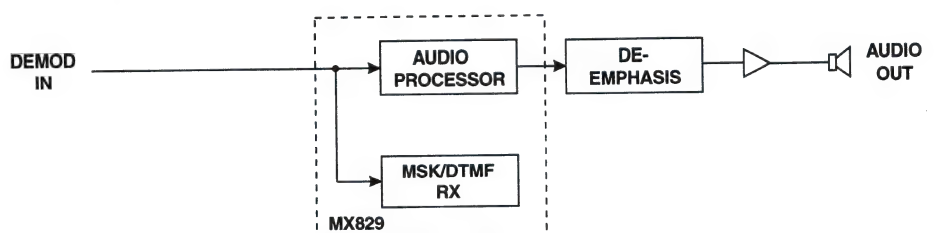


Figure 9: MPT1327 Receiver De-emphasis

Note: De-emphasis shown in audio path only, as required by the MPT1327 specification.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

7. Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
DW / P Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-40	85	°C
Operating Temperature	-40	85	°C
DS Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		550	mW
Derating above 25°C		9	mW/°C above 25°C
Storage Temperature	-40	85	°C
Operating Temperature	-40	85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency		4.0315968	4.0324032	MHz

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, Bit Rate = 1.2k bits/sec, Noise Bandwidth = Bit Rate,

Audio Level 0dB ref. = 308mVrms at 1kHz

V_{DD} = 5.0V, T_{AMB} = 25°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (Tx or Rx) (V_{DD} = 3.3V)	2		2.7	4.0	mA
I_{DD} (Tx or Rx) (V_{DD} = 5.0V)	2		5.0	8.0	mA
I_{DD} (Powersaved) (V_{DD} = 3.3V)	2		0.3	1.0	mA
I_{DD} (Powersaved)(V_{DD} = 5.0V)	2		0.6	1.5	mA
"C-BUS" Interface					
Input Logic "1"		70%			V_{DD}
Input Logic "0"				30%	V_{DD}
Input Leakage Current (logic "1" or "0")		-1.0		1.0	µA
Input Capacitance				7.5	pF
Output Logic "1" (I_{OH} = 120µA)		90%			V_{DD}
Output Logic "0" (I_{OL} = 360µA)				10%	V_{DD}
"Off" State Leakage Current (V_{OUT} = V_{DD})	9			10	µA
AC Parameters					
Input Sensitivity (for 0dB output)					
Tx Audio Input (MIC)	8		308		mV_{RMS}
Rx Audio Input (DEMODFB)	8		308		mV_{RMS}
Output Drive Level					
For 60% Deviation	1, 6, 8	291	308	326	mV_{RMS}
For 100% Deviation	1, 6, 7, 8		1440		mV_{P-P}
Audio Filters					
Gain at 1kHz	5		0		dB
Passband Ripple	5	-2.0		0.5	dB
SINAD	5, 14		59		dBp
Signal Path Noise	5		-55		dB
Narrow Audio Bandwidth Setting					
Passband Frequencies	5	300		2550	Hz
Stopband Attenuation					
(f = 100Hz)	5		3.0		dB
(f = 3400Hz)	5		5.5		dB
(f = 6000Hz)	5	10.5	24		dB
(f = 12500Hz)	5	25	49		dB
Wide Audio Bandwidth Setting					
Passband Frequencies	5	300		3000	Hz
Stopband Attenuation:					
(f = 100Hz)	5		3.0		dB
(f = 3400Hz)	5		3.0		dB
(f = 6000Hz)	5	10.5	19		dB
(f = 25000Hz)	5	39.5	68		dB

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

	Notes	Min.	Typ.	Max.	Units
Amp 1 and Amp 2					
Open Loop Gain (INPUT = 1mV at 100Hz)			70		dB
Unity Gain Bandwidth			5.0		MHz
Input Impedance (at 100Hz)		10			MΩ
Output Impedance					
Open Loop			6.0		kΩ
Closed Loop			600		Ω
Distortion (DTMF)			2	5	%
MSK/DTMF TX OUT					
Tx output impedance (not powersaved)	3		1.0	2.5	kΩ
Tx output impedance (powersaved)	3	300	500		kΩ
Signal Level					
MSK	1	-1	0	1	dB
DTMF High Tone	1		2.0		dB
DTMF Low Tone	1		0		dB
Distortion (DTMF)			2	5	%
MSK TX OUT					
Isochronous Distortion:					
(1200Hz - 1800Hz)			25	40	µs
(1800Hz - 1200Hz)			25	40	µs
(1200Hz - 2400Hz)			20	30	µs
(2400Hz - 1200Hz)			20	30	µs
Third Harmonic Distortion			2	3	%
Deviation Limiter					
Threshold	1		1300		mV_{P-P}
Gain		-0.5		0.5	dB
Transmitter Modulator Drives					
Input Impedance (MOD1 IN, VOLUME IN at 100Hz)			15.0		kΩ
Mod.1 Attenuator					
Nominal Adjustment Range		0		12.0	dB
Attenuation Accuracy		-1.0		1.0	dB
Step Size		0.2	0.4	0.6	dB
Output Impedance	3		600		Ω
Mod.2 Attenuator					
Nominal Adjustment Range		0		6.0	dB
Attenuation Accuracy		-0.6		0.6	dB
Step Size		0.1	0.2	0.3	dB
Output Impedance	3		600		Ω
Audio Output Attenuator					
Nominal Adjustment Range		0		48.0	dB
Attenuation Accuracy		-1.5		1.5	dB
Step Size			1.6		dB
Output Impedance	3		600		Ω

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

	Notes	Min.	Typ.	Max.	Units
MSK Receiver					
Signal Input Dynamic Range (SNR = 50dB)	10, 11	100	230	1000	mV_{RMS}
Bit Error Rate					
SNR = 12dB at 1200 Baud	11		2.5		10^{-4}
SNR = 12dB at 2400 Baud	11		1.5		10^{-3}
SNR = 20dB at 1200/2400 Baud	11		1.0		10^{-8}
Receiver Synchronization (SNR = 12dB)	12				
Probability of Bit 16 being correct			0.995		%
Carrier Detect					
Sensitivity	12, 13			150	mV_{RMS}
Probability of Carrier Detection					
After Bit 16 (SNR = 12dB)			0.995		%
With 230mV_{RMS} Noise (No Signal)			0.05		%
Miscellaneous Impedance					
FILTER OUT			600		Ω
Tx Audio Input (MIC) (at 100Hz)		10			MΩ
Xtal/Clock Input					
'High' pulse width	4	40			ns
'Low' pulse width	4	40			ns
Input Impedance (at 100Hz)		10			MΩ
Gain (INPUT = 1mV_{RMS} at 100Hz)		20			dB

Operating Characteristics Notes:

1. Signal levels are proportional to V_{DD}.
2. Not including any current drawn from the modem pins by external circuitry.
   Powersaved = all functions disabled.
   Tx or Rx = device configured into any half-duplex operating mode.
3. Small signal impedance. A minimum load resistance of 6kΩ is suggested.
4. Timing for an external input to the XTAL/CLOCK pin.
5. Between MIC or AMP1 inputs to Modulator and Audio outputs, see Figure 10 and Figure 11.
6. It is recommended that these output levels are used to produce 60% or 100% deviation in the transmitter.
7. With the Tx Audio input level 20dB above the level required to produce 0dB at the Output Drives.
8. With output gains set to 0dB.
9. $\overline{IRQ}$ pin.
10. See Figure 14 (variation of BER with Input Signal Level).
11. SNR = Signal to Noise Ratio in the Bit Rate Bandwidth.
12. For a "10101010101 ...01" pattern.
13. Measured with a 150mV_{RMS} input signal (no noise).
14. dBp represents a psophometrically weighted measurement.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

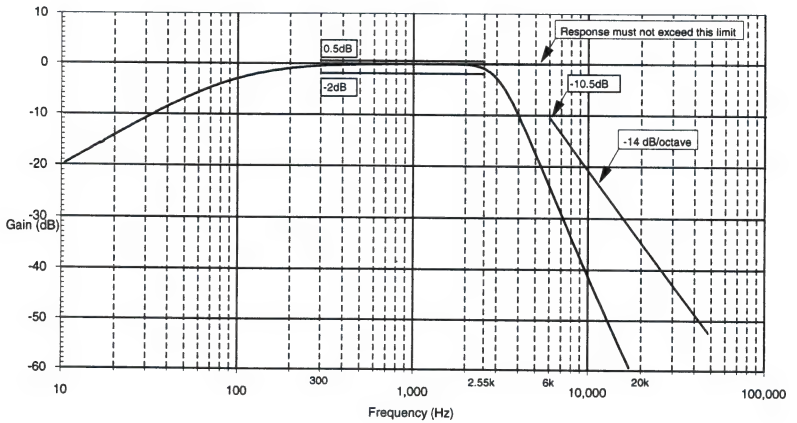


Figure 10: Overall Audio Frequency Response for 12.5kHz Channel Separation

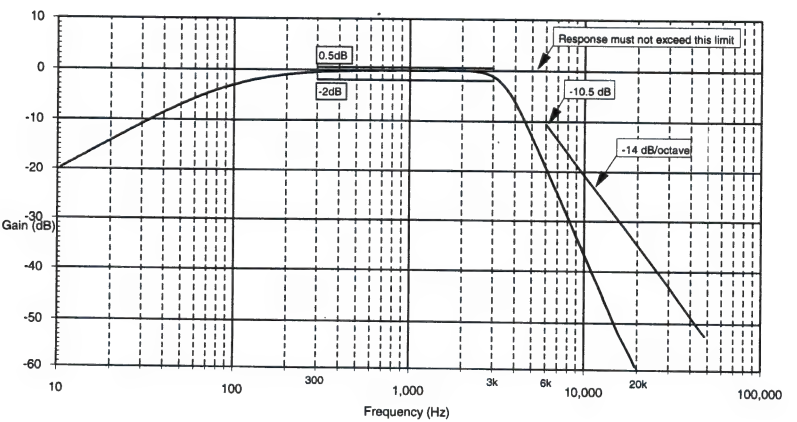


Figure 11: Overall Audio Frequency Response for 20kHz/25kHz Channel Separation

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.
Doc. # 20480160.003

7.1.4 Timing

For the following conditions unless otherwise specified:

Xtal Frequency = 4.032MHz, V_{DD} = 5.0V, T_{AMB} = 25°C.

	Parameter	Notes	Min.	Typ.	Max.	Units
t_{CSE}	"CS-Enable to Clock-High"		2.0			µs
t_{CSH}	Last "Clock-High to CS-High"		4.0			µs
t_{HIZ}	"CS-High to Reply Output 3-state"				2.0	µs
t_{CSOFF}	"CS-High" Time between transactions		2.0			µs
t_{NXT}	"Inter-Byte" Time		4.0			µs
t_{CK}	"Clock-Cycle" time		2.0			µs

Timing Notes:

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (bit 7) first, LSB (bit 0) last. REPLY DATA is read from the peripheral MSB (bit 7) first, LSB (bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µController serial interface formats "C-BUS" compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

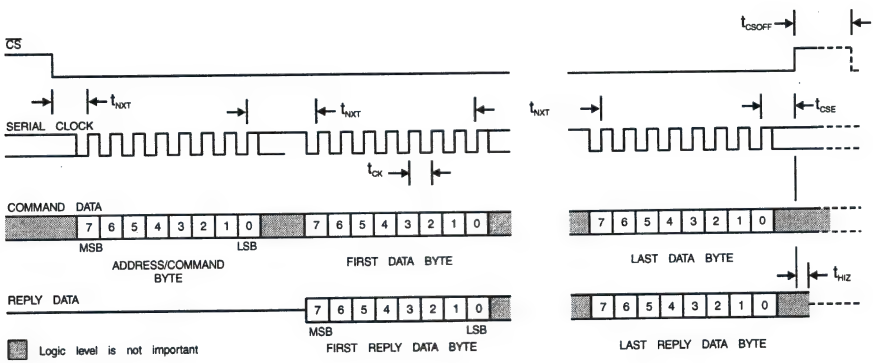


Figure 12: "C-BUS" Timing

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

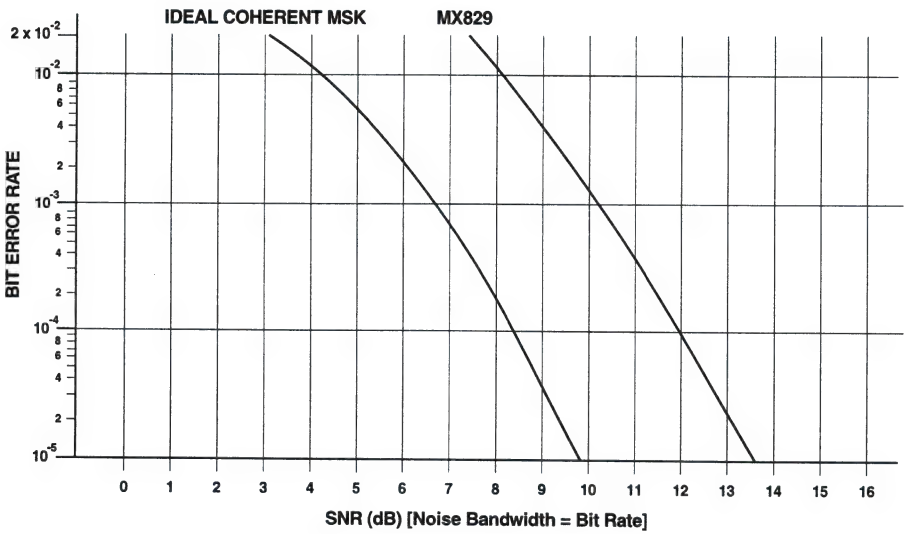
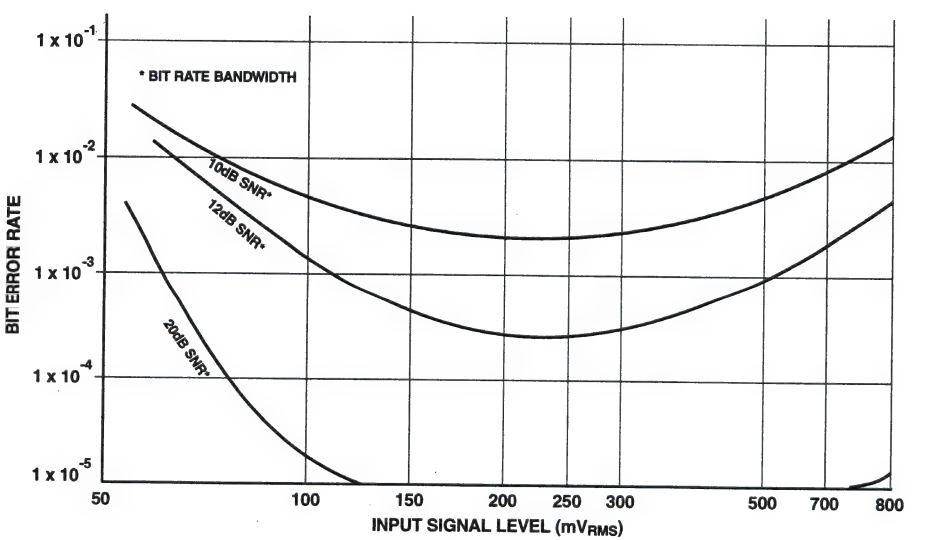


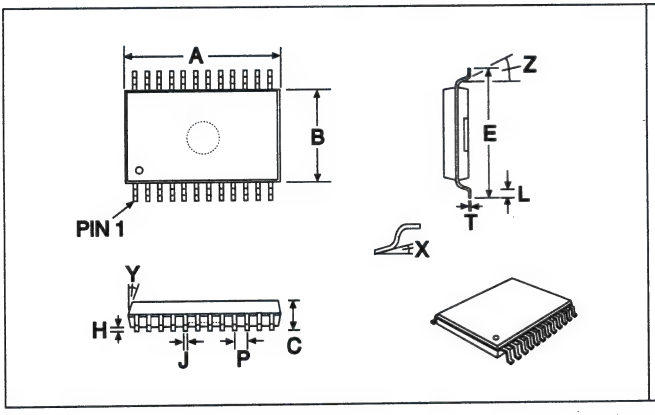
Figure 13: Bit Error Rate Graph



© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Figure 14: Typical Variation of Bit Error Rate with Input Signal Level

7.2 Packaging

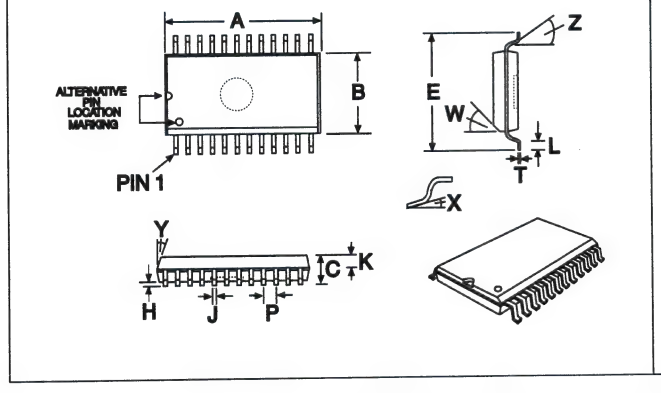


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.213 (5.39)
C	0.066 (1.67)		0.079 (2.00)
E	0.301 (7.65)		0.312 (7.90)
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 24-pin SSOP Mechanical Outline: *Order as part no. MX829DS*



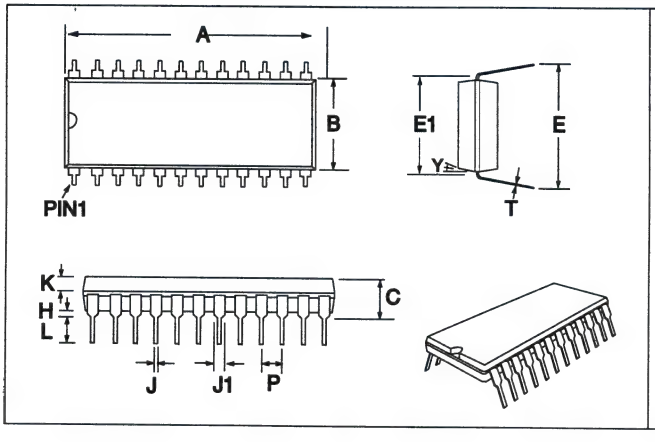
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16: 24-pin SOIC Mechanical Outline: Order as part no. MX829DW

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 17: 24-pin PDIP Mechanical Outline: *Order as part no. MX829P*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480160.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX980

Digital Radio Baseband Processor for π/4 DQPSK TETRA

ADVANCE INFORMATION

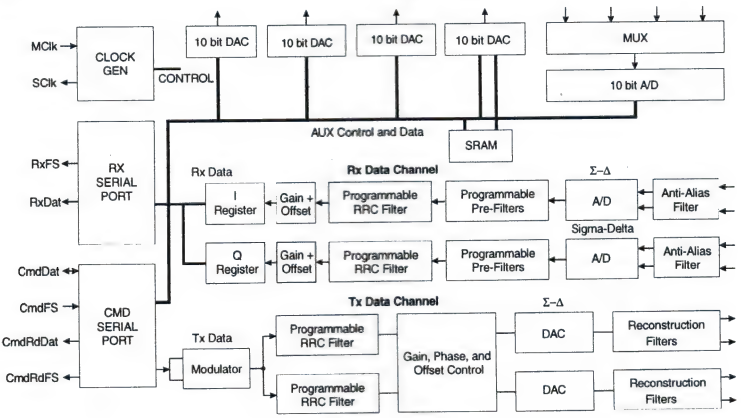
Shipping: Contact MX-COM, Inc.

FEATURES

- **Tx and Rx 36kbps Baseband DSP Engine**
  - **π/4 DQPSK Modulation**
  - **Root Raised Cosine (RRC) filters**
  - **2 x 16 bit Sigma Delta D/A for quadrature Tx signals**
  - **2 x 16 bit Sigma Delta A/D for quadrature Rx signals**
- **Default TETRA filter coefficients (can be user reprogrammed)**

APPLICATIONS

- **Integrated Analog I/O Processor for Radio Support**
  - **4 x 10 bit D/A converters**
  - **4 input x 10 bit A/D converter**
  - **Integrated r.f. transmit power control with programmable ramp up/down attack profile**
- **Full control, configuration, and digital signal flow via Serial Interface**
- **Low Voltage Operation (3.3 to 5.0V) with powersave**



The MX980 plays a key role in a digital radio system with processing intensive I/O and support functions to mate digital signal circuits to the analog radio section. By providing focused capability in this particular baseband processing and interface area, the MX980 helps partition digital radio designs to achieve maximum system performance at minimum cost.

Designed for use in both TETRA (Trans European Trunked RAdio) mobile and base stations, the MX980 can also be user reprogrammed for other applications.

The MX980 Tx path provides all necessary signal processing to convert an input digital data stream into properly root raised cosine filtered analog quadrature (I and Q) signals ready for up-conversion and transmission. Output gain, offset, and filter coefficients are all digitally programmable with default coefficients for TETRA's RRC response.

The MX980 Rx path features differential quadrature (I and Q) analog inputs with A/D converters and digital filters to produce a digitally sampled and filtered data stream ready for further processing and baseband data extraction. Like the Tx path, the Rx path features digitally programmable gain, offset, and filter coefficients with default filter coefficients for TETRA.

The integrated analog I/O processor provides a sophisticated toolbox of features which can be applied for AFC, AGC, RSSI, part of a Cartesian Loop control system, or the monitoring and control of other subsystems. One of its functions, suited for precise transmit power control, is a user programmable attack/decay ramp profile on an analog output signal.

© 1997 MX•COM, INC
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480167.001
All trademarks and service marks are held by their respective companies.

CONTENTS

Section **Page**

1. Block Diagram **63**

2. Signal List **64**

3. General Description **65**

3.1 Transmit Description 65
3.2 Receive Description 67
3.3 Auxiliary Circuits 69
3.4 IRQ Function 70
3.5 Serial Interface 71
3.6 Register Description 73

4. Application TBD **95**

5. Performance Specification **96**

5.1 Electrical Performance 96
5.2 Timing 98
5.3 Packaging TBD 101

MX•COM, Inc. reserves the right to change specifications and without notice.

© 1997 MX•COM, INC
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480167.001

1. Block Diagram

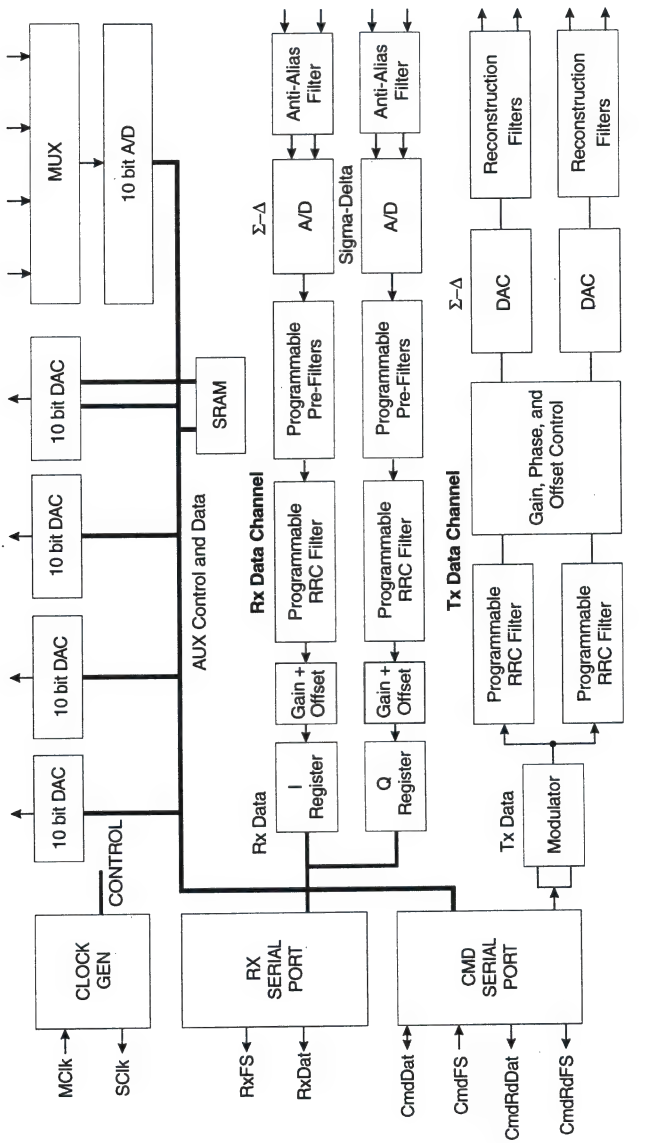


Figure 1 Block Diagram

© 1997 MX•COM, INC
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480167.001

2. Signal List

Pin No.		Signal		Description
XX	XX	Name	Type	
		MCLK	input	Master clock input (typically 9.216MHz)
		SCLK	output	Serial interface clock
		SCmdDat	bi-directional	Command serial interface Data
		SCmdFS	input	Command serial interface Frame
		SCmdRdDat	output	Command serial interface Read Data
		SCmdRdFS	output	Command serial interface Read Frame
		SRxDat	output	Receive serial interface Data
		SRxFS	output	Receive serial interface Strobe
		$\overline{IRQ}$	output	Interrupt request
		$\overline{RESET}$	input	Chip Reset
		CS	input	Chip Select (normally tied high)
		SCANSEL	input	Scan Select (normally tied low)
		ITXP	output	Transmit "I" channel, P output
		ITXN	output	Transmit "I" channel, N output
		QTXP	output	Transmit "Q" channel, P output
		QTXN	output	Transmit "Q" channel, N output
		IRXP	input	Receive "I" channel, P input
		IRXN	input	Receive "I" channel, N input
		QRXP	input	Receive "Q" channel, P input
		QRXN	input	Receive "Q" channel, N input
		AUXADC1	input	Auxiliary ADC channel 1
		AUXADC2	input	Auxiliary ADC channel 2
		AUXADC3	input	Auxiliary ADC channel 3
		AUXADC4	input	Auxiliary ADC channel 4
		AUXDAC1	output	Auxiliary DAC channel 1
		AUXDAC2	output	Auxiliary DAC channel 2
		AUXDAC3	output	Auxiliary DAC channel 3
		AUXDAC4	output	Auxiliary DAC channel 4
		BIAS	bi-directional	Analog bias level. This pin should be decoupled to V_{SS1}
		V_{CC1}	power	Primary analog positive supply rail. Levels and voltages are dependent upon this supply. This pin should be decoupled to V_{SS1}
		V_{CC2}	power	Auxiliary analog positive supply rail. This pin should be decoupled to V_{SS2}
		V_{CC3}	power	Secondary analog positive supply rail. This pin should be decoupled to V_{SS3}
		V_{DD1}	power	Primary digital positive supply rail. This pin should be decoupled to V_{SS4}
		V_{SS1}	Ground	Primary analog negative supply rail.
		V_{SS2}	Ground	Secondary analog negative supply rail.
		V_{SS3}	Ground	Auxiliary analog negative supply rail.
		V_{SS4}	Ground	Primary digital negative supply rail.

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. General Description

3.1 Transmit Description

3.1.1 Modulator

This takes the 2 bit symbols, performs a Gray code conversion and uses a recursive adder to generate a 3 bit code representing the 8 possible phase states. A look up table provides the digitally encoded I and Q values for each phase state. The modulator function can be by-passed if required; in this case the 3 bit code representing the 8 possible phase states passed to the look up table is provided directly via the serial interface.

3.1.2 Filters

Digital filtering is applied to the data from the modulator; the coefficients are set as default to give a Root Raised Cosine response with Roll-off factor of 0.35. These FIR filters operate at 8x the incoming symbol rate and are configured, for each channel, as two filters in cascade; the first filter has 79 taps and the second filter has 49 taps. The first filter is used to enhance stop-band rejection and act as a sampling correction filter and the second filter provides the primary shaping. Coefficients for the filters may also be downloaded to the device via the serial interface; this gives the opportunity, if required, to fine tune the frequency response of a complete system to minimize the BER or to use the device in other applications. The filters can also be by-passed if required.

3.1.3 Gain Multiplier

This circuitry allows independent external control of the digital amplitudes in the I and Q channels to 12 bits of resolution. Extra circuits allow a mode of operation which will enable linear ramping up to a maximum value, stay at this value for a specified duration, then ramp back down to zero. The maximum value for each channel, the duration at maximum, the ramping up rate and the ramping down rate are all programmable via the serial interface.

3.1.4 Offset Adjust

Offset registers allow any offsets introduced in the analog sections of the transmit path to be corrected digitally via the serial interface. The offset adjust will have a resolution of 1 LSB and a maximum value of 0.25 full scale.

3.1.5 Sigma-Delta D-A Converters and Reconstruction Filters

The converters are designed to have low distortion and have >80dB dynamic range. These 3rd order converters are operated at a frequency of 128 x Symbol rate so as to oversample the data at their inputs a further 16 times. The reconstruction filters are 5th order, switched capacitor, low pass filters designed to work in conjunction with an external RC.

3.1.6 Phase Predistortion

A further feature allows the user to compensate for non-orthogonal carrier phase in the external quadrature modulator by adding a programmable fraction of up to 1/8 of the filtered I and Q channel signals to each other immediately prior to the DAC input.

The features described above should allow maximum flexibility for the user to predistort the baseband processing to compensate for nonidealities in the IF, RF and RF linear amplifier sections.

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Parameter	MX980	Units	Conditions/Comments
Input bit rate	36	Kbps	2 bits/symbol
No. of channels	2		I and Q
Modulation type	π/4 DQPSK		
RRC Roll-off coefficient (a)	0.35		
|H(f)| 0 - 5.85kHz	0 ± 0.3	dB	0 dB corresponds to 1V pk-pk
|H(f)| @ 9kHz	-3 ± 0.3	dB	
|H(f)| @ 10.05kHz	-6 ± 1.0	dB	
|H(f)| @ 12.15kHz	< -30	dB	
Max spurii			Relative to maximum passband signal level
@ 16kHz	-60	dBc	
@ 25kHz	-68	dBc	
@ 50kHz	-78	dBc	
@ 75kHz	-80	dBc	
FIR filter sampling rate	144	kHz	
DAC output update rate	2.304	MHz	
DAC resolution	12	Bits	
Integral accuracy	< ±0.5	LSB	
Differential accuracy	< ±0.25	LSB	
Offset	< 25	mV	Without adjustment
Gain matching, I to Q	< ± 0.1	dB	Without adjustment, 0 - 10kHz
Gain matching, (I or Q) to ideal Tx	< ± 0.3	dB	After adjustment, 0 - 10kHz
Phase matching, I to Q	< ±0.5	Degrees	0 - 10kHz
Storage time	< 14	Symbols	
Active Power	<100	mW	
Vector Error			Vector errors measured with ideal IF and RF sections after gain and offset adjustment
Vector Error (rms, typical)	0.017		
Vector Error (rms, max)	0.025		
Vector Error (peak, typical)	0.045		
Vector Error (peak, max)	0.07		

Table 1: Transmit Parameters

Notes:

1. All parameters refer to the entire baseband I and Q channels, unless otherwise indicated.
2. A gain multiplier function allows independent proportional control of each channel; the multiplier is a 12 bit word for each channel, input via the serial interface, representing a value from 0 to 1. This multiplication is applied to the signals from the FIR filters.
3. A facility is provided to allow linear ramping of the outputs; this is accomplished, if enabled, by multiplying the gain multiplier words by the ramping control register (RCR) value. The RCR is a 12 bit word, representing a value from 0 to 1, which is designed to increment by an amount (INC) until its maximum value. This value is held until a number of symbol times from the start of transmission (TRD) when RCR decrements by an amount (DEC) until zero. INC, DEC and TRD are all 12-bit words input via the serial interface prior to the start of a transmission.
4. Offset adjustment for each channel is available by loading a 12-bit word into the transmit offset register via the serial interface.

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.2 Receive Description

3.2.1 Anti-Alias Filtering and Sigma-Delta A-D Converters

The sampling frequency of the Sigma-Delta A-D is 128 x symbol rate which eases the design requirements on the anti-alias filter. However, to achieve optimum performance the anti-alias filter must reject this frequency to about -110dB, of which at least 40dB must be provided externally. Additionally, in order to ease the complexity of the subsequent digital filters, there is a further requirement that the anti-alias filter suppress 8 x Symbol rate to about -30dB. The on-chip anti-alias filter is designed to achieve this when used in conjunction with some external filtering. If required, the on-chip anti-alias filter can be by-passed and powered down, although external anti-aliasing must then be provided. The 4th order Sigma-Delta A-D converters are designed to have low distortion and >96dB dynamic range. The baseband I and Q channels must be provided as differential signals; this minimizes in-band pick up both on and off the chip.

3.2.2 Filters

Digital filtering is applied to the data from the Sigma-Delta A-D converters; the coefficients are set as default to give a Root Raised Cosine response with Roll-off factor of 0.35. These FIR filters are configured, for each channel, as three filters in cascade. The first filter gives sufficient rejection at 8 x Symbol rate to permit decimation at that frequency (note that -30dB is provided by the primary anti-alias filters). The second filter has 63 taps and is used to enhance stop-band rejection. The third filter has 49 taps and provides the primary shaping requirements. Coefficients for the second and third filters may be downloaded to the device via the serial interface; this gives the opportunity, if required, to fine tune the frequency response of a complete system to minimize the BER or to use the device in other applications. The filters can also be by-passed if required.

3.2.3 Offset Registers

System generated offsets may be removed by control of the offset register via the serial interface.

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

PARAMETER	MX980	Units	Conditions/Comments
With internal anti-alias filter disabled			
Input impedance	<10	pF	Capacitive load to Gnd.
Differential Input voltage range	1	V pk-pk (Typ)	Note this means ±0.25V on each input of the diff. pair.
3rd order intercept	tbd		
Anti -alias requirements			
@ 130kHz	<-30	dB	w.r.t. max. input level
@ 2.3MHz	<-120	dB	w.r.t. max. input level
ADC sampling rate	2.304	MHz	
ADC resolution	16	Bits	
Integral accuracy	< ±1	LSB	
Differential accuracy	< ±1	LSB	
RRC Roll-off coefficient (a)	0.35		
|H(f)| 0 - 5.85kHz	0 ± 0.2	dB	0 dB corresponds to 1V pk-pk
|H(f)| @ 9kHz	-3 ± 0.2	dB	
|H(f)| @ 10.05kHz	-6 ± 1	dB	
|H(f)| @ 12.15kHz	< -30	dB	
|H(f)| @ 16kHz	< -70	dB	
|H(f)| @ 25kHz	< -70	dB	
|H(f)| @ 50kHz	< -80	dB	
|H(f)| @ 75kHz	< -90	dB	
FIR filter sampling rate	2.304	MHz	Decimation sections
	144	kHz	RRC sections
Output rate (16 bit words per channel) - selectable	144	kHz	These are output via the serial interface at 4.608 MHz
Offset	or 72	kHz	Without adjustment
Gain matching, I to Q	< 10	mV	Without adjustment, 0 -10kHz
Phase matching, I to Q	< ± 0.1	dB	0 - 10kHz
Storage time	< ±0.5	Degrees	
Active Power	< 14	Symbols	
	<100	mW	
With internal anti-alias filter enabled:-			
Input impedance	>10	kΩ	Source should be < 100 Ω
Differential Input voltage range	1	V pk-pk (Typ)	Note this means ±0.25V on each input of the diff. pair.
3rd order intercept	tbd		
Anti -alias requirements			
@ 2.3MHz	<-30	dB	
Active Power	<110	mW	w.r.t. max. input level

Table 2: Receive Parameters

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Notes:

1. Offset adjustment for each channel is available by loading a 16 bit word into the receive offset register via the serial interface.
2. Optimally, anti-alias filtering should be carried out as much as possible prior to any AGC function before the receive inputs. This would allow the AGC to act on a reduced bandwidth signal and thereby improve the relative magnitude of the wanted part. The device has been designed to reduce the complexity of any external anti-alias filter as much as possible and a 4 pole Butterworth with a -3dB point at about 60kHz should be adequate. The internal anti-alias filter, if used, cannot provide the required -110dB attenuation at 2.3MHz and must be supplemented by external filtering. The most simple supplementary system may be a one or two pole filter before the AGC and an RC after the AGC with a -3dB point on each filter of about 200kHz.

3.3 Auxiliary Circuits

3.3.1 10-Bit DACs

Four 10 bit DACs are provided to assist in a variety of control functions. The DACs are designed to provide an output as a proportion of the supply voltage, depending on the digital input. They are monotonic with an absolute accuracy of better than 1%. Control and Data for these come via the serial interface.

3.3.2 10-Bit ADC

A 10 bit ADC is provided to assist in a variety of measurement and control functions. The ADC is designed to produce a digital output proportional to the input voltage; full scale being the positive supply. It is monotonic with an absolute accuracy of about 1%. An input multiplexer allows the input to be selected from 4 sources. Control and digital data output is via the serial interface.

3.3.3 Power Ramping and Control

One of the DACs has an additional feature which enables a previously downloaded set of values to be sequenced out at a preselected frequency. This is aimed at enabling power ramping of a RF output with a suitable profile. The sequence may be reversed for power down.

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

PARAMETER	MX980	Units	Conditions/comments
DACs			
Resolution	10	Bits	
Settling time to 0.5 LSB	<10	µSec	Worst case large signal transition
Output resistance	<250	Ω	
Integral non-linearity	<4	Bits	Guaranteed Monotonic
Differential non-linearity	<1	Bit	
Zero error (offset)	±20	mV	
Power (all DACs operating)	<10	mW	
Minimum Resistive Load	5	KΩ	
RMS output noise voltage in 30KHz bandwidth	10	µV	
ADC and Multiplexed inputs			
Maximum input source impedance	25	KΩ	Gives < 1 bit error
Resolution	10	Bits	
Maximum input signal "linear rate of change" for < 1 bit error	0.27	mV/µs	
Conversion time	12	µSec	
Integral non-linearity	<2	Bits	No missing codes
Differential non-linearity	<1	Bit	
Zero error (offset)	±20	mV	
A-D Clock frequency	MCLK/8		
Input capacitance	<5	pF	
Power	<3	mW	

Table 3: Auxiliary Parameters

3.4 IRQ Function

An interrupt request (IRQ) pin is provided for asynchronous communication with an external processor. The IRQ (asserted low) will be asserted when any of the error or user information flags are activated by an internal operation. The operations which generate an IRQ are:

1. An attempt to write to a full Tx data input FIFO
2. Default symbol data is being transmitted because the TX data input FIFO is empty
3. An internal arithmetic overflow has occurred in an FIR filter.

The cause of the IRQ can be obtained by reading the error flags register. All possible causes of an IRQ can also be masked by writing to the IRQ mask register.

Note: Default coefficients and settings have been optimized to maximize performance and should not cause arithmetic overflows. However, use of non-default coefficients, large offset corrections or large Tx phase adjustments may cause problems, which can be corrected by scaling down coefficients or via the gain multiplier feature.

© 1997 MX•COM, INC
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480167.001
All trademarks and service marks are held by their respective companies.

3.5 Serial Interface

All digital data I/O and control functions for the IC are via the serial interface. It is expected that the IC will be used in conjunction with a DSP and/or other processor. The device has three serial interface ports, each port is based on the industrial standard three wire serial interface. Both interfaces allow communication with standard DSP ICs using a minimum of external components. The three ports are:

Cmd Command port, generally this is an input port receiving data from the host, but may also be configured as a bi-directional IO interface.

RdCmd Command read port, an output port to send command read data back to the host. Read data is only sent on this port in response to a *Read Command*.

RxData Data receive port, an output port to send Receive data back to the host, data is only present on this interface when the *Receive Channel* is active. This port may also be configured as the *RdCmd* port.

Functions performed by the serial interface include:

1. Power up or down and optional bypassing of selected blocks
2. Setting digital filter coefficients
3. Loading ramp up and ramp down increments and burst lengths for TX
4. Loading and transmitting data
5. Loading offset correction, gain multiplier and phase adjustment registers
6. Enabling/disabling of output via the RX serial interface
7. Vary sampling time for RX data relative to the symbol (144kHz) clock.
8. Loading data into auxiliary DACs
9. Initiating conversions using auxiliary ADCs and reading results
10. Writing data to, and reading data from, the Power Ramping SRAM
11. Power Ramping timestep control

The interface consists of the following signal pins:

SClk	output	Serial clock pin. This pin is common for all three interfaces.
SCmdDat	input/ output	Command port data pin. This pin is by default an input, but may be configured as an *Open Drain* bi-directional pin.
SCmdFS	input	Command port *Frame Sync* pin. This pin is used to mark the first bit in a serial frame.
SCmdRdDat	output	Command read data port data pin. This pin only has active data on it in response to a *Read Command*.
SCmdRdFS	output	Command read data port *Frame Sync* pin. This pin is used to mark the first bit in a serial frame.
SRxDat	output	Receive data port data pin. This pin is only active when the *Receive Channel* is active.
SRxFS	output	Receive data port *Frame Sync* pin This pin is used to mark the first bit in a serial frame.

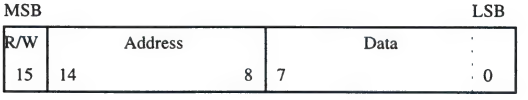
3.5.1 RxData Interface

The Rxdata interface is used only for outputting the I and Q received data. When data reception is enabled, I and Q received data will be output at either 8x or 4x the symbol rate under control of command registers RxSetup2. (see Section 3.6). This is achieved by reducing the serial interface clock rate from MCLK/2 to MCLK/4 and discarding alternate data samples under control of command registers ConfigCtrl1 and Rxsetup2. Sixteen bit I and Q data words are output at SRXDAT, MSB first (by default), on the rising edge of SCLK. SRXFS will go low during the output of each I data word and will go high during the output of each Q data word.

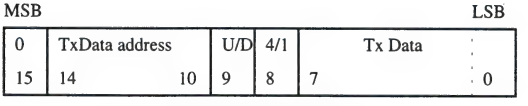
© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.5.2 Command Interface

A serial command word consists of a 16 bit frame. Each frame is marked by an active Frame Sync event which precedes the MSB bit. A command word can be either a control word or a command data word.

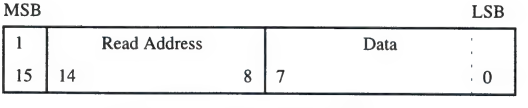


Command control serial word



Command transmit data serial word

Control read data is either output on one of the serial read ports, or driven out in the last 8 bits (data part) on the Cmd port. When control read data is output on a serial read port the read address is put in the top half of the word, and the read data in the lower half.



Read control response serial word

3.5.3 Data Transmission

Transmission data words are written to the TxData port address. This data may be in the form of either one or four two bit symbols, which are subsequently modulated into the DQPSK constellation, or three bit words which map directly into constellation points according to the table shown below.

Constellation map

3 bit code	000	001	010	011	100	101	110	111
I	1	0.7071	0	-0.7071	-1	-0.7071	0	0.7071
Q	0	0.7071	1	0.7071	0	-0.7071	-1	-0.7071

Two control bits are associated with each data transmission word. One controls the format of the word and the other initiates and terminates a transmission cycle. This close association enables precise control of the transmission frame. To relieve the user of the need to synchronize each TxData port write with the internal transmit cycle, transmit data words are written into an internal 4 deep FIFO. Symbols or constellation points are then read as needed from this FIFO. It is necessary to make sure that there is always a word to be read, and also that the FIFO is never written to when full. This may be accomplished by using one of two Data Interlock Mechanisms.

3.5.3.1 Data Interlock Mechanisms

There are two possible transmission data interlock mechanisms, the user must always use one of these methods.

1. Software polling.
2. Serial clock when ready.

Software polling requires the user to first check that the FIFO is not full before writing each TxData word. This may be accomplished by inspecting the relevant FIFO status bits before writing one or more transmit data words.

© 1997 MX•COM, INC
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480167.001
All trademarks and service marks are held by their respective companies.

The Serial Clock when ready method is a hardware interlock mechanism (enabled by setting the TxHandshakeEn bit active), this mechanism allows the user to send transmit data to the device without doing any FIFO checks. This hardware handshake is implemented by stopping the serial port clock when the FIFO is full. To prevent a serial port lockout condition the handshake is only enabled once the transmission frame has been initiated and is automatically disabled at the end of a frame. This mechanism should be used with care, because stopping the clock will freeze all other serial port transfers (common serial port clock).

3.5.3.2 Power Ramping and Frame Interlock

The RampUp bit in the TxData word is used to control both the Power Ramping function and the frame activation. To start a transmission frame, a transmission word is written with the RampUp bit active. All subsequent TxData words prior to frame termination must also have this bit active. The frame is terminated by writing transmit data words with the RampUp bit inactive. Subsequent TxData words must also have this bit inactive, until initiation of a new frame is required. While the power Ramping is active (up or down) the user must supply transmission symbols, or valid constellation points. Once the ramp down operation has completed all subsequent TxData writes with the RampUp bit inactive will be ignored

3.5.4 Control Words

A Control word either directly accesses an internal register for a read or write operation, or acts as a data port to internal memory. For test purposes all registers that can be written may also be read, though not all registers may be written, some are just status registers. Each register or data port is assigned a unique address, the whole address range is reserved for this device, if more than one device is to be accessed using the same serial port, the device should be selected by the optional Chip Select pin (CS).

All internal memory access is via a data port. First a control word access is used to reset the internal address pointer, then data port access operations post increment this address pointer.

3.5.5 Command Word Description

The following sections describes in detail each of the addressed Command Words.

3.5.5.1 Key to Register Map

Each section that follows describes in detail the operation and use of each of the registers in the device. The registers are split into their functional groups, grouping associated registers together. Each section consists of a Title Section, an Address Specifier, a Function Reference Field, a Description Block, and a Bit Specification Section.

Title Section	Title of section
Address Specifier	Address for this section.
Function Reference Field	Overall access available to the section (RW/W/R)
Description Block	Description of the section.
Bit Specification Section	This section describes the function of each individual bit, or a range of bits within a register. There is a separate line for each distinct field of bits. The fields in this line are:
Bit Specifier	bit number or range of bits.
Bit type	Type of bit field, active high, low, or just data.
Operator field	Valid operation for this bit field, RW/R/W

There may be an address offset specified before a Bit Specification Section, this indicates the register address offset for the next bit fields from the address specified in the Address Specifier.

3.5.5.2 Register Reset State

All IO access registers (both read & write) are reset to logic zero on Reset. The reset state of status bits will depend on the level of the status signal being monitored.

3.6 Register Description

3.6.1 ConfigCtrl 1

Title	Configuration control register
Address	
Function	RW
Description	General configuration bits, together with operational control signal bits.

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Bit	Name	Active State		Function
0	SymbModuBypass	High	RW	Setting this bit bypasses the *Symbol Modulator*, thereby taking the least significant 3 bits of each *TxDataReg* word received over the serial interface to represent an absolute constellation mapping.
1	RdCmdPortDisable	High	RW	When set active tristates the RdCmdDat and RdCmdFS pins.
2	RxDataPortDisable	High	RW	When set active tristates the RxDataDat and RxDataFS pins.
3	LowRxRdFS	High	RW	When set active both the RdCmdFS and the RxDataFS output pins will be driven active low, when set inactive the two frame sync's will be driven active high (default).
(5,4)	Command Read Data Mode		RW	The *BiDirCmdPortEn* bit and *RxDataForCmdRdEn* bit together control the method command read data is sent back to the user.
		00	(Default)	Read data driven out on *CmdRd* port.
		01		Read data driven out on *RxData* port.
		10,11		Read data driven out on *Cmd* port.
4	BiDirCmdPortEn	High	RW	When this bit is set active the Cmd port will drive its data line out of the chip for the last 8 bits of read operations. When set inactive command read data will be driven out on either the RdCmd port or the RxData port (default).
5	RxDataForCmdRdEn	High	RW	This bit only takes effect if the *BiDirCmdPortEn* bit is inactive. When set active this bit causes all command read operations to respond with data on the RxData serial port. When set inactive the command read data will be output via the *RdCtrl* port (default).
6	TxHandshakeEn	High	RW	When set active enable the transmit hardware interlock protocol, thereby stopping the serial clock (SerialClk) if the transmit path is enabled and the transmit FIFO is full
7	DataRateHi	High	RW	When set active all serial port data transfers will be at half of the master clock rate. When inactive, all serial port data rates will be at a quarter of the master clock rate. This has the effect of altering the Rx sample output rate from 8 times the symbol rate when active. to 4 times when inactive. See Rxsetup2 for more details.

3.6.2 ConfigCtrl 2

Title	Configuration control register
Address	
Function	RW
Description	General configuration bits, together with operational control signal bits.

Bit	Name	Active State		Function
0	n_BigEndData	Low	RW	When set active cause all serial port read data, for both the RdCmd and RxData port to be generated with the MSB data word bit in the first serial word bit. If inactive, the LSB is first. On Reset this bit is active.
1	CoeffRamIoEn	High	RW	When set active allows read/write access to all the coefficient memories. It is only valid to activate this bit when the Transmit and Receive Path are inactive. When this bit is set active, the first access to any of the coefficient memories will access the first coefficient location (A0). Subsequent read or write accesses to any coefficient memory will

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

				increment the address pointers for all the coefficient memories.
2	CoeffRamIoRdInc	High	RW	This bit determines whether a read or write operation to a coefficient memory will increment the address pointers. When set active the address pointer is incremented by any coefficient ram read operation, thereby allowing a write then read verification. When set inactive write operations increment the address pointer.
3	SRamIoEn	High	RW	When set active allows read/write access to the Auxiliary SRAM. It is only valid to activate this bit when the SRAM is not being accessed by the RamDac. When this bit is set active, the first access to the SramData port will access the first SRAM address location.. Subsequent read or write accesses will increment the address pointer to the next memory location.
4	SRamIoRdInc	High	RW	This bit determines whether a read or write operation to the Auxiliary SRAM will increment the address pointers. When set active causes read operations to move the address pointer on, this would therefore allow an efficient write then read verify scheme to be used. When set inactive write operations increment the address pointer.
7:5	NU			

3.6.3 PowerDownCtrl

Title	Power control register
Address	
Function	RW
Description	This register together with the *TxEn* and RxEn bits controls the power saving features.

Bit	Name	Active State		Function
0	RxAafPowEn	High	RW	When set active powers down the receive analog AAF.
1	AuxDac1PowDn	High	RW	When set active powers down Auxiliary Dac1.
2	AuxDac2PowDn	High	RW	When set active powers down Auxiliary Dac2.
3	AuxDac3PowDn	High	RW	When set active powers down Auxiliary Dac3.
4	AuxDac4PowDn	High	RW	When set active powers down Auxiliary Dac4.
5	BiasPowDn	High	RW	When set active powers down the analog bias section.
6,7	NU			

3.6.4 TxSetup

Title	Transmit setup register
Address	
Function	RW
Description	

Bit	Name	Active State		Function
0	n_TxFirCoeffReset	Low	RW	When set active this bit forces all the Transmit Path filters to load their default coefficient values. This bit will be set active on Reset, and therefore needs to be deactivated before default filter coefficients can be overwritten.
1	TxPowRampEn	High	RW	When set active, this bit enables the transmit power ramping function, ramping is then controlled by the TxRampUp (TxRampUp see TxDataReg spec). When this bit is inactive, the TxRampUp bit will directly control the transmit amplitude (Up meaning full amplitude, Down

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

				zero).
2	TxEn	High	RW	When set active, enables the Transmit Path, allowing transmission to start when the correct enable sequence has been seen. This bit may only be cleared when the TxPathEn status bit is inactive, setting inactive during a transmission cycle will cause erroneous behaviour. This bit also acts as a transmit section power enable bit.
3	TxClkStop	High	RW	When set active causes the TxEn bit to also be used to gate the Transmit Path master clock. When inactive (default state) the Transmit Path master clock is always supplied.
7:4	NU			

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.5 TxData

Title	Transmit data register
Address	(Mapped over four locations, two address bit being used as data bits)
Function	
W	FIFO input
R	FIFO output
Description	This transmit data register is 10 bits wide, it utilizes the least significant two bits of the address bus to drive bits 8 and 9, hence it can be considered to be mapped over four consecutive locations. This data word is written into a *FIFO*. The function is only decoded when the *FIFO* is read (there is an exception for the first data word). The *FIFO* will be read when the *Transmit Path* demands data. This will only occur when the *TxEn* bit is set active. For test purposes the *FIFO* data output may be accessed by reading this registers.

Data write with symbol modulator not bypassed.				
Bit	**Name**	**Active State**		**Function**
1:0	TxRelSymbol1	Data	W	First symbol in word to be written to FIFO.
3:2	TxRelSymbol2	Data	W	Second symbol in word to be written to FIFO.
5:4	TxRelSymbol3	Data	W	Third symbol in word to be written to FIFO.
7:6	TxRelSymbol4	Data	W	Fourth symbol in word to be written to FIFO.
8	MultSymbol	High	W	This bit is written to the FIFO, and when set active the symbol data written to the FIFO will be marked as a four symbols word. This bit has no meaning if the SymbModuBypass bit is active.
9	TxRampUp	High	W	This bit is written to the FIFO. When it is changed while the TxEn bit is active, it will control the Transmit Path Ramping action; setting it active will cause the amplitude to ramp up to its full value, conversely setting the bit inactive will cause the amplitude to ramp down to its minimum value. If the bit is changed while the amplitude is being ramped, the ramp direction will change to the direction set by this bit.
Data write with symbol modulator bypassed.				
Bit	**Name**	**Active State**		**Function**
2:0	TxAbsSymbol	Data	W	IQ constellation point which is written into the FIFO.
8:3	NU	Data	W	Redundant data which is still written into the FIFO.
9	TxRampUp	High	W	(See above)
Data read with or without symbol modulator bypassed.				
Bit	**Name**	**Active State**		**Function**
Address offset 0				
1:0	UpperFIFORdData	Data	R	Reading address access bits 9 and 8 of the FIFO data output register, these are placed in bits 1 and 0.
Address offset 1				
7:0	LowerFIFORdData	Data	R	Reading address access bits 7 to 0 of the FIFO data output register. Reading this location also performs a FIFO read operation, thereby moving the next (if any) FIFO data location into the FIFO data output register.

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.6 RxSetup 1

Title	First receive setup control register
Address	
Function	RW
Description	Receive path setup and initialization control bits.

Bit	Name	Active State		Function
0	RxFirCoeffReset	Low	RW	When set active forces all the Receive Path filters to load their default coefficient values. This bit will be set active on Reset, and therefore needs to be deactivated before default filter coefficients can be overwritten.
1	AnaAutoReset	Low	RW	When active this bit enables the ADC auto reset function. On Reset this bit is set active, the default operating condition.
2	AnaAdcReset	Pulse		
			W	When a logic 1 is written to this bit, a four clock cycle ADC Auto Reset event is generated. It is not necessary to clear this bit before another ADC Auto Reset event is initiated.
			R	The read state of this bit indicates the logic level last written to this bit. It does not have a functional significance, and is only available for test purposes.
3	NU	Data	RW	Present only for test purposes.
7:4	VernierDelay	High	RW	Vernier sampling delay, allowing the sampling point to be adjusted to a resolution of 1/16 of the input sample clock rate

3.6.7 RxSetup 2

Title	Second receive setup control register
Address	
Function	RW
Description	Receive path setup and initialization control bits.

Bit	Name	Active	State	Function
0	RxEn	High	RW	When set active, enables the Receive Path, which then starts to process the differential data on the IRXP,IRXN and QRXP,QRXN pins, outputting results via the RxData serial port. This bit also acts as a receive section power enable bit.
1	TxClkStop	High	RW	When set active causes the RxEn bit to also be used to gate the Receive Path master clock. When inactive (default state) the Receive Path master clock is always supplied.
2	RxSampleSel	High	RW	This bit is used to select which I and Q value is selected out of the possible two when the RxDataRateHi is in the low mode (inactive).
7:3	NU			

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.8 AnaCtrl

Title	Analog Configuration Control register
Address	
Function	RW
Description	For manufacturer's use only

Bit	Name	Active State		Function
2:0	AdcTestCtrl	Data	RW	These mode bits allow test access to the internal functions of the Sigma Delta ADC.
		Mode		**Function**
		000		Normal operational mode (default).
		001		Internal integrator 1's output driven out on the AuxAdc pins. Pins driven: I+ → AuxAdc1, I– → AuxAdc2, Q+ → AuxAdc3, Q– → AuxAdc4
		010		Internal integrator 2's output driven out on the AuxAdc pins. Pins driven: I+ → AuxAdc1, I– → AuxAdc2, Q+ → AuxAdc3, Q– → AuxAdc4
		011		Internal integrator 3's output driven out on the AuxAdc pins. Pins driven: I+ → AuxAdc1, I– → AuxAdc2, Q+ → AuxAdc3, Q– → AuxAdc4
		100		Internal integrator 4's output driven out on the AuxAdc pins. Pins driven: I+ → AuxAdc1, I– → AuxAdc2, Q+ → AuxAdc3, Q– → AuxAdc4
		101		ADC P output driven out on AuxAdc1 and AuxAdc3 pins. Pins driven: I→AuxAdc1, Q→AuxAdc3
		110		Analog AAF outputs driven out on to AuxAdc pins. Pins driven: I+ → AuxAdc1, I– → AuxAdc2, Q+ → AuxAdc3, Q– → AuxAdc4
		111		AuxAdc pins used to override the Sigma Delta ADC outputs. Pins driven: AuxAdc2 → I, AuxAdc4 → Q
5:3	DacTestCtrl	Data	RW	These mode bits allow test access to the internal functions of the Sigma Delta DAC.
		Mode		**Function**
		000		Normal operational mode (default).
		001		DAC modulator I driven onto the AuxAdc pins. Pins driven: Modulator bits[2:0] → AuxAdc[3:1]
		010		I channel DACp, DACn and Q channel DACp, DACn override ITXP, ITXN, QTXP, QTXN.
		011		I channel FILTp, FILTn and Q channel FILTp, FILTn override ITXP, ITXN, QTXP, QTXN.
		100		DAC modulator Q driven onto the AuxAdc pins. Pins driven: Modulator bits[2:0] → AuxAdc[3:1]
		101		AuxAdc pins drive I, Q DAC reconstruction filters. Pins driven: AuxAdc[3:1} → Modulator bits[2:0]
		110		AuxAdc pins drive I, Q DAC reconstruction filters (AuxAdc[3:1} → Modulator bits[2:0]). I channel DACp, DACn and Q channel DACp, DACn override ITXP, ITXN, QTXP, QTXN.
		111		AuxAdc pins drive I, Q DAC reconstruction filters (AuxAdc[3:1} → Modulator bits[2:0]) I channel FILTp, FILTn and Q channel FILTp, FILTn override ITXP, ITXN, QTXP, QTXN.
7,6	NU			

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.9 AuxAdcCtrl

Title	Auxiliary ADC data converter control register
Address	
Function	RW
Description	This register controls the operation of the four ADC channels. A little understanding of the implementation of the ADC's is needed to use them correctly. The ADC's block is implemented using a single ADC converter, multiplexed on to each of the ADC channels. A conversion cycle consists of performing a conversion for each of the active channels in turn.

Bit	Name	Active State		Function
0	StartConvert	High		Single conversion control bit, this bit only has a valid meaning when the ADC's are set to single conversion mode.
			W	Writing a one to this bit starts the ADC data conversion. A zero may also be written to clear this bit, but clearing should only be used for test purposes, because the ADC conversion logic will automatically clear this bit when the conversion operation has completed.
			R	This bit is set or cleared by the serial interface, but the ADC conversion logic will automatically clear it when the current conversion cycle has completed.
1	EnableAdc1	High	RW	Setting this bit high will enable ADC channel 1 for conversion. This bit may be updated at any time, but will only change the active state of the ADC channel for the next time it is converted.
2	EnableAdc2	High	RW	Setting this bit high will enable ADC channel 2 for conversion. This bit may be updated at any time, but will only change the active state of the ADC channel for the next time it is converted.
3	EnableAdc3	High	RW.	Setting this bit high will enable ADC channel 3 for conversion. This bit may be updated at any time, but will only change the active state of the ADC channel for the next time it is converted.
4	EnableAdc4	High	RW	Setting this bit high will enable ADC channel 4 for conversion. This bit may be updated at any time, but will only change the active state of the ADC channel for the next time it is converted.
5	AdcContConv	High	RW	Continuous conversion mode control bit; when inactive, sets the ADC's into single conversion mode; when Active the ADC's will continuously convert. Single conversion mode is initiated by the StartConvert bit. In Continuous convert mode, the ADC will start a new conversion cycle on all active channels after the previous cycle has completed.
6	AdcConvertRate	High	RW	This bit changes the ADC conversion rate. If this bit is zero the ADC is clocked by MCLK/8, yielding a conversion time of MCLK/80 per ADC channel. Setting this bit high will halve the ADC clock rate, and hence double the conversion time.
7	NU			

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.10 AuxAdcData

Title	Auxiliary ADC Data registers
Address	(Eight registers)
Function	R
Description	These registers enable the user to inspect the conversion value for each of the four auxiliary ADC's. There are two read registers per ADC, one to obtain the least significant 2 bit of the data, the other for the eight most significant bits. Reading these registers does not affect the ADC conversion cycle. Reading the MSB read register directly reads the ADC output and simultaneously causes the 2 LSB's of the ADC data to be written into a holding register. This holding register is read when the LSB read register is read. This mechanism is necessary to allow the user to read MSB and LSB data from the same ADC conversion cycle. If only the MSB read register is read the converter can be considered as an 8 bit ADC.

Bit	Name	Active	State	Function
	Address Offset 0			
7:0	Adc1LsbData	Data	R	Least significant eight bits of the data from the last conversion of AuxAdc1.
	Address Offset 1			
1:0	Adc1MsbData	Data	R	Most significant two bits of the data from the last conversion of AuxAdc1.
7:2	NU			
	Address Offset 2			
7:0	Adc2LsbData	Data	R	Least significant eight bits of the data from the last conversion of AuxAdc2.
	Address Offset 3			
1:0	Adc2MsbData	Data	R	Most significant two bits of the data from the last conversion of AuxAdc2.
7:2	NU			
	Address Offset 4			
7:0	Adc3LsbData	Data	R	Least significant eight bits of the data from the last conversion of AuxAdc3.
	Address Offset 5			
1:0	Adc3MsbData	Data	R	Most significant two bits of the data from the last conversion of AuxAdc3.
7:2	NU			
	Address Offset 6			
7:0	Adc4LsbData	Data	R	Least significant eight bits of the data from the last conversion of AuxAdc4.
	Address Offset 7			
1:0	Adc4MsbData	Data	R	Most significant two bits of the data from the last conversion of AuxAdc4.
7:2	NU			

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.11 RamDacCtrl

Title	RamDac control register
Address	
Function	RW
Description	This register controls the operation of DAC 1, together with the operation of the memory (DacSram) which can be used to drive the digital input of DAC 1.

Bit	Name	Active State		Function
0	RamDacActive	High	RW	DAC 1 input mode bit. When inactive, the DacData1 input register is used as the source for conversion. If this bit is active the DAC is driven from the output of the RamDac memory.
1	AutoCycle	High	RW	This bit is only valid if the if the RamDacActive bit is active. When set active the DacSram memory will be continually scanned at the rate set by the RamDacRate bits, this enables a symmetrical periodic waveform to be driven out on the AuxDac1 pin. The DacSram address cycles from the bottom location up to the top location, and back down to the bottom again.
2	RamDacInc	High	RW	This bit activates the RamDac memory scan operation. setting it active will cause the memory address to increment up to the top location, conversely setting the bit inactive will cause the memory address to decrement down to the bottom location. If the bit is changed while the memory is being scanned, the current scan will complete before the new state of the RamDacInc bit takes effect.
5:3	RamDacRate	High	RW	These three bits set the rate at which the RamDac memories DAC access address pointer changes. The three bit value (RamDacRate) causes a change rate of (144 * 2^RamDacRate) kHz.
7:6	NU			

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.12 AuxDacData

Title	Auxiliary DAC Data register
Address	(Eight registers)
Function	RW
Description	There are two *DacData input* registers. for each of the four auxiliary DACs Writing to the *AuxDacLsbData* register writes the two least significant bits of the *DacData* register. Writing to the *AuxDacMsbData* register writes the eight most significant bits of the *DacData* register and passes all ten bits to the appropriate DAC input (only if the *RamDacMode* bit is cleared for *AuxDac1*). If the *AuxDacMsbData* register is written while the *RamDacLsbData* register is left constant, the converter may be considered as an 8 bit DAC.

Bit	Name	Active	State	Function
Address Offset 0				
1:0	AuxDac1LsbData	Data	RW	Writing to this address writes the least significant 2 bits of the DacData1 register. These two bits may be read for test purposes.
7:2	NU			
Address Offset 1				
7:0	AuxDac1MsbData	Data	RW	Writing to this address writes the most significant 8 bits of the DacData1 register and updates DAC1. This register may also be read for test purposes.
Address Offset 2				
1:0	AuxDac2LsbData	Data	RW	Writing to this address writes the least significant 2 bits of the DacData2 register. These two bits may be read for test purposes.
7:2	NU			
Address Offset 3				
7:0	AuxDac2MsbData	Data	RW	Writing to this address writes the most significant 8 bits of the DacData2 register and updates DAC2. This register may also be read for test purposes.
Address Offset 4				
1:0	AuxDac3LsbData	Data	RW	Writing to this address writes the least significant 2 bits of the DacData3 register. These two bits may be read for test purposes.
7:2	NU			
Address Offset 5				
7:0	AuxDac3MsbData	Data	RW	Writing to this address writes the most significant 8 bits of the DacData3 register and updates DAC3. This register may also be read for test purposes.
Address Offset 6				
1:0	AuxDac4LsbData	Data	RW	Writing to this address writes the least significant 2 bits of the DacData4 register. These two bits may be read for test purposes.
7:2	NU			
Address Offset 7				
7:0	AuxDac4MsbData	Data	RW	Writing to this address writes the most significant 8 bits of the DacData4 register and updates DAC4. This register may also be read for test purposes.

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.13 LoopBackCtrl

Title	Loopback control register
Address	
Function	RW
Description	This register is only used for test purposes, for normal operation all these bits should be inactive.

Bit	Name	Active State		Function
0	TxtoRxDataPath	High	RW	Tx (I,Q) DAC input to serial receive port (RxData). This enables the output of the transmit 15 tap filter to be observed in real time.
1	TxDPAccessSel	High	RW	When set active this bit disables the Transmit Path sample clock, thereby enabling the DataPath access register to directly update the input to the 15tap digital filter without the data being overridden by subsequent sample clocks.
2	RxDPAccessSel	High	RW	When set active this bit disables the Receive Path sample clock, thereby enabling the DataPath access register to directly update the output of the RX DataPath operator.
3	AnaLoopBack	High	RW	When set active this bit enables the analog loopback feature. This connects the output of the Transmit Path ADC to the input of the Receive Path DAC, thereby allowing loopback through the digital interfaces.
4	DigLoopBack	High	RW	When set active this bit enables the digital loopback feature. This connects the output of the Receive Path 49tap filter to the input of the Transmit Path 79tap digital filter, thereby allowing loopback via the analog pins.

3.6.14 TxErrorStatus

Title	Transmit Error Status register.
Address	
Function	R (Read only status register).
Description	This register acts as both the transmission path error status register, and an interrupt generation source status register. The *IrqActive* bit is active if one of the bits in this register is the source of an interrupt. All these error conditions are caused by transitory events, therefore the error condition is latched (marked with an 'L'). Reading this status register cause all its latched bits to be cleared to their deactivated state, unless they are currently being activated.

Bit	Name	Active State		Function
0	IrqActive	High	RL	This bit is set high if their is an active interrupt caused by one of the status bit in this register.
1	Tx79tapOF	High	RL	79 tap I and Q filter data accumulator overflow error status bit
2	Tx49tapOF	High	RL	49 tap I and Q filter data accumulator overflow error status bit.
3	Tx15tapIOF	High	RL	15 tap I filter data accumulator overflow error status bit.
4	Tx15tapQOF	High	RL	15 tap Q filter data accumulator overflow error status bit.
5	TxDataPathIOF	High	RL	Data path GPO (Gain, phase, and offset) adjustment unit I channel overflow error status bit.
6	TxDataPathQOF	High	RL	Data path GPO adjustment unit Q channel overflow error status bit.
7	NU			

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.15 TxErrStatMask

Title	Transmit Error Status Interrupt Mask register
Address	
Function	RW
Description	Interrupt mask generation mask bit, on *Reset* these bit are set active, so masking out all possible interrupt sources. Each bit which is taken inactive will allow its associated status bit when active to generate an interrupt.

Bit	Name	Active State		Function
0	NU	Data		Only present for test purposes.
2	n_Tx79tapOF _Mask	Low	RW	49 tap I and Q filter error interrupt generation mask bit.
3	n_Tx49tapOF _Mask	Low	RW	49 tap I and Q filter error interrupt generation mask bit.
4	n_Tx15tapIOF _Mask	Low	RW	15 tap I filter error interrupt generation mask bit.
4	n_Tx15tapQOF _Mask	Low	RW	15 tap Q filter error interrupt generation mask bit.
5	n_TxDataPathIOF _Mask	Low	RW	GPO I channel error status interrupt generation mask bit.
6	n_TxDataPathQOF _Mask	Low	RW	GPO Q channel error status interrupt generation mask bit.
6,7	NU	Data	RW	Only present for test purposes.

3.6.16 RxErrorStatus

Title	Receive Error Status register.
Address	
Function	R (Read only status register).
Description	This register acts as both the receive path error status register, and an interrupt generation source status register. The *IrqActive* bit is active if one of the bits in this register is the source of an interrupt. All these error conditions are caused by transitory events, therefore the error condition is latched (marked with an 'L'). Reading this status register causes all its latched bits to be cleared to their deactivated state, unless they are currently being activated.

Bit	Name	Active State		Function
0	IrqActive	High	RL	This bit is set high if their is an active interrupt caused by one of the status bit in this register.
1	Rx59tapOF	High	RL	59 tap I and Q filter data accumulator overflow error status bit.
2	Rx49tapOF	High	RL	49 tap I and Q filter data accumulator overflow error status bit.
3	Rx63tapOF	High	RL	63 tap I and Q filter data accumulator overflow error status bit.
4	AdcIOF	High	RL	ADC I channel overflow error due to excessive amplitude.
5	AdcQOF	High	RL	ADC Q channel overflow error due to excessive amplitude.
6	RxDataPathIOF	High	RL	Data path GPO (Gain, phase, and offset) adjustment unit I channel overflow error status bit
7	RxDataPathQOF	High	RL	Data path GPO (Gain, phase, and offset) adjustment unit Q channel overflow error status bit

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.17 RxErrorStatMask

Title	Receive Error Status Interrupt Mask register.
Address	
Function	RW
Description	Interrupt mask generation mask bit. On *reset* these bits are set active, masking out all possible interrupt sources. Each bit which is taken inactive will allow its associated status bit, when active, to generate an interrupt.

Bit	Name	Active	State	Function
0	NU	Data		Only present for test purposes.
1	n_Rx59tapOF _Mask	Low	RW	59 tap I and Q filter error interrupt generation mask bit.
2	n_Rx49tapOF _Mask	Low	RW	49 tap I and Q filter error interrupt generation mask bit.
3	n_Rx63tapOF _Mask	Low	RW	63 tap I and Q filter error interrupt generation mask bit.
4	n_AdcIOF_Mask	Low	RW	ADC I channel error interrupt generation mask bit.
5	n_AdcQOF_Mask	Low	RW	ADC Q channel error interrupt generation mask bit.
6	n_RxDataPathIOF_Mask	Low	RW	GPO I channel error interrupt generation mask bit.
7	n_RxDataPathQOF_Mask	Low	RW	GPO Q channel error interrupt generation mask bit.

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.18 TxFIFOStatus

Title	Transmission Data FIFO Status register
Address	
Function	R (Read only status register).
Description	This register acts as both the Tx Data FIFO status register, and an interrupt generation source status register. The *IrqActive* bit is active if one of the bits in this register is the source of an interrupt. Some of these status conditions are caused by transitory events, therefore their state is latched (marked with an 'L'). The bits marked with a parenthesised 'L' are only latched in their interrupt generation state if their associated mask bit is inactive. Reading this status register causes all its latched bits to be cleared to their deactivated state, unless they are currently being activated.

Bit	Name	Active State		Function
0	IrqActive	High	RL	This bit is set high if there is an active interrupt caused by one of the status bit in this register.
1	FIFOEmpty	High	R(L)	When active indicates the FIFO is empty.
3:2	FIFOLength	(Low)	R(L)	Least significant two bits of FIFO length status.
				00 - indicates FIFO is empty
				01 - one location used
				10 - two location used
				11 - three location used
				For interrupt generation purposes a logic low on these bits will be considered as active.
4	FIFOFull	H/L	R(L)	Most significant FIFO length bit, when active also indicates the FIFO is full. For interrupt generation purposes a logic low on this bit will be considered as active.
5	FIFOOverWrite	High	RL	Error status bit, when active indicates a write to the FIFO occurred while it was full.
6	FIFOUnderRead	High	RL	Error status bit, when active indicates a read from the FIFO occurred while the FIFO was empty.
7	TxPathEn	High	R(L)	When active this bit show that the Transmit path is currently active. This bit enables the user to confirm Ramp Down has completed. For interrupt generation purposes a logic low on this bit will be considered as active.

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.19 TxFIFOStatMask

Title	Tx Data FIFO Status Interrupt Mask register
Address	
Function	RW
Description	Interrupt generation mask bit, on *Reset* these bits are set active, so masking out all possible interrupt sources. Each bit which is taken inactive will allow its associated status bit when active to generate an interrupt. Also in the case of the status bits marked with a parenthesised 'L', taking the mask bit inactive will enable the latching mechanism.

Bit	Name	Active State		Function
0	NU	Data	RW	Only present for test purposes.
1	n_FIFOEmpty_Mask	Low	RW	Interrupt generation mask bit.
2	n_FIFOLength0_Mask	Low	RW	Interrupt generation mask bit.
3	n_FIFOLength1_Mask	Low	RW	Interrupt generation mask bit.
4	n_FIFOFull_Mask	Low	RW	Interrupt generation mask bit.
5	n_FIFOOverWrite_Mask	Low	RW	Interrupt generation mask bit.
6	n_FIFOUnderRead_Mask	Low	RW	Interrupt generation mask bit.
7	n_TxPathEn_Mask	Low	RW	Interrupt generation mask bit.

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.20 CoeffRamData

Title	IO access addresses for the coefficient memories.
Address	(mapped over 10 locations)
Function	RW
Description	Each coefficient memory has two address ports assigned to it for read and write access. It is only valid to access the coefficient memory when the *CoeffRamIoEn* bit is active. After the *CoeffRamIoEn* has been taken active the *Coeff IO Access Address Pointer* will be reset to the first valid coeff location (A1). First the MSB port should be accessed, then the LSB port, accessing the LSB port will move the *Coeff IO Access Address Pointer* to the next coefficient value (refer to description of *CoeffRamIoRdInc* bit for full details). Therefore subsequent access to the LSB port will access incremental locations. Performing a valid IO access to the port after the last coefficient has been addressed is not valid, and will corrupt exist coefficients written. Only one coefficient memory may be accessed at one time, if further memories are to be accessed then the *CoeffRamIoEn* must first be deactivated, and then activated again, allowing another coefficient ram to be incrementally accessed.

Bit	Name	Active State		Function
Address offset 0				
7:0	Tx15tapCoeffLSB	Data	RW	Transmit 15 tap filter LSB coefficient data port.
Address offset 1				
3:0	Tx15tapCoeffMSB	Data	RW	Transmit 15 tap filter MSB coefficient data port.
7:4	NU			
Address offset 2				
7:0	Tx49tapCoeffLSB	Data	RW	Transmit 49 tap filter LSB coefficient data port.
Address offset 3				
3:0	Tx49tapCoeffMSB	Data	RW	Transmit 49 tap filter MSB coefficient data port.
7:4	NU			
Address offset 4				
7:0	Tx79tapCoeffLSB	Data	RW	Transmit 79 tap filter LSB coefficient data port.
Address offset 5				
3:0	Tx79tapCoeffMSB	Data	RW	Transmit 79 tap filter MSB coefficient data port.
7:4	NU			
Address offset 6				
7:0	Rx49tapCoeffLSB	Data	RW	Receive 49 tap filter LSB coefficient data port.
Address offset 7				
3:0	Rx49tapCoeffMSB	Data	RW	Receive 49 tap filter MSB coefficient data port.
7:4	NU			
Address offset 8				
7:0	Rx63tapCoeffLSB	Data	RW	Receive 63 tap filter LSB coefficient data port.
Address offset 9				
3:0	Rx63tapCoeffMSB	Data	RW	Receive 63 tap filter MSB coefficient data port.
7:4	NU			

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.21 SramData

Title	IO Access address for the Auxiliary DAC1 memories.
Address	(mapped over 2 locations)
Function	RW
Description	These two address locations allow access to the 64 x 10 bit SRAM. This SRAM is used in conjunction with DAC1 to enable profile power ramping of an external RF power transmitter stage. This memory is addressed incrementally, first the *SRamIoEn* bit is taken active, while this bit is inactive the *SRam Address Pointer* is held reset. Therefore the first IO access to the SRAM will access the first address location. The MSB is always accessed first, then the LSB, which also increments the *SRam Address Pointer* to the next memory address location. The *SRamIoRdInc* bit determines whether a read or a write operation will increment the *SRam Address Pointer*. All 64 locations are accessed incrementally, further accesses to this port while the *SRamIoEn* bit is active is not valid (may cause data loss)

Bit	Name	Active	State	Function
	Address offset 0			
7:0	SRamLSBPort	Data	RW	Access port for the LSB register.
	Address offset 1			
1:0	SRamMSBPort	Data	RW	Access port for the MSB register.
7:2	NU			

3.6.22 TxRampUpInc

Title	Transmit Ramp Up increment registers.
Address	(mapped over 2 locations)
Function	RW
Description	This register determines the ramp up time period, the value in this register determines the number of increments the signal amplitude increases by each sample clock period. The ramp up rate in terms of the number of symbols is given by the formula: $N_{symbols} = \frac{64}{N_{inc}}$ Where: $N_{symbols}$ is the ramp time in terms of number of symbols. N_{inc} is the value in the register.

Bit	Name	Active State		Function
Address offset 0				
7:0	RampUpIncLSB	Data	RW	Least significant 8 bits of the ramp up increment register.
Address offset 1				
1:0	RampUpIncMSB	Data	RW	Most significant 2 bits of the ramp up increment register.
7:2	NU			

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.23 TxRampDnInc

Title	Transmit Ramp Down increment registers.
Address	(mapped over 2 locations)
Function	RW
Description	This register determines the ramp down time period, the value in this register determines the number of decrements the signal amplitude increases by each sample clock period. The ramp down rate in terms of the number of symbols is given by the formula: $N_{Symbols} = \frac{64}{N_{inc}}$ Where: $N_{symbols}$ is the ramp time in terms of number of symbols N_{inc} is the value in the register

Bit	Name	Active State		Function
Address offset 0				
7:0	RampDnIncLSB	Data	RW	Least significant 8 bits of the ramp down increment register.
Address offset 1				
1:0	RampDnIncMSB	Data	RW	Most significant 2 bits of the ramp down increment register.
7:2	NU			

3.6.24 TxIQGainMult

Title	Transmit I & Q channel gain attenuation register
Address	(mapped over 4 locations)
Function	RW
Description	A twos-complement multiplication is performed on the *Transmit Channel* data path signal value, the result is then re-normalized to the systems dynamic range, thus the function may be considered as a digital attenuator. This register sets the multiplicand, the result being given by the formula: $S_{out} = D_{in}\ (\frac{G_{VAL}}{2^n})$ Where: D_{in} is the signal input S_{out} is the signal Output G_{val} is the value in the register

Bit	Name	Active State		Function
Address offset 0				
7:0	TxIGainLSB	Data	RW	Least significant 8 bits of the TxIGain register (G_{val}).
Address offset 1				
2:0	TxIGainMSB	Data	RW	Most significant 3 bits of the TxIGain register (G_{val}).
7:3	NU			
Address offset 2				
7:0	TxQGainLSB	Data	RW	Least significant 8 bits of the TxQGain register (G_{val}).
Address offset 3				
2:0	TxQGainMSB	Data	RW	Most significant 3 bits of the TxQGain register (G_{val}).
7:3	NU			

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.25 TxIQOffset

Title	Transmit I & Q Channel Offset Correction register
Address	(mapped over 4 locations)
Function	RW
Description	This register controls the *Transmit Channel* data path signal offset. This offset value is a twos-complement value (N_{offset}t). This offset is applied to the channel data path signal after the Gain Multiplier (G_{val}), but before the DAC. The offset applied is at the discretion of the user, inappropriate values may cause arithmetic overflow in the subsequent operator sections. The resultant offset is given by the formula: $$D_{out} = D_{in}(\frac{Noffset}{2^n})$$ Where: D_{in} is the signal input D_{out} is the signal Output N_{offset} is the value in the register

Bit	Name	Active State		Function
Address offset 0				
7:0	TxIOffsetLSB	Data	RW	Least significant 8 bits of the TxIOffset register (N_{offset}).
Address offset 1				
3:0	TxIOffsetMSB	Data	RW	Most significant 4 bits of the TxIOffset register (N_{offset}).
7:4	NU			
Address offset 2				
7:0	TxQOffsetLSB	Data	RW	Least significant 8 bits of the TxQOffset register (N_{offset}).
Address offset 3				
3:0	TxQOffsetMSB	Data	RW	Most significant 4 bits of the TxQOffset register (N_{offset}).
7:4	NU			

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.26 TxPhase

Title	Transmit I and Q channel Phase Correction register
Address	(mapped over 4 locations)
Function	RW
Description	This register controls the *Transmit Channel* data path I & Q channel phase compensation. The phase may be adjusted by ±7.1° with respect to the input data signal phase. As each channel has separate phase adjustments the maximum differential phase compensation that can be achieved is ±14.2°. The phase adjustment value written to this register is a twos-complement value (N_{phase}).The amount of phase adjustment applied is given by the formula: $$\Phi = \tan^{-1}\left(\frac{N_{phase}}{2^{n}}\right)$$ Where: ϕ is the phase adjustment N_{phase} is the value in the register and has a range of -256 to +255.

Note: Although each channel is separately adjustable with it's own compensation value, the effect of phase adjustment is only detectable by measuring the phase angle between I and Q channels. It should be noted that the N_{phase} value has the effect of lagging the I channel for positive values of N_{phase} (conversely, leading the phase for negative values) and leading the I channel for positive values of N_{phase} (conversely, lagging the phase for negative values).

For example, putting the value 10 (decimal) into both TxIPhase and TxQPhase would produce a differential phase on I and Q of:

$$90^{\circ} - 2(\tan^{-1}(4.88\text{x}10^{-3})) = 89.44^{\circ}$$

Bit	Name	Active State		Function
Address offset 0				
7:0	TxIPhaseLSB	Data	RW	Least significant 8 bits of the TxIPhase register (nPhase).
Address offset 1				
0	TxIPhaseMSB	Data	RW	Most significant bit of the TxIPhase register (sign bit).
7:1	NU			
Address offset 2				
7:0	TxQPhaseLSB	Data	RW	Least significant 8 bits of the TxQPhase register (N_{phase}).
Address offset 3				
0	TxQPhaseMSB	Data	RW	Most significant bit of the TxQPhase register (sign bit).
7:1	NU			

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.27 TxDataAccess

Title	*Transmit Path* data access point.
Address	(mapped over 4 locations)
Function	RW
Description	This register block allows direct access to the *Transmit Path* data values just after the GPO block. Both read and write operations are permitted, a read operation reads the signal values on the I & Q channels. A write will write data to the data path just before the 15 tap filter. To prevent the Transmit Path overwriting this value the *RxDPAccessSel* bit should be set active. The MSB read data register is buffered to enable access to a discrete sample value (if this register was not buffered, data from different sample period could be in the MSB and LSB registers). Therefore the LSB register must be read first for correct operation.

Bit	Name	Active State		Function
Address offset 0				
7:0	TxDPIDataLSB	Data	RW	Least significant 8 bits of the TxDPIData register. This register must be read before its associated MSB register.
Address offset 1				
1:0	TxDPIDataMSB	Data	RW	Most significant bits of the TxDPIData register.
7:2	NU			
Address offset 2				
7:0	TxDPQDataLSB	Data	RW	Least significant 8 bits of the TxDPQData register. This register must be read before its associated MSB register.
Address offset 3				
1:0	TxDPQDataMSB	Data	RW	Most significant bits of the TxDPQData register.
7:2	NU			

3.6.28 RxIQGainMult

Title	Receive I & Q channel gain attenuation register
Address	(mapped over 2 locations)
Function	RW
Description	A twos-complement multiplication is performed on the *Receive Channel* data path signal values, the result is then re-normalized to the systems dynamic range. This register sets the multiplication value, the result of which may be considered as a digital attenuator. The result being given by the formula: $$S_{out} = D_{in} (\frac{G_{VAL}}{2^n})$$ Where: D_{in} is the signal input S_{out} is the signal Output G_{val} is the value in the register

Bit	Name	Active State		Function
Address offset 0				
7:0	RxIGain	Data	RW	8 bits of the RxIGain register (G_{val}).
Address offset 1				
2:0	RxIGain	Data	RW	8 bits of the RxIGain register (G_{val}).
Address offset 2				
7:0	RxQGain	Data	RW	8 bits of the RxQGain register (G_{val}).
Address offset 3				
2:0	RxQGain	Data	RW	8 bits of the RxQGain register (G_{val}).

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.6.29 RxDataAccess

Title	*Receive Path* data access point.
Address	(mapped over 4 locations)
Function	RW
Description	This register block allows direct access to the *Receive Path* data values just after the 59 tap (Rx anti-alias) filter. Both read and write operations are permitted, a read operation reads the signal values on the I & Q channels. A write operation will write data to the Data path operator output. To prevent the *Receive Path* overwriting this value the *RxDPAccessSel* bit should be set active. The MSB read data register is buffered to enable access of a discrete sample value (if this register was not buffered, data from different sample period could be in the MSB and LSB registers). Therefore the LSB register must be read first for correct operation.

Bit	Name	Active State		Function
Address offset 0				
7:0	RxDPIDataLSB	Data	RW	Least significant 8 bits of the RxDPIData register. This register must be read before its associated MSB register.
Address offset 1				
7:0	RxDPIDataMSB	Data	RW	Most significant 8 bits of the RxDPIData register.
Address offset 2				
7:0	RxDPQDataLSB	Data	RW	Least significant 8 bits of the RxDPQData register. This register must be read before its associated MSB register.
Address offset 3				
7:0	RxDPQDataMSB	Data	RW	Most significant 8 bits of the RxDPQData register.

4. Application TBD

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. Performance Specification

5.1 Electrical Performance

5.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
# Package			
Total Allowable Power Dissipation at T_{AMB} = 25°C		TBD	mW
Derating above 25°C		TBD	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

5.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	Typ.	Max.	Units
Supply (V_{DD} - V_{SS})	4.5		5.5	V
Operating Temperature	-40		+85	°C
MCLK Frequency				MHz

© 1997 MX•COM, INC
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480167.001

5.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.0V to 5.5V, T_{AMB} = 25°C
MCLK Frequency = 9.216MHz, Symbol Rate = 18k bits/sec

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (Tx powersaved)	1		TBD		mA
I_{DD} (Rx powersaved)	1		TBD		mA
I_{DD} (Aux powersaved)	1		TBD		mA
I_{DD} (Not powersaved)	1		TBD		mA
AC Parameters					
MCLK Input					
'High' pulse width	2	40			ns
'Low' pulse width	2	40			ns
Input impedance (at 100Hz)		10			MΩ

Notes:

1. Not including any current drawn from the device pins by external circuitry.
2. Timing for an external input to the MCLK pin.

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

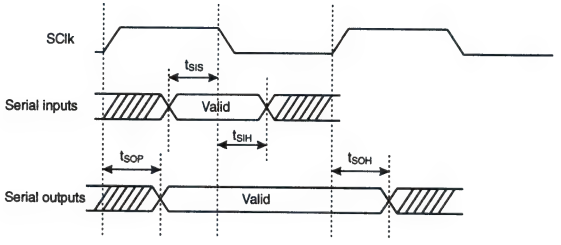
5.2 Timing

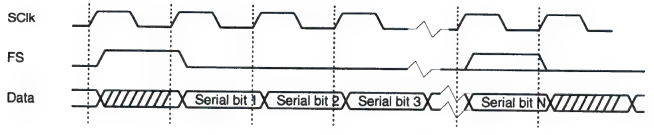
For the following conditions unless otherwise specified:

V_{DD} = 3.0V to 5.5V, T_{AMB} = 25°C, MCLK Frequency = 9.216MHz,

5.2.1 Serial Port

Timing Parameter	Marker	Min	Max	units
CmdDat setup to fall edge of SClk	t_{SIS}	TBD		ns
CmdFS setup to fall edge of SClk	t_{SIS}	TBD		ns
CmdDat hold from fall edge of SClk	t_{SIH}		TBD	ns
CmdFS hold from fall edge of SClk	t_{SIH}		TBD	ns
RxDat propagation from rising edge of SClk	t_{SOP}		TBD	ns
RxFS propagation from rising edge of SClk	t_{SOP}		TBD	ns
CmdRdDat propagation from rising edge of SClk	t_{SOP}		TBD	ns
CmdRdFS propagation from rising edge of SClk	t_{SOP}		TBD	ns
RxDat hold from rising edge of SClk	t_{SOH}	TBD		ns
RxFS hold from rising edge of SClk	t_{SOH}	TBD		ns
CmdRdDat hold from rising edge of SClk	t_{SOH}	TBD		ns
CmdRdFS hold from rising edge of SClk	t_{SOH}	TBD		ns
**** Cmd port in Bidirectional mode ****				
CmdDat propagation from rising edge of SClk	t_{SOP}		TBD	ns
CmdDat hold from rising edge of SClk	t_{SOH}	TBD		ns





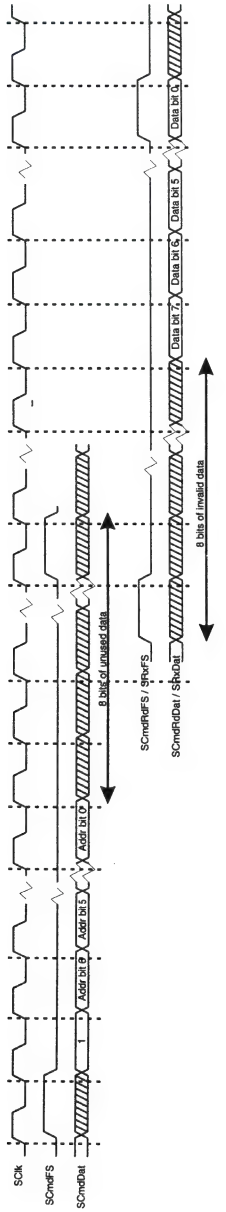
Basic serial port signals

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

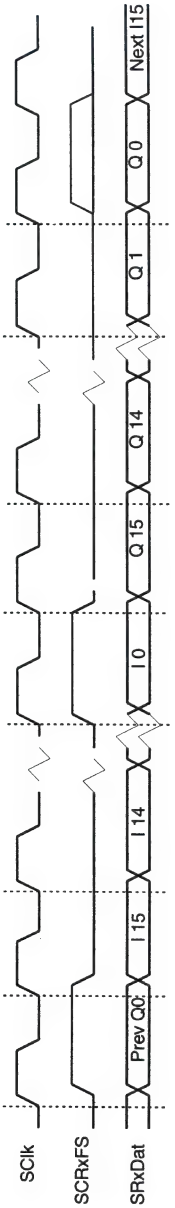
Command write operation

Bi-dir command read operation

© 1997 MX•COM, INC www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480167.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



Non bi-dir command read operation



RxData serial port read operation

© 1997 MX•COM, INC
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480167.001

5.3 Packaging TBD

© 1997 MX•COM, INC
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480167.001

Technical Specifications

Section 7:
Voice Security IC's

Device	Description	Page
MX014	Voice Band Inverter	3
MX128	Cordless Telephone Scrambler	15
MX224	Variable Split Band Inverter	25

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX014

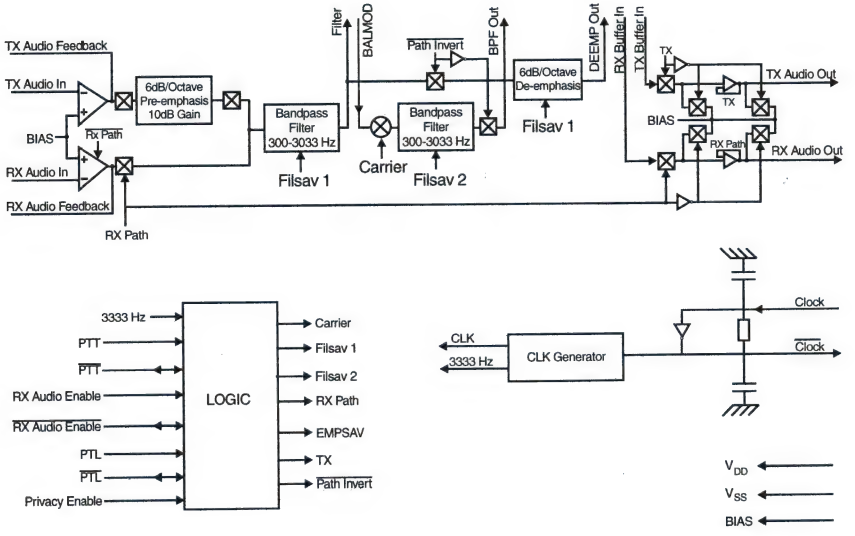
Voice Band Inverter

Features

- **CTCSS Compatible**
- **Fixed Frequency Inversion**
- **Low Power CMOS**

Applications

- **Land Mobile Radio Systems**
- **Community Repeaters**



The MX014 Voice Band Inverter gives the security of private voice communications to land mobile radio users, as well as to the users of other shared radio channel systems. Designed for use in half-duplex systems, the MX014 exchanges high and low frequencies in the voiceband and renders transmitted messages unintelligible. This privacy function is achieved by a single frequency inversion. When used with CTCSS, ***Pvt*SQUELCH**™ privacy adapter operation is achieved.

Sharp cut-off in the internal voiceband filters permits operation with CTCSS and similar sub-audio signaling schemes. This results in high quality recovered audio.

The core of the MX014 consists of two audio band pass filters and a balanced modulator. The device uses a programmable clock divider which controls the carrier and filter cut-off frequencies. Control of the RX/TX, PTL and privacy function is by pin selection.

The MX014 operates from a single 5V supply and uses a 4 MHz crystal oscillator to ensure the correct pitch in recovered speech. Signal coupling and decoupling are the only external components needed. The device is available in 24-pin PLCC (MX014LH), 24-pin PDIP (MX014P) and 24-pin CDIP (MX014J) packages.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480013.006
All trademarks and service marks are held by there respective companies.

CONTENTS

Section **Page**

1. Block Diagram **7-5**

2. Signal List **7-6**

3. External Components **7-7**

4. Application **7-8**

5. Performance Specification **7-10**

5.1 Electrical Performance 7-10

5.1.1 Absolute Maximum Ratings 7-10

5.1.2 Operating Limits 7-10

5.1.3 Operating Characteristics 7-10

5.2 Packaging 7-12

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480013.006
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

1. Block Diagram

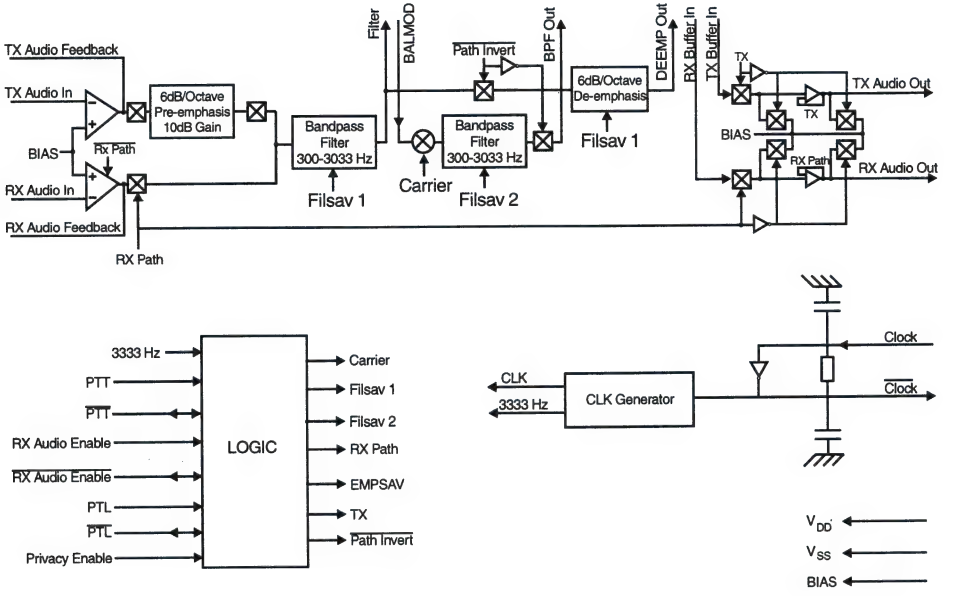


Figure 1: Device Block Diagram

© 1997 MX-COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480013.006
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

2. Signal List

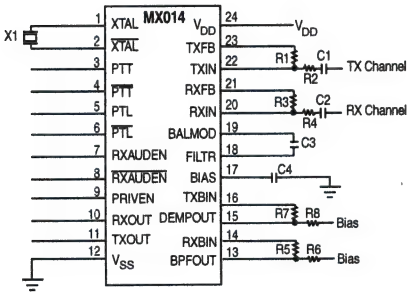
Pin No.	Name	Description
1	XTAL	An external 4MHz clock can be applied to this input. The clock circuit on chip has a resistor and capacitors so that only one external crystal is required.
2	$\overline{\text{XTAL}}$	This is the inverted 4MHz clock output for use when a crystal oscillator is used, or as a buffer for driving other clocked devices.
3	PTT	Push To Talk is an input with a 3MΩ pull-down resistor.
4	$\overline{\text{PTT}}$	This is the inverted PTT output. It has a 100kΩ output impedance.
5	PTL	Push To Listen is an input with a 3MΩ pull-down resistor.
6	$\overline{\text{PTL}}$	$\overline{\text{Push To Listen}}$ is the inverted output of PTL; it has a 100kΩ output impedance.
7	RXAUDEN	RX Audio Enable is an input with a 3MΩ pull-down resistor.
8	$\overline{\text{RXAUDEN}}$	$\overline{\text{RX Audio Enable}}$ is the inverted output of RX Audio Enable; it has a 100kΩ output impedance.
9	PRIVEN	Privacy Enable controls the input action of the balanced modulator by switching the carrier clock. When audio signals are inverted, the signal path gain is adjusted automatically to compensate for the upper sideband loss. It contains a 3MΩ pull-down resistor.
10	RXOUT	This is the receive audio output pin. It is biased at $V_{DD}/2$ when in the TX mode.
11	TXOUT	This is the "send" voice output pin. It is biased at $V_{DD}/2$ when in RX mode.
12	V_{SS}	The negative supply pin (ground).
13	BPFOUT	For a gain of one in the RX Output stage, these two pins are wire linked together. However, if gain is introduced at the RX input, attenuation may be introduced at the RX Output using these pins and two resistors.
14	RXBIN	
15	DEMPOUT	The pre-emphasis circuit has a 10dB gain at 1 kHz. Additional gain, or attenuation can be introduced as in the RX path.
16	TXBIN	
17	BIAS	This is the internally generated $V_{DD}/2$ decoupling pin.
18	FILTR	This filter is the output of the Input Audio BPF and must be a.c. coupled into the Balanced Modulator Input through a 0.1µF capacitor.
19	BALMOD	This is the input to the balanced modulator. It must be a.c. coupled to the Filter Output.
20	RXIN	This is a negative input of an op-amp at the input of the RX path. It can be used, along with RX Audio Feedback and two external resistors, to increase the signal to its optimum level prior to frequency inversion/filtering. This may improve the S/N.
21	RXFB	RX Audio Feedback is the output of an op-amp at the input of the RX path. See RXIN.
22	TXIN	The negative input of an op-amp at the input of the TX path. It can be used, along with TX Audio Feedback and two external resistors, to increase the signal to its optimum level prior to frequency inversion/filtering. This may improve S/N.
23	TXFB	TX Audio Feedback is the output of an op-amp at the input of the TX path. See TXIN.
24	V_{DD}	The positive supply pin.

Table 1: Signal List

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480013.006
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

3. External Components

Configuration for Radios with Existing Pre- and De-emphasis.



For Use in Radios without Pre- and De-emphasis.

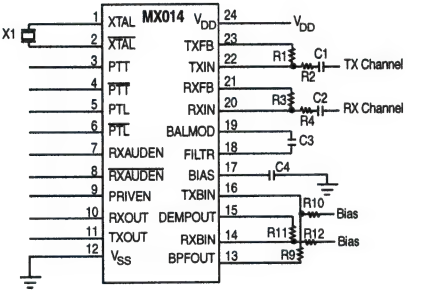


Figure 2: External Components Connections

$\text{TX Attenuation} = \frac{R8}{R7+R8}$	$\text{TX Attenuation} = \frac{R10}{R9+R10}$
For a gain of 1, $R8 = \infty$, $R7 = 0$	For a gain of 1, $R9 = 0$, $R10 = \infty$
$\text{RX Attenuation} = \frac{R6}{R5+R6}$	$\text{RX Attenuation} = \frac{R12}{R11+R12}$
For a gain of 1, $R6 = \infty$, $R5 = 0$	For a gain of 1, $R11 = 0$, $R12 = \infty$

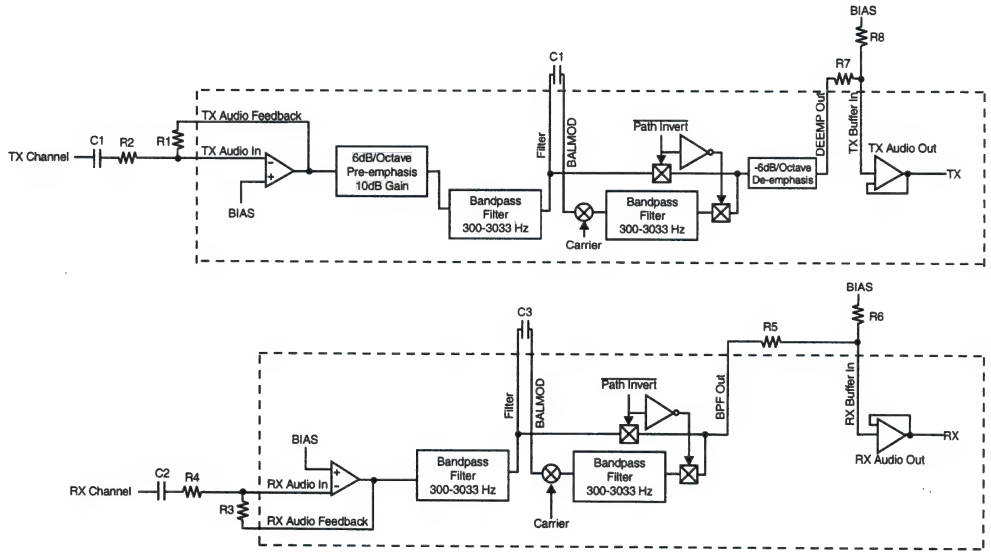
Table 2: Gain and Attentuation Calculations

Recommended External Component Notes:

1. Component Values: C1- C3 = 0.1 µF, C4 = 1.0 µF, X1 = 4 MHz crystal
2. R1 to R12 values will depend on the configuration and the gain or attenuation required. However R1, R3, R5, R7, and R11 should be 100 kΩ or greater. To add gain or attenuate, use R5-R12 as shown. See pin descriptions for more information.
3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of VDD, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480013.006
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

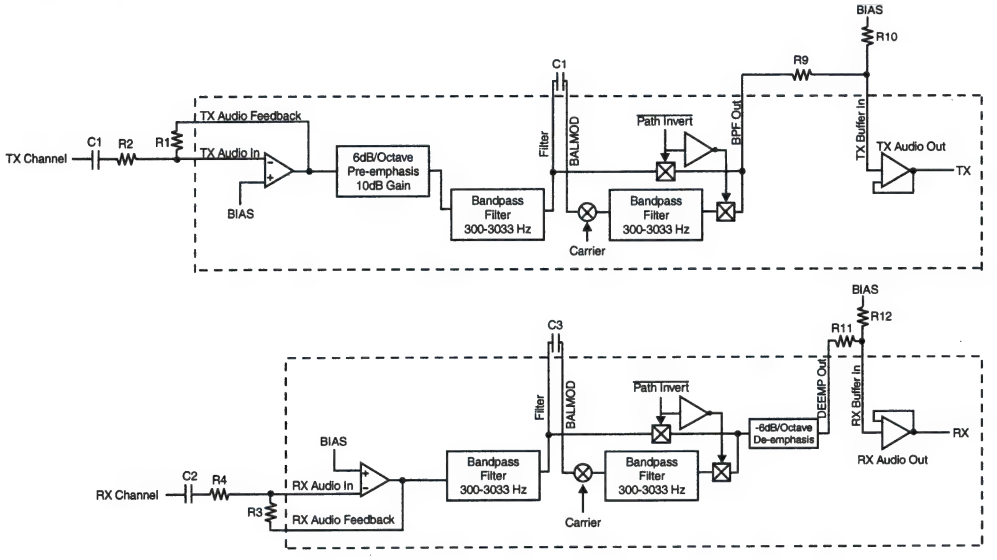
4. Application



Note: Dotted Lines contain on-chip functions

Figure 3: Voice Privacy Application (Add-on)

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480013.006
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.



Note: Dotted Lines contain on-chip functions

Figure 4: Voice Processing Application (OEM)

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480013.006
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

5. Performance Specification

5.1 Electrical Performance

5.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply Voltage	-0.3	7.0	V
Input Voltage at any pin			
(ref. V_{SS} + 0 V)	-0.3	(V_{DD} + 0.3)	V
Current:			
V_{DD}		30	mA
V_{SS}		30	mA
Any other pin		20	mA
J / P / LH Packages			
Maximum Device Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C
Operating Temperature Range:	-40	85	°C
Storage Temperature Range:	-55	125	°C

5.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	Typ.	Max.	Units
V_{DD}	4.5	5.0	5.5	V
Clock Frequency		4.0		MHz
Operating Temperature	-40		85	°C

5.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V at T_{AMB} = 25°C
Clock Frequency = 4.0MHz, 0dB reference = 300mV_{RMS} (Note: Measured at pin 18, the FILTR output. This pin must not exceed 300mV_{RMS} at 1kHz in Tx and 500mV_{RMS} at any frequency in Rx, or clipping may occur. The difference in levels is due to the pre-emphasis filter in the Tx path.

	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Current:					
RX/TX Operating (Private)				11.0	mA
RX/TX Operating (Clear)				8.0	mA
Standby	4			1.8	mA
Audio Input Impedance			10		MΩ
Audio Output Impedance	5		0.5		kΩ
Digital Output Impedance(Pulldown)		1			MΩ
Digital I/O Impedance			100		kΩ
Input Logic "1"		70%			V_{DD}
Input Logic "0"				30%	V_{DD}

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480013.006
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

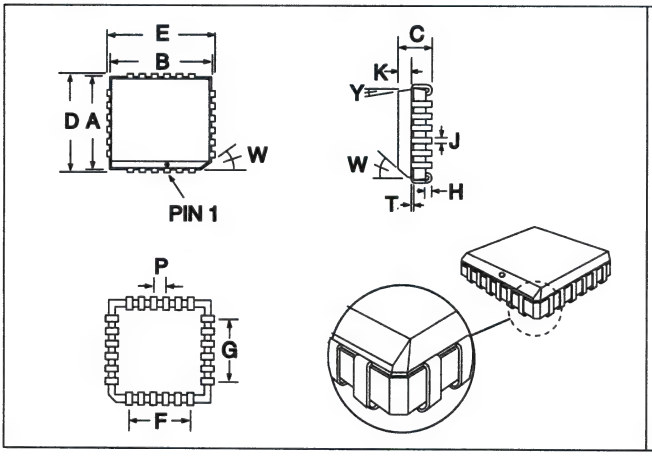
	Notes	Min.	Typ.	Max	Units
RX Clear Performance					
Total Harmonic Distortion	1		2	5	%
Output Noise Level	2		2		mV_{RMS}
Passband Gain			0		dB
Passband Ripple (300-3033 Hz)	1	-3		+2	dB
Stopband Attenuation					
(fin > 3333 Hz)			20		dB
(fin > 3633 Hz)			45		dB
(fin < 250 Hz)			42		dB
RX Inverted					
Total Harmonic Distortion	1,3		4		%
Output Noise Level	2,3		4		mV_{RMS}
Passband Ripple (300 - 3033 Hz)	3			4	dB
Stopband Attenuation					
(fin > 3333 Hz)			50		dB
(fin > 3633 Hz)			60		dB
Highpass Attenuation					
(fin < 250 Hz)			60		dB
TX Clear					
Total Harmonic Distortion	1		2	5	%
Output Noise Level	2		2		mV_{rms}
Passband Gain					
(fin = 300 - 3033 Hz)	1		0		dB
Passband ripple					
(fin = 300 - 3033 Hz)	1			4	dB
Stopband Attenuation					
(fin > 3333 Hz)	2		20		dB
(fin > 3633 Hz)			45		dB
(fin < 250 Hz)			42		dB
TX Inverted					
Total Harmonic Distortion	1,3		4		%
Output Noise Level	2		4		mV_{rms}
Passband Ripple					
(fin = 300 - 3333 Hz)	1,3			4	dB
Stopband Attenuation					
(fin > 3333 Hz)	3		50		dB
(fin > 3633 Hz)	3		60		dB
(fin < 250 Hz)	3		60		dB
Pre-Emphasis					
Frequency Response			6		dB/Octave
Gain at 1 kHz			10		dB
De-emphasis					
Frequency response			-6		dB/Octave
Gain at 1 kHz			0		dB

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480013.006
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Operating Characteristics Notes:

1. Input signal = 1kHz tone 0dB (300 mV_{RMS})
2. Input AC short circuit, audio path enabled. Measured in 30 kHz band
3. Due to frequency inversion (and pre- and de-emphasis), this refers to deviation from expected ideal response
4. Standby occurs in RX with RX Audio Enable = 0, RX Audio Enable = 1, and PTL = 1
5. TX Audio Out and RX Audio Out only

5.2 Packaging



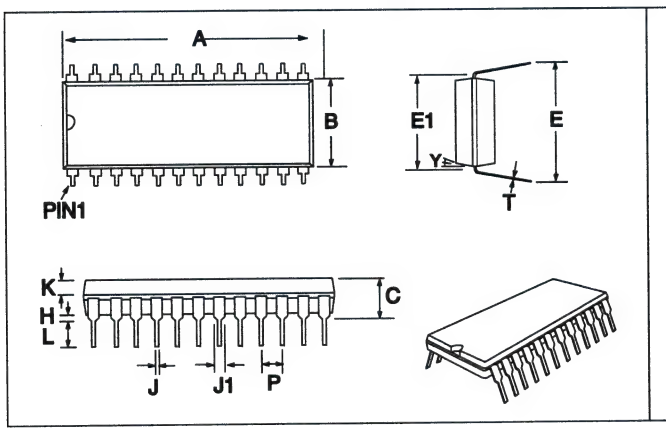
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 24-pin PLCC Mechanical Outline: Order as part no. MX014LH

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc. # 20480013.006

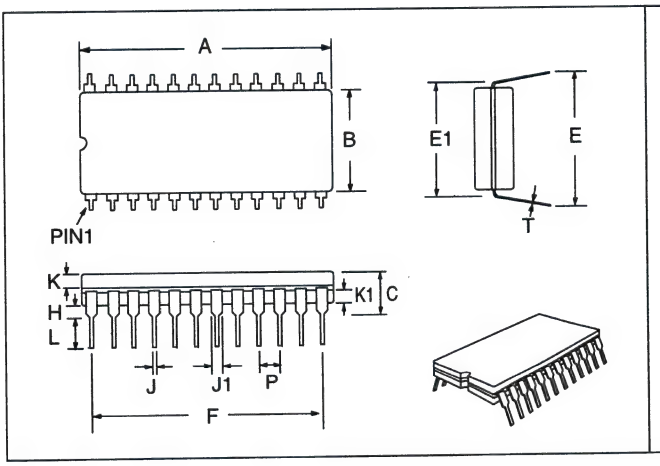


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin PDIP Mechanical Outline: Order as part no. MX014P



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 24-pin CDIP Mechanical Outline: Order as part no. MX014J

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc. # 20480013.006

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX128

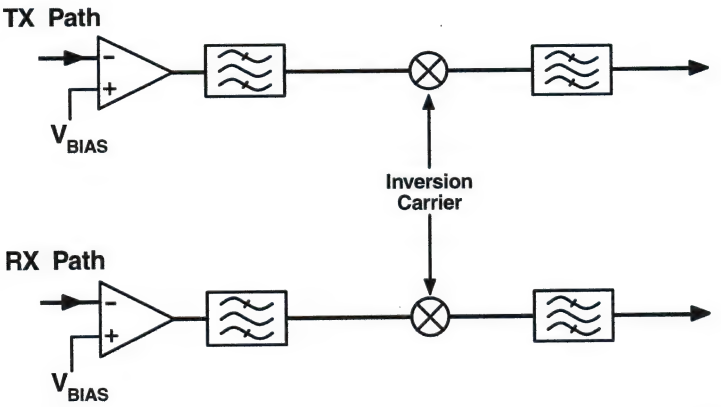
Cordless Telephone Scrambler

Features

- Full-Duplex Audio Processing
- On-Chip Filters
- Carrier Rejection >55dB
- Uses IF (10.24 MHz) Clock
- Requires No Extra Crystal
- Excellent Audio Quality
- Low Voltage 3.3V/5.0V Operation
- ECPA* Qualified Voice Protection

Applications

- Battery Powered Portability
- Cordless Telephones
- Wireless PBXs



The MX128 is a full-duplex frequency inversion scrambler designed to provide secure conversations for 46/49 MHz cordless telephone users. The RX and TX audio paths consist of the following:

1. A switched-capacitor balanced modulator with high baseband and carrier rejection.
2. A 3.3 kHz inversion carrier (injection tone).
3. A 3100 Hz lowpass filter.
4. Input op-amps with externally adjustable gain.

The MX128 uses mixed signal CMOS switched-capacitor filter technology and operates from a single supply in the range of 3.0V to 5.5V. The inversion carrier's frequency and filter switching clock are generated on-chip using an external 10.24 MHz or 3.58/3.6864 MHz crystal or clock input (selectable).

The MX128 is available in the following package styles: 16-pin SOIC (MX128DW) and 16-pin PDIP (MX128P).

*Electronics Communications Privacy Act (Title 18, US Code 2510 et seq.).

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480101.009
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.

CONTENTS

Section **Page**

1. Block Diagram **7-17**

2. Signal List **7-18**

3. External Components **7-19**

4. Application **7-20**

4.1 Application Notes 7-20

5. Performance Specification **7-21**

5.1 Electrical Performance 7-21

5.2 Packaging 7-24

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480101.009
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1. Block Diagram

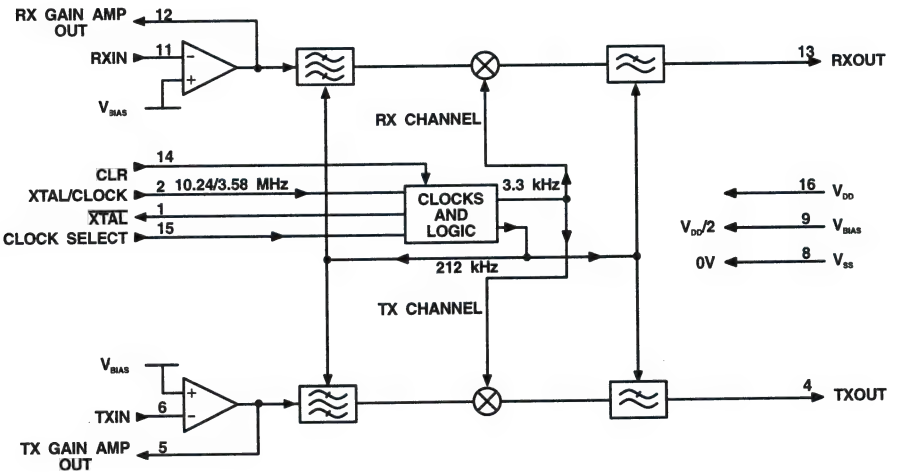


Figure 1: Device Block Diagram

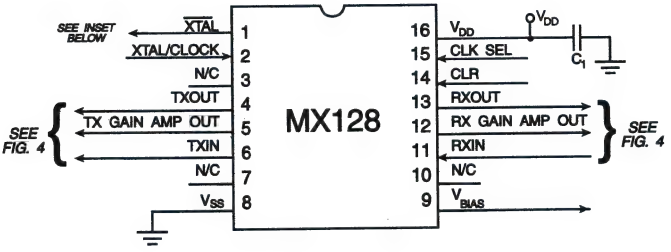
© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480101.009
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

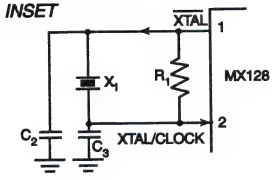
2. Signal List

Pin No.	Signal	Type	Description
1	$\overline{\text{Xtal}}$	output	This is the output of the clock oscillator inverter
2	Xtal/Clock	input	A 10.24 MHz, 3.58/3.6864 MHz, or an externally derived clock signal is injected at this pin. See Figure 3
4	TXOUT	output	This is the analog output of the transmit channel. It is internally biased at $V_{DD}/2$
5	TX Gain Ampout	output	This is the output pin of the transmit channel gain adjusting op-amp. See Figure 4 for gain setting components
6	TXIN	input	This is the analog signal input to the transmit channel. This input is to a gain adjusting op-amp whose gain is set by internal components. See Figure 4.
8	V_{SS}	power	Negative supply (GND)
9	V_{BIAS}	output	This is an internally generated bias voltage output ($V_{DD}/2$)
11	RXIN	input	This is the analog signal input to the receive channel. This input is to a gain adjusting op-amp whose gain is set by internal components. See Figure 4.
12	RX Gain Ampout	output	This is the output pin of the receive channel gain adjusting op-amp. See Figure 4 for gain setting components
13	RXOUT	output	This is the analog output of the receive channel. It is internally biased at $V_{DD}/2$
14	CLR		A logic 1 on this input selects the invert mode. A logic 0 selects the clear (not inverted) mode
15	Clock Select		Selects either 10.24 or 3.58/3.6864 MHz clock frequency. A logic "1" selects 10.24 MHz, and a logic "0" selects 3.58/3.6864 MHz. This input is internally pulled high
16	V_{DD}	power	Positive supply of 3.0V to 5.5 V
3, 7, 10	N/C		No internal connections

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480101.009
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components





10.24 MHz			
R1		1.0MΩ	±10%
C1		0.47µF	±20%
C2		22.0pF	±20%
C3		22.0pF	±20%
X1		10.24 MHz	

3.58/3.6864 MHz			
R1		1.0MΩ	±10%
C1		0.47µF	±20%
C2		33.0pF	±20%
C3		47.0pF	±20%
X1	Note 1	3.58/3.6864 MHz	

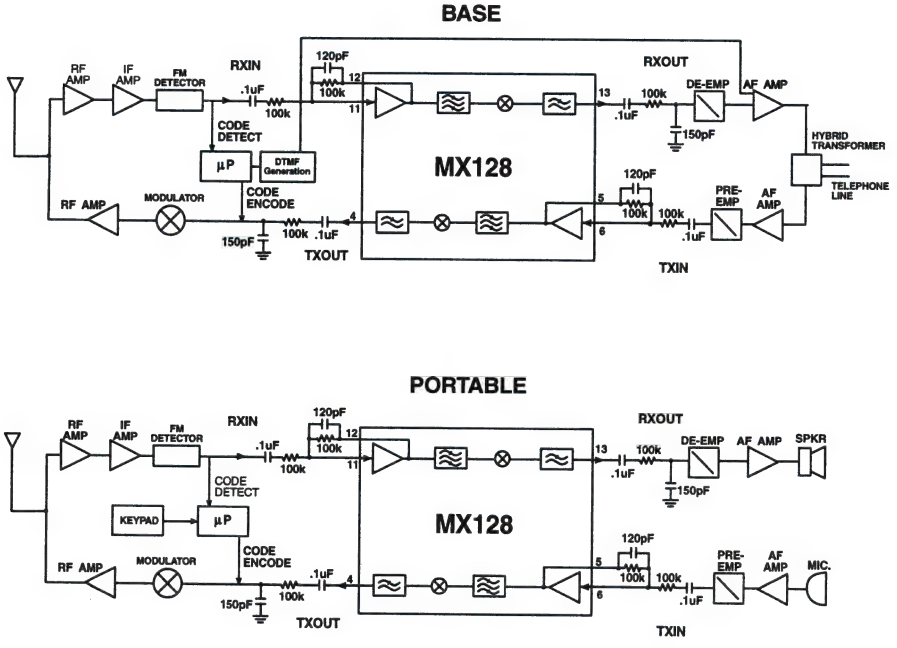
Figure 2: Recommended External Components

External Components Note:

1. For best results, a crystal oscillator should drive the clock inverter input with signal levels of at least 40% of V_{DD} peak - peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480101.009
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4. Application



Note: Components shown set a gain of 0dB.

Figure 3: Block Diagram of a Typical Application of the MX128 (Cordless Phone)

4.1 Application Notes

Formulas for calculating the carrier frequency, upper cutoff frequency and lower cutoff frequency with clock select pin high are as follows:

Carrier Frequency	=	(3.2995kHz / 10.24MHz) * XTAL frequency
Upper Cutoff Frequency	=	(2.800kHz / 10.24MHz) * XTAL frequency
Lower Cutoff Frequency	=	(400Hz / 10.24MHz) * XTAL frequency

Formulas for calculating the carrier frequency, upper cutoff frequency and lower cutoff frequency with clock select pin low are as follows:

Carrier Frequency	=	(3.2995kHz / 3.415MHz) * XTAL frequency
Upper Cutoff Frequency	=	(2.800kHz / 3.415MHz) * XTAL frequency
Lower Cutoff Frequency	=	(400Hz / 3.415MHz) * XTAL frequency

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480101.009
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. Performance Specification

5.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply Voltage (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pin	-20	20	mA
P/DW Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW max.
Derating above 25°C		10	mW/°C above 25°C
Operating Temperature	-40	85	°C
Storage Temperature	-55	125	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Clock Frequency			10.24	MHz

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480101.009
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.3V at T_{AMB} = 25°C
Clock Frequency = 10.24MHz
Audio Level 0dB ref. @ 1kHz = (V_{DD}-1) x 150mV_{RMS} e.g. V_{DD} = 3.3V 0dB = 345mV_{RMS}.

	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Current			2.0	3.0	mA
Input Impedance					
Digital	2	100			kΩ
Amplifiers	2	1.0	10.0		MΩ
Output Impedance (RXOUT, TXOUT)			1.0		kΩ
Input Logic 1 Voltage	1	70%			V_{DD}
Input Logic 0 Voltage	1			30%	V_{DD}
Dynamic Values					
Analog Signal Input Levels		-16.0		3	dB
Analog Output Noise	4		2.5	5.0	mV_{RMS}
Clear Mode					
Passband -3dB Cutoff Frequencies					
Low				300	Hz
High		3000			Hz
Passband Ripple (300-3000Hz)					
RX Channel		0		3.6	dB
TX Channel		0		2.9	dB
Passband Ripple (500-2750Hz)					
RX Channel		0		2.2	dB
TX Channel		0		2.0	dB
Filter Attenuation at 3.3 kHz					
RX Channel			30		dB
TX Channel			30		dB
Filter Attenuation at 3.6 kHz					
RX Channel			45		dB
TX Channel			45		dB
Passband Gain (@1kHz ref.)					
RX Channel		-1.5		0.5	dB
TX Channel		-1.5		0.5	dB
Switched-Capacitor Filter Sampling			211.066		kHz
Carrier Frequency			3298		Hz

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480101.009
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

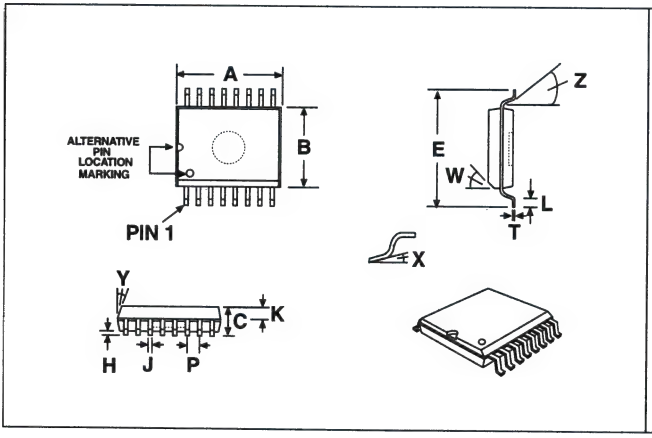
	Notes	Min.	Typ.	Max	Units
Invert Mode Combined TX and RX Response					
Passband -3dB Cutoff Frequencies					
Low				400	Hz
High		2800			Hz
Passband Gain		-3		0.5	dB
Distortion (@1kHz)	3		1.75	2.75	%
Passband Gain (@1kHz ref.)	5	-2.5	-1.5	0	dB
Low Frequency Roll-off (<200 Hz)		12			dB/octave
Invert Mode Single Channel Response					
Unwanted Modulation Products	3				
RX Channel			-40		dB
TX Channel			-40		dB
Carrier Breakthrough	3				
RX Channel			-55		dB
TX Channel			-55		dB
Baseband Breakthrough	3				
RX Channel			-40		dB
TX Channel			-40		dB

Operating Characteristics Notes:

1. Batch sampled only
2. By characterization only
3. Measured with Input Level 0dB
4. Short circuit RX or TX input, measure noise at corresponding analog output, in 30KHz bandwidth
5. Op Amp gain 0dB
6. Clear mode only

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480101.009
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.2 Packaging

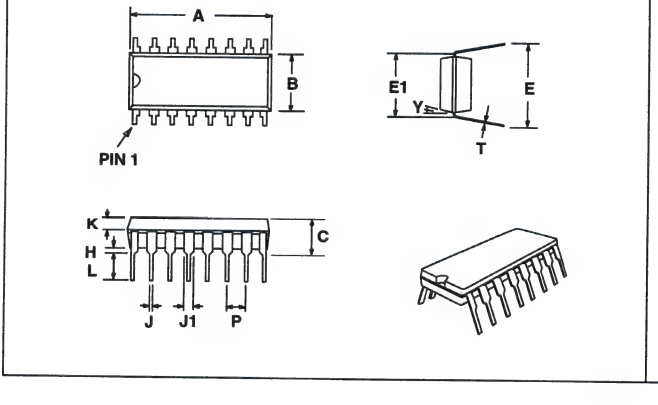


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 4: 16-pin SOIC Mechanical Outline: Order as part no. MX128DW



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 16-pin SOIC Mechanical Outline: Order as part no. MX128DW

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480101.009
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX214/224

Variable Split Band Inverter

VARIABLE SPLIT BAND INVERTER

FEATURES:

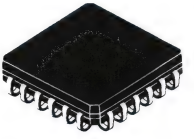
- CTCSS Highpass Filter
- Good Recovered Audio Quality
- Fixed and Rolling Code Modes
- Serial/Parallel Loading Options
- 32 Programmable Split Points
- Half-Duplex Capability

APPLICATIONS:

- Mobile Radio Voice Security
- Cellular Telephone Voice Security

MX214J (CDIP)
MX214P (PDIP)
22 pins

MX224J (CDIP)
MX224P (PDIP)
24 pins



MX214LH
MX224LH
(24p PLCC)

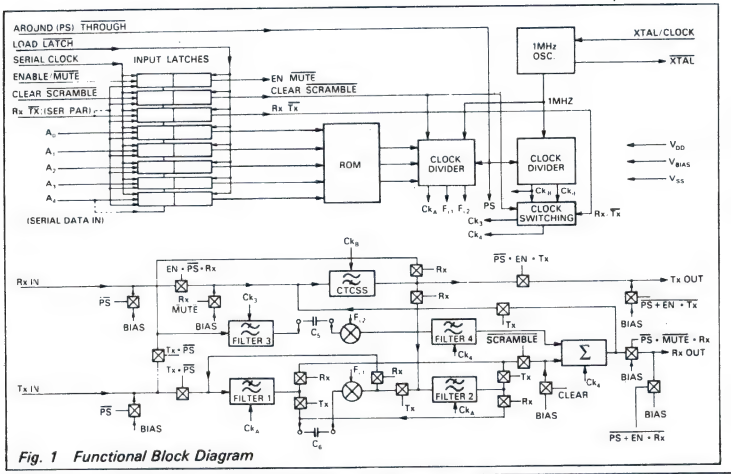


Fig. 1 Functional Block Diagram

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc. # 20480112.001

DESCRIPTION:

The MX214/MX224 Variable Split Band Inverters are designed for mobile and cellular radio voice security applications. Digital control functions are loaded serially into the MX214. The MX224 is loaded in parallel.

The MX214/MX224 ICs include a highpass filter which rejects subaudio frequencies, ensuring full CTCSS compatibility. This CTCSS filter is not included on the earlier-generation MX204 VSB Inverter.

The MX214/ MX224 splits the voiceband (300-2700 Hz) into upper and lower subbands, and inverts each subband about itself. The "split point" (defined as the frequency where the voice band is subdivided), is externally programmable to 32 distinct values in the 300 to 3000 Hz range. In the "fixed code" mode, a single split point is used. Fixed mode operation nets approximately 4 mutually exclusive voice channels.

In "rolling code" mode, the split point is changed many times per second, usually under control of a microprocessor. Rolling code scrambling requires synchronization, offers higher security than fixed code operation, and provides a much greater number of mutually exclusive secure channels.

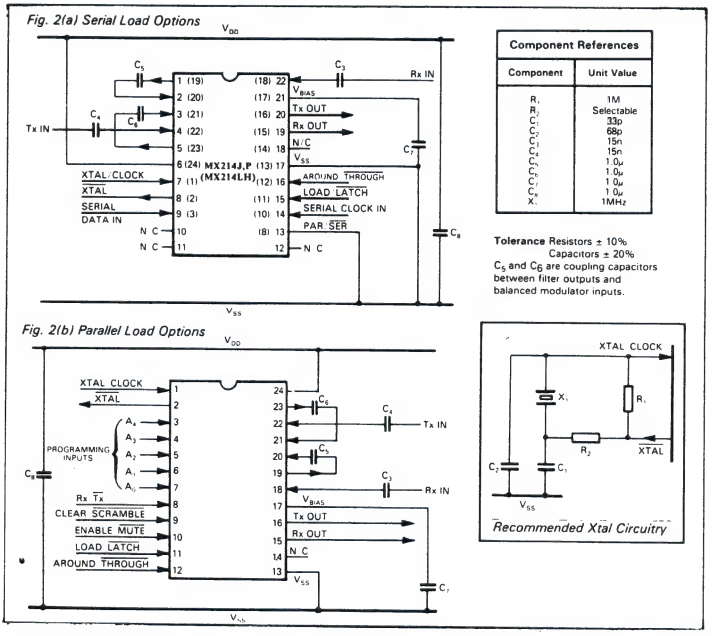
The MX214/224 offers a recovered audio product close to that of a telephone. The on-chip "Mute" function is useful when implementing rolling code continuous synchronization schemes. "Powersave" and "Clear/Scramble" controls are also included on-chip. Timing and filter clocks are derived internally from an on-chip 1 MHz reference oscillator driven by a 1 MHz crystal or clock pulse input.

APPLICATIONS INFORMATION:

Recommended external component connections are shown in Figure 2. In "Scramble" mode, split point frequencies are selected and set in accordance with the ROM address code present at the inputs A_0 to A_4(see Table 2). In "Clear" mode, both the Upper and Lowerband filter limits are used (see Figures 5 or 6), the carrier frequencies are turned off, and the balanced modulators are bypassed internally. The Low Band audio is removed from the output signal prior to summing.

The MUTE function disables the MX214/224's audio outputs to allow periodic transmission of synchronization data. A logic "0" at this input isolates the device while leaving the audio input and output pins at bias level (see Table 1). When the MX214/224 is in POWERSAVE mode, audio signals may be hardwired around the device since the input and output pins are open circuit (see Table 1).

Component Connections



© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Doc. # 20480112.001

MX214/224 PIN FUNCTION TABLE

PIN NUMBER				FUNCTION
214 J,P	224 J,P	214 LH	224 LH	
7	1	1	1	**Xtal/Clock:** Input to the clock oscillator inverter. A 1 MHz xtal input or externally derived 1 MHz clock is injected here.
8	2	2	2	**$\overline{\text{Xtal}}$:** Output of the clock oscillator inverter.
9	—	3	—	**Serial Data Input:** This pin is used to input an 8-bit word representing the digital control functions. This word is loaded using the serial data clock and is input in the following sequence: MUTE, CLEAR, Rx/$\overline{\text{Tx}}$, A_0, A_1, A_2, A_3, A_4. The load/$\overline{\text{latch}}$ pin is operated on completion. Reference the timing diagram in Figure 7.
—	—	—	3	A_4 ┐ **Programming Inputs:** In parallel mode, these five digital inputs define the
—	—	—	4	A_3 ┤ split point frequency. Each of the 5 input pins have a 1MΩ internal pullup
—	5	—	5	A_2 ┤ resistor. See Table 2 for programming information.
—	6	—	6	A_1 ┤
—	7	—	7	A_0 ┘
—	8	—	8	**Rx/$\overline{\text{Tx}}$:** This digital input selects the Receive or Transmit paths and configures upperband and lowerband filter bandwidths while setting the CTCSS highpass filter position on the signal path. See Table 1 and Figures 5 and 6. 1MΩ internal pullup resistor (Rx).
13	—	8	—	**Parallel/$\overline{\text{Serial}}$:** This pin must be connected to V_{ss} for serial loading. Internal 1MΩ pullup resistor.
—	9	—	9	**Clear/$\overline{\text{Scramble}}$:** This digital input puts the device into "Clear" or "Scramble" mode by controlling the application of carrier frequency to the Upper and Lower band balanced modulators. In "Scramble" mode, the balanced modulator carrier frequency values are selected by the split point address A_0-A_4 (Table2). In "Clear" mode, the carriers are disabled and the balanced modulators are bypassed internally, i.e. the lower band signal is not added to the output signal. 1MΩ internal pullout resistor (Clear).
—	10	—	10	**Enable/$\overline{\text{Mute}}$:** This digital function is used to disable Receive or Transmit signal paths for rolling code synchronization while maintaining bias conditions. Synchronization data can be transmitted during the Mute periods, as is done in the MX1204 VSB Scrambler module. Internal 1MΩ pullup resistor (Enable).
14	—	10	—	**Serial Clock Input:** This is the externally applied data clock frequency used to shift input data along on devices wired in the Serial loading mode. One full data clock cycle is required to shift one data bit completely into the register. See Timing Diagram (Figure 7). 1MΩ internal pullup resistor.
15	11	11	11	**Load/$\overline{\text{Latch}}$:** This pin controls the loading of the 8 digital function inputs (ENABLE, CLEAR, Rx/Tx, A_0-A_4) into the internal register. When this pin is at logic "1," all eight inputs are transparent and new data acts directly. For controlled changing of parameters in the parallel mode, Load/$\overline{\text{Latch}}$ must be kept at logic "0" while a new function is loaded, then strobed 0-1-0 to latch the inputs in. For serial loading, the serial data should be loaded with Load/$\overline{\text{Latch}}$ at logic "0" and then Load $\overline{\text{Latch}}$ strobed 0-1-0 on completion of data loading. Internal 1MΩ pullup resistor (Load). See Figure 7.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480112.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

MX214/224 PIN FUNCTION TABLE

PIN NUMBER				FUNCTION
214 J,P	224 J,P	214 LH	224 LH	
16	12	12	12	**Powersave:** This digital input is used to place the MX214/224 into Powersave mode, where all parts of the device except for the 1 MHz oscillator are shut down. All signal input and output lines are made open circuit, free of all bias. This allows signal paths to be routed externally around the device, while reducing current consumption. A logic "0" at this input enables the device to work normally as shown in Table 1. Internal 1MΩ pullup resistor.
17	13	13	13	**V_{SS}:** Negative Supply (GND).
18	14	14	14	**Internal Connection:** This pin is internally connected. Leave open circuit.
19	15	15	15	**Rx Output:** This is the processed received audio signal output. This pin is held at a DC "bias" voltage for all functions except Powersave. This buffered output is driven by the Summing circuit in the Rx mode. Signal paths and bias levels are detailed in Table 1 and Figure 6.
20	16	16	16	**Tx Output:** This is the processed audio output for the transmission channel. This pin is held at a DC "bias" for all functions except Powersave. This summed and buffered signal is passed through the CTCSS High Pass Filter to the output pin in the Tx mode. Signal paths and bias levels are detailed in Table 1 and Figure 5.
21	17	17	17	**V_{BIAS}:** Normally at $V_{DD}/2$, this pin requires an external decoupling capacitor (C_7) to V_{SS}.
22	18	18	18	**Rx Input:** This is the analog received audio signal input. This pin is held at a DC "bias" voltage by a 300 Kohm on-chip bias resistor which is selected for all functions except Powersave. It must be connected to external circuitry by capacitor C_3 (See Figure 2). This input is routed through the CTCSS High Pass Filter in Rx mode to remove subaudio frequencies from the voiceband. Signal paths and bias levels are detailed in Table 1 and Figure 6.
1	19	19	19	**Highband Filter Output:** The output of the Input Filter of the Upperband limit. The Rx/$\overline{Tx}$ function sets the lowpass filter at 3400 Hz or 2700 Hz respectively. This output must be connected to the Highband Balanced Modulator input via capacitor C_5 (See Figure 2).
2	20	20	20	**Highband Balanced Modulator Input:** The input to the Balanced Modulator of the Upperband limit. This input must be connected to the Highband Filter Output via capacitor C_5 (See Figure 2).
3	21	21	21	**Lowband Balanced Modulator Input:** The input to the Balanced Modulator of the Lowerband limit. This input must be connected to the Lowband Filter Output via capacitor C_6 (See Figure 2).
4	22	22	22	**Tx Input:** This is the analog "Clear" audio input for the VSB scrambler. This pin is held at a DC "bias" voltage by a 300 Kohm on-chip bias resistor, which is selected for all functions except Powersave. It must be connected to external circuitry by capacitor C_4 (See Figure 2). This input, in the Tx mode, is connected to Upper and Lowerband input filters. Signal paths and bias levels are detailed in Table 1 and Figure 5.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480112.001
All trademarks and service marks are held by there respective companies.

MX214/224 PIN FUNCTION TABLE

PIN NUMBER				FUNCTION
214 J,P	224 J,P	214 LH	224 LH	
5	23	23	23	**Lowband Filter Output:** The output of the Input Filter of the Lowerband limit. The Rx/$\overline{Tx}$ function determines which filter is used (Filter 1 or 2). See figures 5 and 6. This output must be connected to the Lowband Balanced Modulator Input via capacitor C_6 (See Figure 2).
6	24	24	24	V_{DD}: A single + 5V supply is required.

Note: Pins 10, 11, and 12 on the MX214J and MX214P are not connected. Pins 4, 5, 6, 7 and 9 on the MX214LH are not connected.

MX214/224 TRUTH TABLE

	Rx/$\overline{Tx}$ = 1	Rx/$\overline{Tx}$ = 0	$\overline{MUTE}$ = 0	POWERSAVE
Rx Path	Enabled	Disabled	Disabled	Disabled
Rx Out Level	Bias	Bias	Bias	High Impedance
Tx Path	Disabled	Enabled	Disabled	Disabled
Tx Out Level	Bias	Bias	Bias	High Impedance

TABLE 1 FUNCTIONS INFLUENCING SIGNAL PATHS

APPLICATIONS INFORMATION

The term "MX214" can be taken to mean MX214 or MX224.

Audio Quality

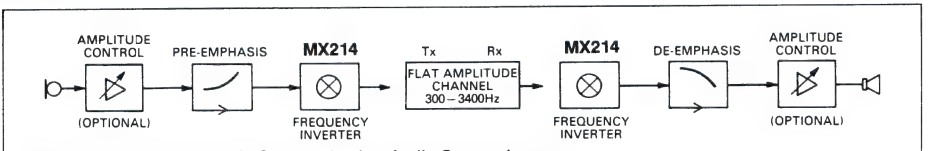


Fig. 3 Recommended Basic Communication Audio System Layout

Figure 3 shows the recommended basic audio system layout using added pre- and deemphasis circuitry to maintain good recovered speech quality. In the Transmit mode, *Do Not* preemphasise the audio output of the MX214. In the Receive mode, deemphasis should be used after the MX214.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480112.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

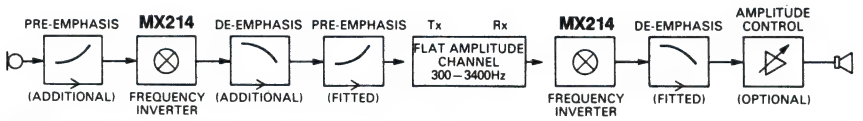


Fig. 4 Recommended Basic Radio Communication Audio System Layout

Figure 4 shows the recommended basic audio system layout if it is necessary to install the MX214 within a radio having pre- and deemphasis circuitry as a standard. This is where post-emphasis access is not possible in the transmitter.

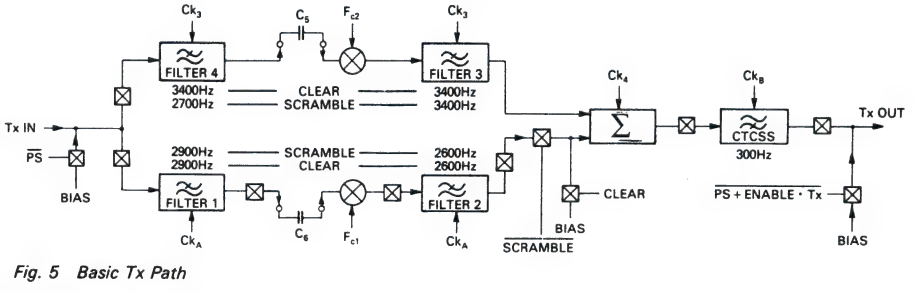


Fig. 5 Basic Tx Path

During the Transmit function the Low Pass and CTCSS filters are configured automatically as shown in Figure 5, with cut-off frequencies (-3dB) indicated.

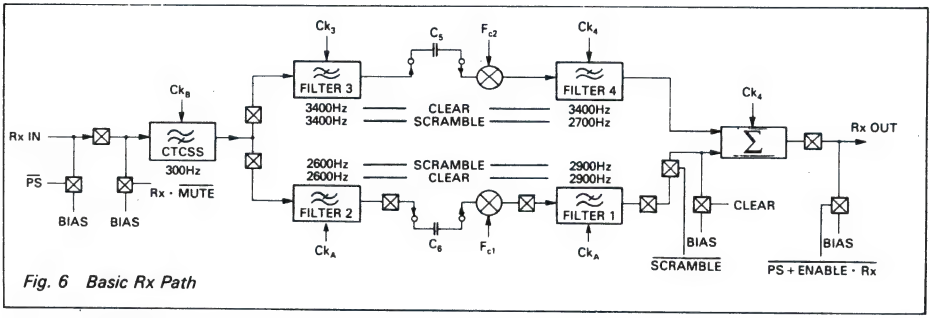


Fig. 6 Basic Rx Path

During the Receive function the Low Pass and CTCSS filters are configured automatically as shown in Figure 6, with cut-off frequencies (-3dB) indicated.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480112.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

MX214/224 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref. V_{ss} = 0V)		−0.3V to (V_{DD} + 0.3V)
Sink/source current (supply pins)		±30mA
(other pins)		±20mA
Total device dissipation @ 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	MX214J/224J	−30°C + 85 °C (Ceramic)
	MX214P/214LH/224P/224LH	−30°C + 70°C (Plastic)
Storage temperature range:	MX214J/224J	−55°C to + 125° (Ceramic)
	MX214P/214LH/224P/224LH	−40° to + 85°C (Plastic)

Operating Limits:

All characteristics measured using the following parameters unless otherwise specified:

V_{DD} = 5.0V, T_{amb} = 25°C, F_{clk} = 1.0MHz, Audio Level Ref: 0dB = 775 mVrms.

Characteristics	See Note	Min	Typ	Max	Unit
Static Values					
Supply Voltage		4.5	5	5.5	V
Supply Current (Enabled)		—	8	—	mA
Supply Current (Powersave)		—	1.2	—	mA
Analog Input Impedances					
Tx/Input (Enabled)		—	100	—	kΩ
Tx/Rx Input (Powersave)		1	—	—	MΩ
Balanced Modulator		—	40	—	kΩ
Analog Output Impedances					
Rx Output (Tx Mode)		—	100	—	kΩ
Rx Output (Rx Mode)		—	—	2	kΩ
Rx Output (Powersave)		1	—	—	MΩ
Tx Output (Tx Mode)		—	—	2	kΩ
Tx Output (Rx Mode)		—	100	—	kΩ
Tx Output (Powersave)		1	—	—	MΩ
Input LPF		—	—	1	kΩ
Digital Values					
Digital Input Impedance		100	—	—	kΩ
Dynamic Values					
Input Logic '1'		3.5	—	—	V
Input Logic '0'		—	—	1.5	V
Xtal/Clock Frequency		—	1	—	MHz
Analog Input Level		−18	—	+6	dB
Carrier Breakthrough	1	—	−55	—	dB
Baseband Breakthrough	1, 2 or 3	—	−33	—	dB
Filter Clock Breakthrough	1, 2, or 3	—	−50	—	dB
Output Noise	1, 4	—	−45	—	dB

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480112.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

MX214/224 ELECTRICAL SPECIFICATIONS (cont.)

Characteristics	See Note	Min	Typ	Max	Unit
Passband Characteristics					
Clear Mode	7				
Passband Gain		—	0	—	dB
Output Lower 3dB Point (Rx or Tx)		—	300	—	Hz
Output Upper 3dB Point (Rx or Tx)		—	3400	—	Hz
Scramble-Descramble	5				
Received Signal Passband Gain	6	—	0	—	dB
Received Signal Lower 3dB Point		—	400	—	Hz
Received Signal Upper 3dB Point		—	2700	—	Hz
Transmitted Signal Lower 3dB Point		—	300	—	Hz
Transmitted Signal Upper 3dB Point		—	3400	—	Hz
CTCSS (Highpass Filter)					
−3dB Point		—	300	—	Hz
Passband Gain		—	0	—	dB
Stopband Attenuation at f < 250 Hz		—	40	—	dB
Timing *(Figure 7)*					
Serial Mode Enable Set Up (t_{SMS})		250	—	—	ns
Serial Clock 'High' Pulse Width (t_{PWH})		250	—	—	ns
Serial Clock 'Low' Pulse Width (t_{PWL})		250	—	—	ns
Data Set Up Time (t_{DS})		150	—	—	ns
Data Hold Time (t_{DHS})		50	—	—	ns
Load/$\overline{\text{Latch}}$ Set Up Time (t_{LL})		250	—	—	ns
Load/$\overline{\text{Latch}}$ Pulse Width (t_{LLW})		150	—	—	ns
Data Set Up Time(t_{DSP})		150	—	—	ns
Data Hold Time (t_{DHP})		20	—	—	ns

Notes: *1. Measured at the output of a single device.*
2. Tx Mode.
3. Rx Mode.
4. With input A.C. short-circuited to V_{ss}.
5. Measured at the output of a receiving device in a scrambler-descrambler system with a transmission channel having a flat amplitude response and a bandwidth of 300Hz to 3400 Hz and measured relative to the input signal at the transmitting device.
6. Excluding split point ± 150 Hz.
7. Measured at the Rx or Tx output pin of a single device.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc. # 20480112.001

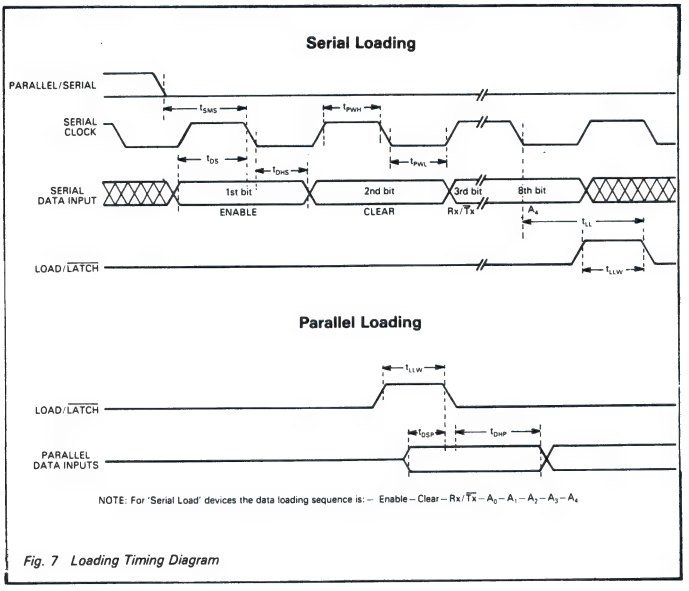


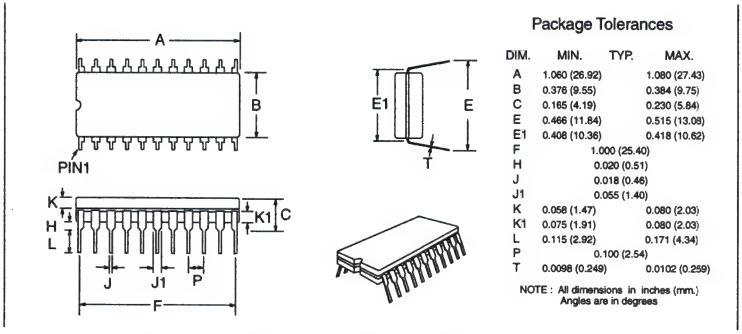
Fig. 7 Loading Timing Diagram

ROM Address A_4–A_0	Split Point Hz	Low Band Carrier, Hz f_{c_1}	High Band Carrier, Hz f_{c_2}	ROM Address A_4–A_0	Split Point Hz	Low Band Carrier, Hz f_{c_1}	High Band Carrier, Hz f_{c_2}
00000	2800	3105	6172	10000	1135	1436	4504
00001	2625	2923	6024	10001	1050	1351	4424
00010	2470	2777	5813	10010	976	1278	4347
00011	2333	2631	5681	10011	913	1213	4310
00100	2210	2512	5555	10100	857	1157	4273
00101	2100	2403	5494	10101	792	1094	4166
00110	2000	2304	5376	10110	736	1037	4132
00111	1909	2212	5263	10111	688	988	4065
01000	1826	2127	5208	11000	636	936	4032
01001	1750	2049	5102	11001	591	891	3968
01010	1680	1984	5050	11010	552	853	3937
01011	1555	1858	4950	11011	512	813	3906
01100	1448	1748	4807	11100	471	772	3846
01101	1354	1655	4716	11101	428	728	3816
01110	1272	1572	4629	11110	388	688	3787
01111	1200	1501	4587	11111	350	650	3731

Table 2 ROM Address Programming Table

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480112.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

Packaging

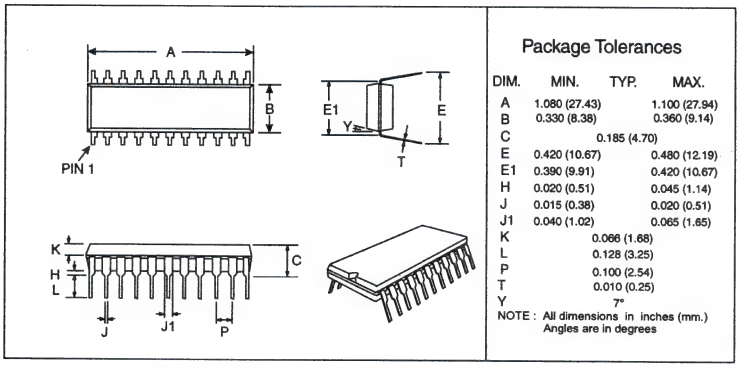


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.060 (26.92)		1.080 (27.43)
B	0.376 (9.55)		0.384 (9.75)
C	0.165 (4.19)		0.230 (5.84)
E	0.466 (11.84)		0.515 (13.08)
E1	0.408 (10.36)		0.418 (10.62)
F		1.000 (25.40)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.40)	
K	0.058 (1.47)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 22-pin CDIP Mechanical Outline: order as part no. MX214P

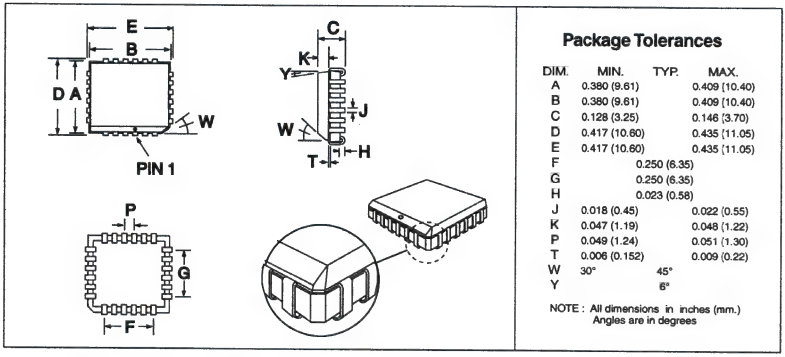


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.080 (27.43)		1.100 (27.94)
B	0.330 (8.38)		0.360 (9.14)
C		0.185 (4.70)	
E	0.420 (10.67)		0.480 (12.19)
E1	0.390 (9.91)		0.420 (10.67)
H	0.020 (0.51)		0.045 (1.14)
J	0.015 (0.38)		0.020 (0.51)
J1	0.040 (1.02)		0.065 (1.65)
K		0.066 (1.68)	
L		0.128 (3.25)	
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 22-pin PDIP Mechanical Outline: order as part no. MX214P



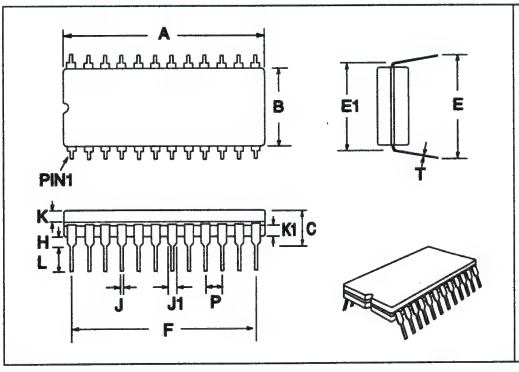
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 10: 24-pin PLCC Mechanical Outline: order as part no. MX214LH

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480112.001
All trademarks and service marks are held by there respective companies.

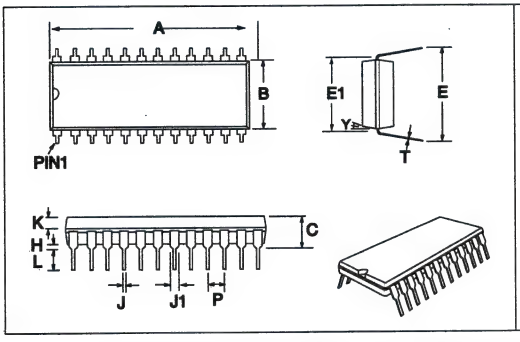


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.240 (31.50)		1.260 (32.00)
B	0.514 (13.06)		0.583 (14.79)
C	0.165 (4.19)		0.230 (5.84)
E	0.600 (15.23)		0.670 (17.00)
E1	0.594 (15.09)		0.615 (15.61)
F		1.100 (27.94)	
H		0.02 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.074 (1.88)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.10 (2.54)	
T	0.0094 (0.239)		0.0106 (0.269)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 24-pin CDIP Mechanical Outline: order as part no. MX224J

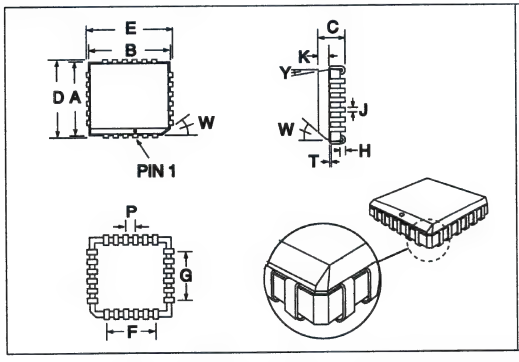


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 12: 24-pin PDIP Mechanical Outline: order as part no. MX224P



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 13: 24-pin PLCC Mechanical Outline: order as part no. MX224LJ

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc. # 20480112.001

Technical Specifications

Section 8: Cellular IC's

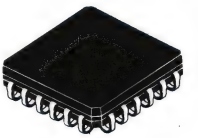
Device	Description	Page
MX316	NMT Audio Filter Array	3
MX826	AMPS/NAMPS System Audio Processor	9

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX316 NMT Audio Filter Array

MX316J (CDIP)
MX316P (PDIP)
16 pins



MX316LH
(24p PLCC)

FEATURES:

- **12th Order Lowpass Filter for S.A.T.* Rejection**
- **4 KHz S.A.T. Recovery Bandpass Filter**
- **Low Group Delay Distortion**
- **Single 5V CMOS Power Requirement**

APPLICATIONS:

- **Nordic Mobile Telephone (NMT) 450/900 MHz Mobile and Base Specifications**

DESCRIPTION:

The MX316 is a low power CMOS switched capacitor filter array designed to meet Nordic Mobile Telephone base and mobile specifications. As depicted in Figure 1, the device is comprised of:

1) a 12th order, 3.4 KHz lowpass filter which meets NMT 450 and 900 MHz base and mobile filter response specifications. Group delay distortion is minimized through this filter.
2) a 6th order, 4 KHz narrow bandpass filter which meets NMT 450 and 900 MHz S.A.T. recovery specifications.
3) an uncommitted amplifier, which may be used for a variety of applications, such as pre-emphasis, de-emphasis, and buffering.

An on-chip oscillator is driven by a 1 MHz crystal and provides all reference clocks for the switched capacitor filters via a divider chain. Alternatively, an external clock may be used. In standby mode, the chip enable feature is used to disable the three circuit elements.

*Supervisory Audio Tone

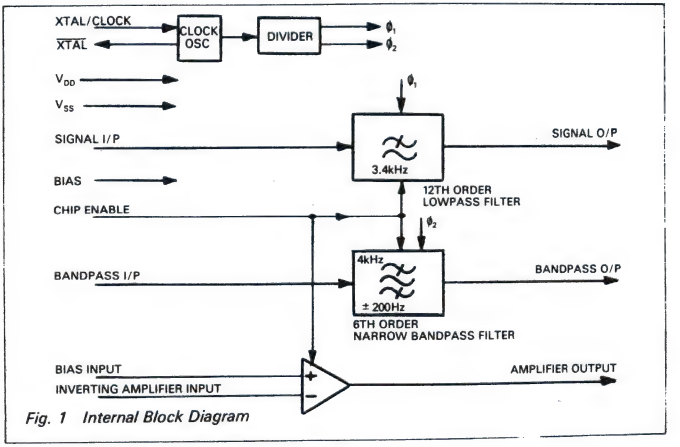


Fig. 1 Internal Block Diagram

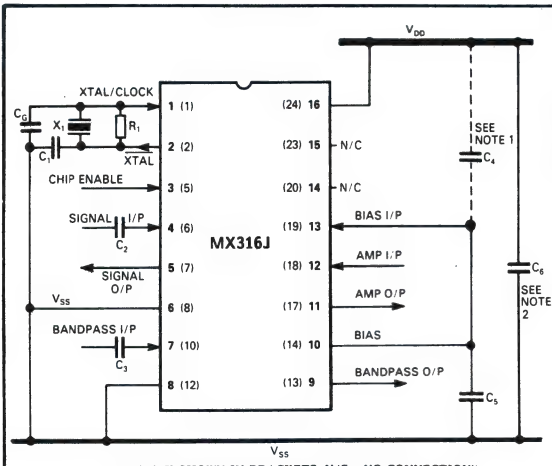
© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480166.001
All trademarks and service marks are held by there respective companies.

MX316 PIN FUNCTION TABLE

PIN		FUNCTION	DESCRIPTION
MX316J MX316P	MX316LH		
1	1	**Xtal/Clock**	Connect 1 MHz crystal or externally derived clock to this input. Drives the on-chip inverting oscillator.
2	2	**$\overline{\text{Xtal}}$**	1 MHz crystal O/P. Inverting output of on-chip oscillator.
3	5	**Chip Enable**	Internally pulled to V_{dd}. A logic "0" applied to this pin will disable all filters and the uncommitted amplifier (powersave).
4	6	**Signal I/P**	Input to the lowpass filter. This input is internally biased and externally a.c. coupled by C2.
5	7	**Signal O/P**	Lowpass filter output internally biased to $V_{dd}/2$.
6	8	**V_{ss}**	Negative supply voltage
7	10	**BP I/P**	Input to bandpass filter. Internally biased and externally a.c. coupled by C3.
8	12	**V_{ss}**	Negative supply voltage
9	13	**BP O/P**	Bandpass filter output. Internally biased to $V_{dd}/2$.
10	14	**Bias**	$V_{dd}/2$ Bias Pin. Externally decoupled by C5 (see fig. 2, note 1).
11	17	**Amp O/P**	Uncommitted amplifier output
12	18	**Amp I/P**	Uncommitted amplifier inverting input
13	19	**Bias I/P**	Connect externally to "Bias" pin.
14	20	**N/C**	Internally connected. Leave open circuit.
15	23	**N/C**	Internally connected. Leave open circuit.
16	24	**V_{dd}**	Positive supply voltage

Note: MX316LH pin numbers 3,4,9,11,15,16,21, and 22 are not connected.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc. # 20480166.001



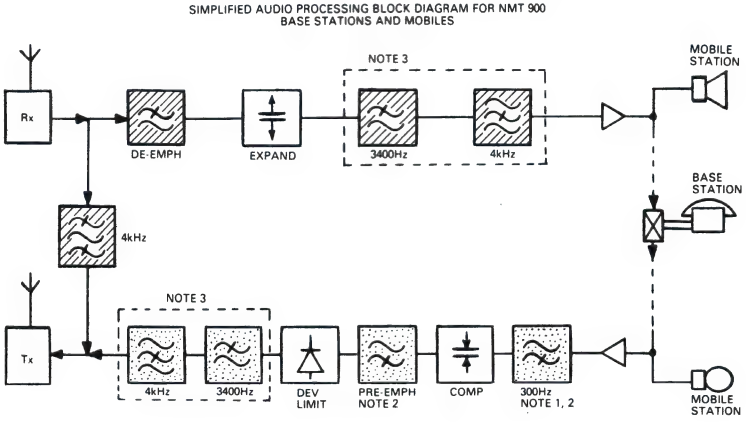
Component References

Component	Typical Unit Value	
R_1	1M	10%
C_1	33p	20%
C_2	0.1µ	20%
C_3	0.1µ	20%
C_4	0.1µ	20%
C_5	0.1µ Min.	20%
C_6	0.1µ	20%
C_G	68p	20%
X_1	1MHz	

NOTES:

1. *Bias may be decoupled to V_{SS} and V_{DD} using C_4, C_5 when input signals are referenced to the bias pin. For input signals referenced to V_{SS}, decouple Bias to V_{SS} using C_5 only.*
2. *Use C_6 when input signals are referenced to V_{SS}, to decouple V_{DD}.*

Fig. 2 External Component Connections



NOTES:

1). Not required in base station.
2). Pre-emph and highpass filter may be constructed using on-chip amplifier.
3). MX316 Lowpass Filter achieves both these functions.

MX316 (DEVICE A) MX316 (DEVICE B) BASE STATION ONLY

FIG. 3: MX316 TYPICAL APPLICATION

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480166.001
All trademarks and service marks are held by there respective companies.

MX316 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	MX316J	−30°C to +85°C
	MX316LH, MX316P	−30°C to +70°C
Storage temperature range:	MX316J	−55°C to +125°C
	MX316LH, MX316P	−40°C to +85°C
Maximum device dissipation:		All versions 100mW

Operating Limits

All characteristics measured using the following parameters unless otherwise specified:
V_{DD} = 5V, T_{amb} = 25°C, ∅ = 1MHz, $\Delta f_{\varnothing}$ = 0, f_{in} = 1kHz.

Characteristics		See Note	Min	Typ	Max	Unit
Static Characteristics						
Supply voltage			4.5	5	5.5	V
Supply current (Enabled)			—	6.0		mA
Supply current (Disabled)			—	700		µA
Input impedance (Filters & Amplifier)			100	1000	—	kΩ
Output impedance (Filters)			—	3	—	kΩ
Output impedance (Amplifier open loop)			—	800	—	Ω
Output impedance (Amplifier closed loop)			—	6	—	Ω
Input logic '1'			3.5	—	—	V
Input logic '0'			—	—	1.5	V
Dynamic Characteristics						
Passband Ripple	(300-3000Hz) LP	5	—	—	2	dB
	(4kHz ± 55Hz) BP	5	—	—	2	dB
Cut off frequency	(−3dB) LP	4,5	3000	3450	3800	Hz
	(−6dB) BP	4,5	4200	—	3800	Hz
Attenuation	(3800-4200Hz) LP	4,5	36	46	—	dB
	(<2000Hz,>6000Hz) BP	4,5	35	37	—	dB
Group Delay Distortion	(900-2100Hz) LP		—	80	—	µs
	(600-3000Hz) LP		—	450	—	µs
Output Noise (rms)	LP	1	—	1.6	—	mV
	BP	1	—	1	—	mV
Signal Input (rms)	LP	2	—	0.4	1.0	V
	BP	2	—	0.4	1.0	V
Insertion loss (1kHz)	LP		—	0	—	dB
(4kHz)	BP		—	0	—	dB
Aliasing Frequency			50	—	—	kHz
Inverting Amplifier						
Open loop gain		3	—	30	—	dB
Gain bandwidth product			—	1	—	MHz

Note: *1. Measured with input a.c. s/c.*
2. 'MAX' figure specified for nominal 3% distortion (30dB SINAD).
'TYP' figure specified for minimum distortion (MAX SINAD).
3. Relative to 1kHz. 100mV rms input level.
4. Refer to Figs. 4 and 5.
5. Specified over the full operating voltage and temperature range.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480166.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

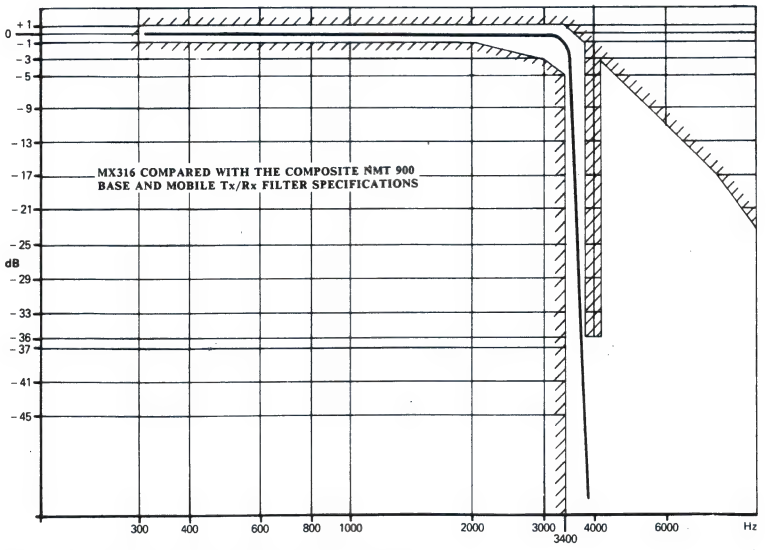


FIG. 4: TYPICAL MX316 LOWPASS FILTER RESPONSE

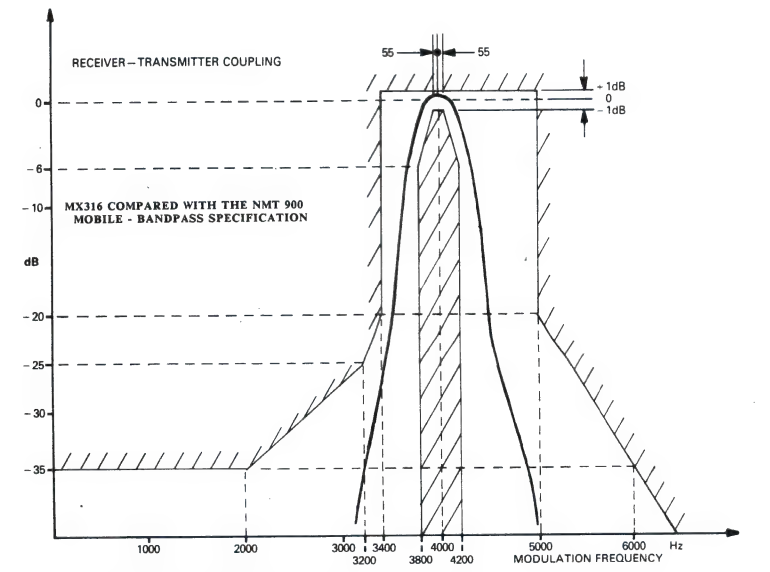
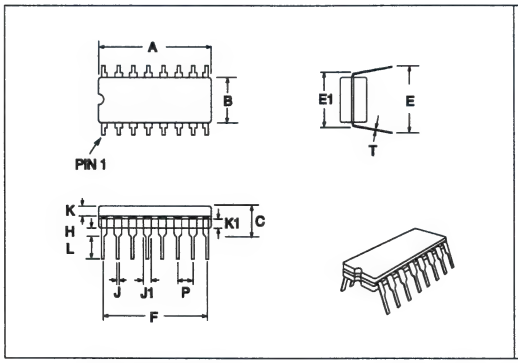


FIG.5: TYPICAL MX316 4kHz BANDPASS FILTER RESPONSE

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by there respective companies.
Doc. # 20480166.001

Packaging

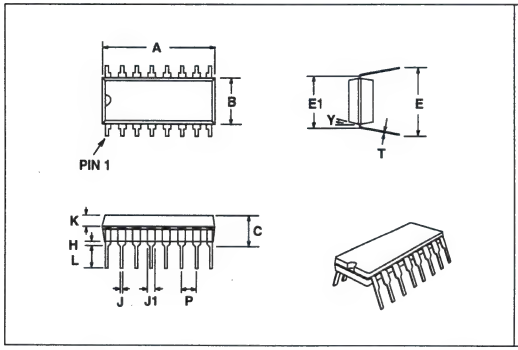


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.753 (19.13)		0.767 (19.48)
B	0.285 (7.24)		0.291 (7.39)
C	0.165 (4.19)		0.230 (5.84)
E	0.370 (9.40)		0.415 (10.53)
E1	0.300 (7.61)		0.317 (8.04)
F		0.70 (17.78)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.053 (1.33)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin CDIP Mechanical Outline: order as part no. MX316P

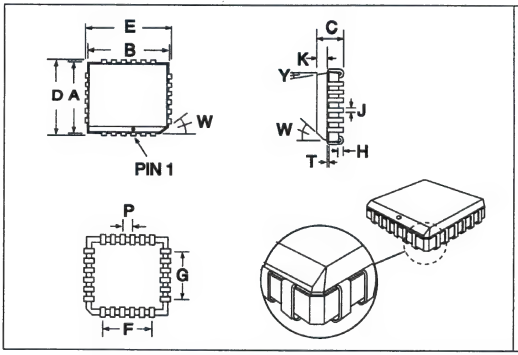


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 16-pin PDIP Mechanical Outline: order as part no. MX316P



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin PLCC Mechanical Outline: order as part no. MX316LH

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480166.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by there respective companies.

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX826 AMPS/NAMPS SYSTEM AUDIO PROCESSOR

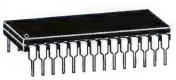
C-BUS COMPATIBLE

PRELIMINARY INFORMATION

Features

- **Full-Duplex Audio Processing for AMPS/ NAMPS Cellular Systems**
- **On-Chip Speech and SAT Capabilities**
  – TX/RX Filtering & Gain – SAT Channel Pre-/De-Emphasis – Deviation Limiter
- **Serial µProcessor Interface**
- **"Sidetone" Output Available**
- **Access to External Processes**
  – Companding – Signaling – VSR Codec (Store/Play)
- **HandsFree Compatibility**
- **Powersave (Low-Current) Settings**

MX826DW
28-pin SOIC



MX826J
28-pin CDIP

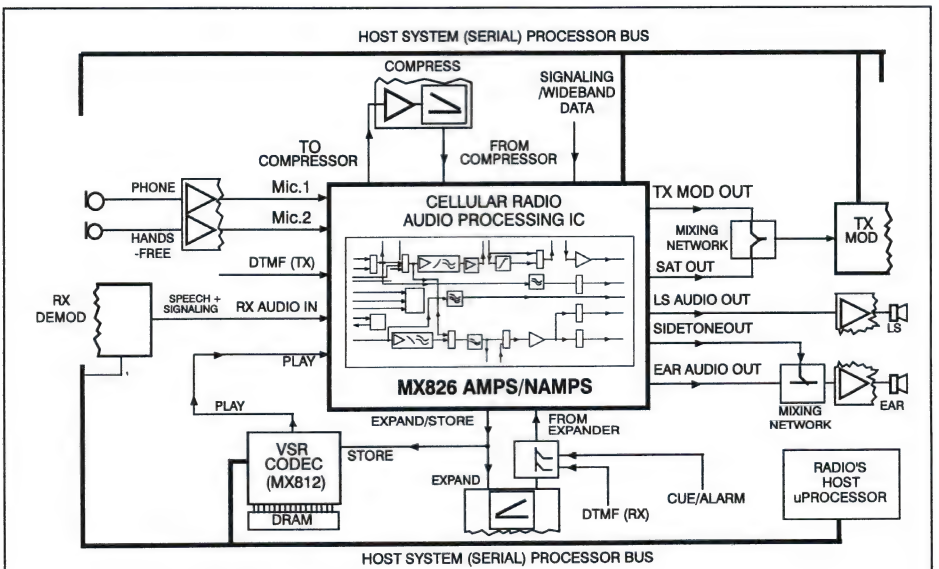


Figure1 - The MX826 AMPS/NAMPS Audio Processor Installed in a Cellular System

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480070.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Description

The MX826 is a µProcessor controlled full-duplex audio processor on a single-chip with separate TX and RX paths to provide all the filter/gain/limiting functions necessary to pre-process audio, wideband-data and SAT cellular communications systems using the AMPS/NAMPS or TACS/ETACS/JTACS specifications.

Selectable inputs available to the transmit path are: a choice of two microphones and DTMF/signaling, with access, in this path, to external compression circuitry. Operationally the TX path provides input gain/filtering, a deviation limiter and TX Modulation Drive controls.

In the RX path the SAT signal is separated from the incoming audio via a filter block and made available at a separate pin for mixing externally with the TX Modulation Drive.

The RX path consists of an input gain/filter block for voice, inputs from an external audio expansion system and an output gain control driving either a loudspeaker system or earpiece.

Unique to the MX816/826/836 cellular audio processors is the ability to route audio (TX or RX) to an external Voice Store and Retrieve (VSR) device such as the MX802 or MX812 thus providing the radio system with a voice answering and announcement facility using external DRAM.

As a member of the DBS800 family, the MX826 follows C-BUS protocol. (C-BUS is the serial interface used by all DBS800 integrated circuits.)

The MX826, a low-power CMOS device which reduces the amount of microcircuits and components required in a cellular audio system by providing more functions on a single chip, is available in 28-pin SOIC and CDIP packages.

Pin	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	**Xtal/Clock:** The input to the on-chip clock oscillator. A Xtal or externally derived clock (f_{XTAL}) should be connected here. Note that operation of the MX826 without a suitable Xtal or clock input may cause device damage. See Figure 2 (notes).
3	**Serial Clock:** The "C-BUS" serial data clock input. This clock, produced by the µController, is used for transfer timing of commands and data to the MX826. See Timing Diagrams.
4	**Command Data:** The "C-BUS" serial data input from the µController. Data is loaded to the MX826 in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the Serial Clock. See Timing Diagrams.
5	**Chip Select ($\overline{\text{CS}}$):** The "C-BUS" data loading control function. This input is provided by the µController. Data transfer sequences are initiated, completed or aborted by this signal. See Timing Diagrams.
6	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS}. See Figure 2.
7	**Rx Audio In:** Normally taken from the radio's discriminator output, this input has a 1MΩ internal resistor to V_{BIAS} and requires to be connected via a capacitor.
8	**Expand/Store:** A common output that can be used as either an input to an external audio expander or the input to a voice storage medium such as the MX812. Components relevant to the external device requirements should be used at this output. See Figures 2 and 3.
9	**(Expanded) Audio In:** The audio input, via SW5, from an external expander or audio mixing function. This input has a 1MΩ internal resistor to V_{BIAS} and requires to be connected via a capacitor. See Figures 2 and 3.
10	**TX Mod Out:** The composite TX audio output to the transmitter modulator from a variable attenuation stage (11_H). This output is set to V_{BIAS} via an internal 1MΩ resistor when set to Powersave or OFF.
11	**LS Audio Out:** An audio output of the Rx path (or selected audios, see Figure 3) for a loudspeaker system. This is available for handsfree operation. This output can be connected to V_{BIAS} when not required, by SW6 (Configuration Command (10_H)). A driver amplifier may be required.
	Notes on Inputs: *To minimize aliasing effects, lowpass filtering may be required at the inputs to this device (especially those supplied from switched-capacitor-type devices) to ensure the input spectrum is kept below 63kHz.*

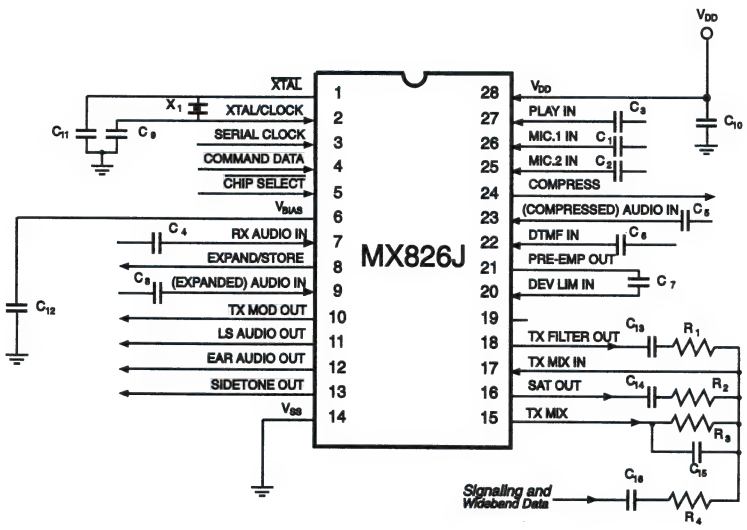
© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480070.004

Pin	Function
12	**Ear Audio Out:** An audio output of the Rx path (or selected audios), available as an output for a handset earpiece. This output, in parallel with the LS Audio Out function, can be connected to V_{BIAS} when not required, by SW7 (Configuration Command (10_H)). A driver amplifier may be required.
13	**Sidetone:** A switched "sidetone" from the microphone inputs made available for mixing externally with the "Ear" audio. See Figure 3.
14	**V_{SS}:** Negative supply rail. Signal ground.
15	**TX Mix:** The output of the TX Mix Amplifier. Used with external components, it allows the TX Filter Out output to mix with externally generated signalling tones prior to the final level adjustment.
16	**SAT Out:** The output of the SAT Bandpass filter. This level is recovered from the input RX audio and is available for mixing externally with the transmitter modulation. See Figure 3.
17	**TX Mix In:** The input to the TX Mix Amplifier. Used with external components, it allows the TX Filter Out output to mix with externally generated signalling tones prior to the final level adjustment. The recovered SAT signal may be introduced at this point. See Figures 2 and 3.
18	**TX Filter Out:** The output of the Deviation Limiter/Lowpass Filter stage. This stage can be by-passed using SW3 (Configuration Command). See Figure 3.
19	No internal connection – Leave open circuit.
20	**Deviation Limiter In:** Input to the on-chip deviation limiter. This input should be a.c. coupled to the Pre-Emphasis Out pin. The a.c. coupling will achieve maximum possible symmetry of limiting as this input has a 1MΩ internal resistor to V_{BIAS}. See Figure 2.
21	**Pre-Emphasis Out:** Audio output from the TX Gain/Pre-Emphasis function. This output should be a.c. coupled to the Deviation Limiter In pin. See Figures 2 & 3.
22	**DTMF In:** To introduce DTMF type audio, at a suitable level for transmission, to the TX Path, controlled by SW2 (Configuration Command (10_H)). This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
23	**Compression In:** The audio input from an external compression system. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
24	**Compression:** The output to an external audio compression system. Currently available compressor/ expanders have Op-Amps incorporated. The compressor can be by-passed by SW2.
25	**Mic.2 In:** TX voice (Mic.) inputs, selectable by SW1 available for handsfree mic./handset mic. or any TX audio input. Pre-amplification may be required at these inputs. These inputs
26	**Mic.1 In:** each have an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
27	**Play In:** The input via SW2 from a voice storage device such as the MX812. This "replayed" audio can be sent to RX or TX paths allowing a Messaging/Voice Notepad/Answering facility. This input has an internal 1MΩ resistor to V_{BIAS} and should be connected via a capacitor.
28	**V_{DD}:** Positive supply rail. A single +5-volt power supply is required. Levels and voltages within this Audio Processor are dependent upon this supply.

***C-BUS** is MX-COM's proprietary standard for the transmission of commands and data between a µController and the relevant Cellular microcircuits. It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions embodied into many types of µController. The "C-BUS" data rate is determined solely by the µController.*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480070.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Application Information



R_1	= 100kΩ	C_3	= 100nF	C_8	= 100nF	C_{13}	= 100nF
R_2	as required	C_4	100nF	C_9	33pF	C_{14}	100nF
R_3	100kΩ	C_5	100nF	C_{10}	100nF	C_{15}	100pF
R_4	as required	C_6	100nF	C_{11}	33pF	C_{16}	100nF
C_1	100nF	C_7	100nF	C_{12}	1.0µF	X_1	4.000MHz
C_2	100nF						

Tolerances – Capacitors ±20%

Figure 2 - Recommended External Components

Notes

1. **Xtal/clock operation**
   Operation of any MX-COM IC without a Xtal or clock input may cause device damage. To minimize damage in the event of a Xtal/drive failure, you should install a current limiting device (resistor or fast-reaction fuse) on the power input (V_{DD}).

2. **SAT Output**
   It is possible, due to the impedance of this output, that an external buffer amplifier will be required when interfacing or mixing with other cellular system sections.

3. **TX Mix Gain**
   The value of R_4 should be chosen with R_3/C_{15} in order to provide the required gain.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480070.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

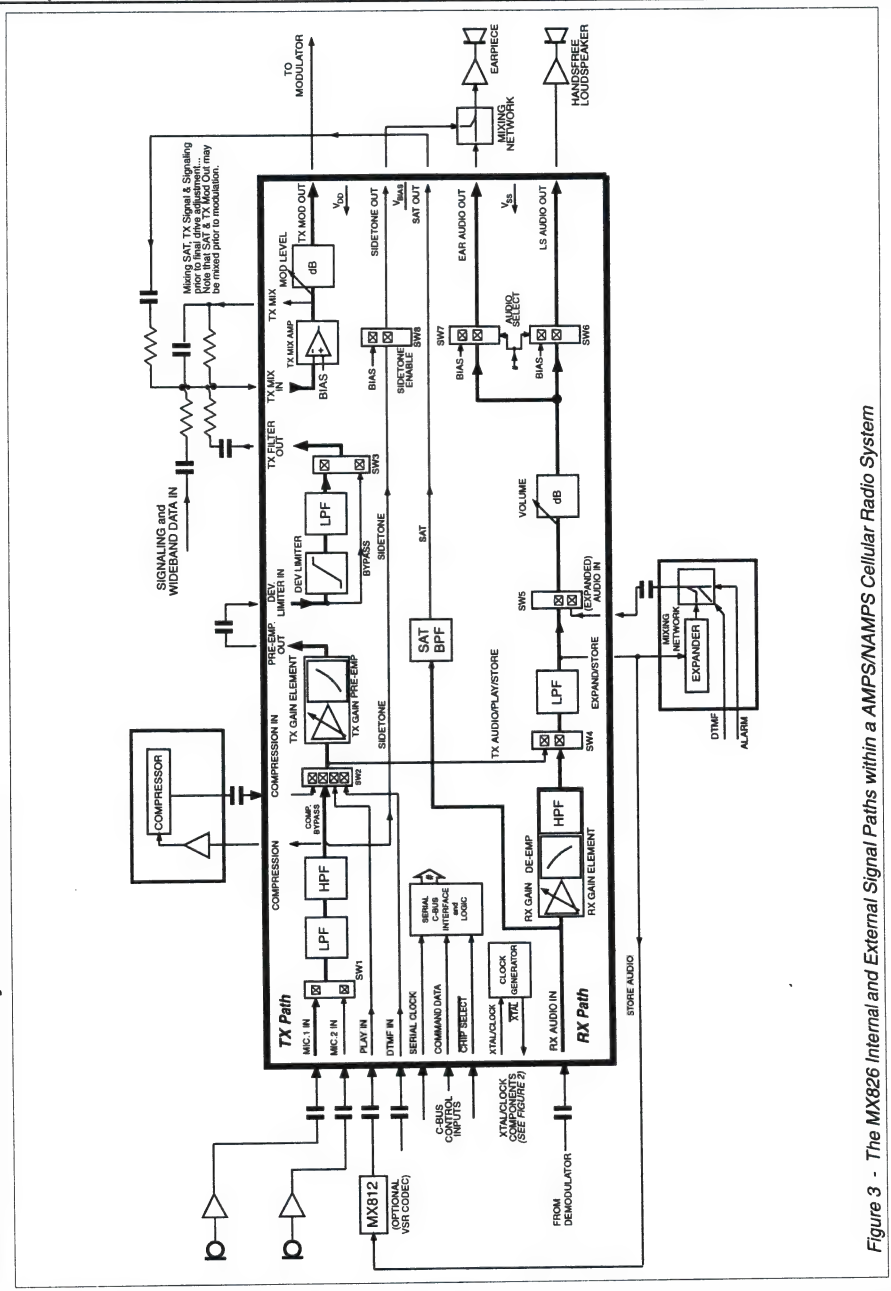


Figure 3 - The MX826 Internal and External Signal Paths within a AMPS/NAMPS Cellular Radio System

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480070.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

The Controlling System: C-BUS Hardware Interface

C-BUS is MX-COM's proprietary standard for the transmission of commands and data between a µController and MX-COM's New Generation integrated circuits. C-BUS has been designed for a low IC pin-count, flexibility in handling variable amounts of data, and simplicity of system design and µController software.

It may be used with any µController, and can, if desired, take advantage of the hardware serial I/O functions built into many types of µController. Because of this flexibility and because the BUS data-rate is determined solely by the µController, the system designer has complete freedom to choose a µController appropriate to the overall system processing requirements.

Control of the functions and levels within the MX826 is by a group of Address/Commands and appended data instructions from the system µController to set/adjust the functions and elements of the device. The use of these instructions is detailed in the following paragraphs and tables.

Command Assignment	Address/Command (A/C) Byte Hex	Binary (MSB … LSB)		Command Data	Table
General Reset	01	0 0 0 0 0 0 0 1			
Configuration Command	10	0 0 0 1 0 0 0 0	+	1 byte	2
TX Gain & Mod. Command	11	0 0 0 1 0 0 0 1	+	1 byte	3
RX Gain & Vol. Command	12	0 0 0 1 0 0 1 0	+	1 byte	4
Powersave Command	13	0 0 0 1 0 0 1 1	+	1 byte	5

Table 1 "C-Bus" Address/Commands

In C-BUS protocol the audio processor is allocated Address/Command (A/C) values 10_H to 13_H. Configuration, TX/RX Gains, Powersave assignments and data requirements are given in Table 1. Each instruction consists of an Address/Command (A/C) byte followed by a data instruction formulated from the following tables.

Commands and Data are only to be loaded in the group configurations detailed, as the C-BUS interface recognizes the first byte after Chip Select (logic "0") as an Address/Command. Function or Level control data, which is detailed in Tables 2, 3, 4 and 5, is acted upon at the end of the loaded instruction. See Timing Diagrams, Figures 5 and 6.

Upon Power-Up the value of the "bits" in this device will be random (either "0" or "1"). A **General Reset Command (01_H)** will be required to set all MX826 registers to 00_H.

Configuration Command *(Preceded by A/C 10_H)*

Setting		Control Bits
MSB Bit 7		***Transmitted First***
0		**Sw8 Sidetone** Sidetone Bias
1		Sidetone Enabled
6		**Sw6/7 RX Audio**
0		Ear Enabled, LS Bias
1		LS Enabled, Ear Bias
5		**Sw5 Expandor**
0		Expander By-Pass
1		Expander Route
4		**Sw4 TX/RX Audio**
0		Tx Store/Audio
1		Rx Store/Audio
3		**Sw3 Dev. Limiter**
0		Dev. Limiter Bypass
1		Dev. Limiter Route
2		**Sw1 Mic. Inputs**
0		Mic. 1 Input
1		Mic.2 Input
1	***0***	**Sw2 TX Function**
0	0	DTMF In
0	1	Compressor Bypass
1	0	Compressor In
1	1	Play In

Table 2 Configuration Commands

TX Gain & Mod. Command *(Preceded by A/C 11_H)*

Setting				Gain (dBs)
MSB				***Transmitted First***
7	***6***	***5***	***4***	**Tx Mod. Level**
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-5.6
0	0	1	0	-5.2
0	0	1	1	-4.8
0	1	0	0	-4.4
0	1	0	1	-4.0
0	1	1	0	-3.6
0	1	1	1	-3.2
1	0	0	0	-2.8
1	0	0	1	-2.4
1	0	1	0	-2.0
1	0	1	1	-1.6
1	1	0	0	-1.2
1	1	0	1	-0.8
1	1	1	0	-0.4
1	1	1	1	0
3	***2***	***1***	***0***	**TX Input Gain**
0	0	0	0	-2.65
0	0	0	1	-2.05
0	0	1	0	-1.50
0	0	1	1	-0.95
0	1	0	0	-0.45
0	1	0	1	0
0	1	1	0	0.45
0	1	1	1	0.85
1	0	0	0	1.25
1	0	0	1	1.65
1	0	1	0	2.05
1	0	1	1	2.40
1	1	0	0	2.70
1	1	0	1	3.05
1	1	1	0	3.35
1	1	1	1	3.65

Table 3 TX Gain & Mod. Commands

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480070.004

The Controlling System .....

RX Gain & Vol. Command *(Preceded by A/C 12$_H$)*

Setting				Gain (dBs)
MSB				Transmitted First
7	6	5	4	RX Volume
0	0	0	0	OFF (Low Z to V_{BIAS})
0	0	0	1	-28.0
0	0	1	0	-26.0
0	0	1	1	-24.0
0	1	0	0	-22.0
0	1	0	1	-20.0
0	1	1	0	-18.0
0	1	1	1	-16.0
1	0	0	0	-14.0
1	0	0	1	-12.0
1	0	1	0	-10.0
1	0	1	1	-8.0
1	1	0	0	-6.0
1	1	0	1	-4.0
1	1	1	0	-2.0
1	1	1	1	0
3	2	1	0	RX Input Gain
0	0	0	0	3.75
0	0	0	1	4.30
0	0	1	0	4.80
0	0	1	1	5.30
0	1	0	0	5.80
0	1	0	1	6.20
0	1	1	0	6.55
0	1	1	1	7.05
1	0	0	0	7.40
1	0	0	1	7.80
1	0	1	0	8.15
1	0	1	1	8.50
1	1	0	0	8.80
1	1	0	1	9.10
1	1	1	0	9.40
1	1	1	1	9.70

Table 4 - RX Gain and Vol. Commands

Powersave Command *(Preceded by A/C 13$_H$)*

Setting							Control Bits
MSB Bit 7							Transmitted First
7	6	5	4	3	2	1	
0	0	0	0	0	0	0	All must be a logic "0"
			0				Powersave Setting
			0				Powersave MX826
			1				Enable MX826

Table 5 - Powersave Command

Reference Signal Levels

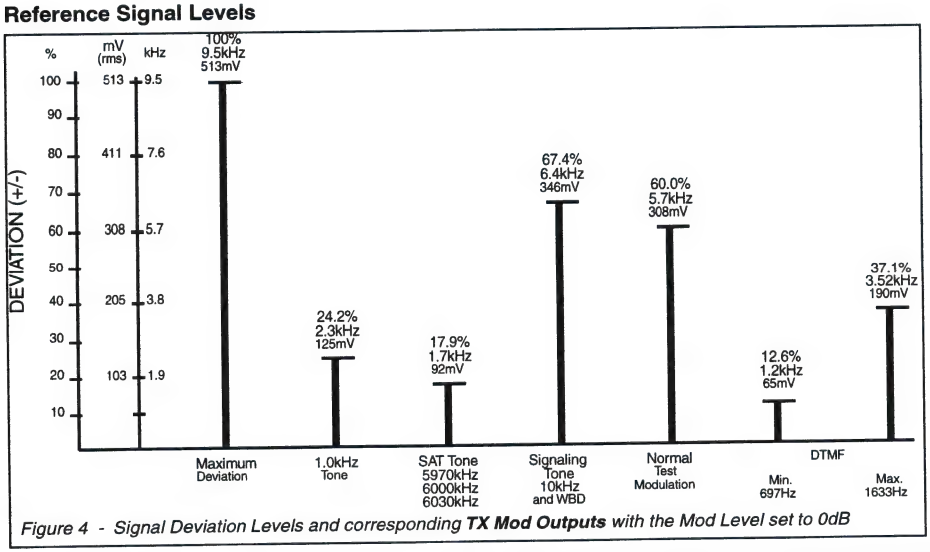


*Figure 4 - Signal Deviation Levels and corresponding **TX Mod Outputs** with the Mod Level set to 0dB*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480070.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Control Timing Information

Characteristics		See Note	Min.	Typ.	Max.	Unit
t_{CSE}	"CS-Enable to Clock-High"	1	2.0	–	–	µs
t_{CSH}	Last "Clock-High to CS-High"	1	4.0	–	–	µs
t_{CSOFF}	"CS-High" Time between transactions	1, 2	2.0	–	–	µs
t_{CK}	"Clock-Cycle" Time	1	2.0	–	–	µs
t_{NXT}	"Inter-Byte" Time	1	4.0	–	–	µs
t_{CH}	"Serial Clock-High" Period		500	–	–	ns
t_{CL}	"Serial Clock-Low" Period		500	–	–	ns
t_{CDS}	"Command Data Set-Up" Time		250	–	–	ns
t_{CDH}	"Command Data Hold" Time		0	–	–	ns

Notes

1. These Minimum Timing values are altered during operation of the MX812 VSR Codec.
2. Chip Select must be taken to a logic "1" between each individual transaction.

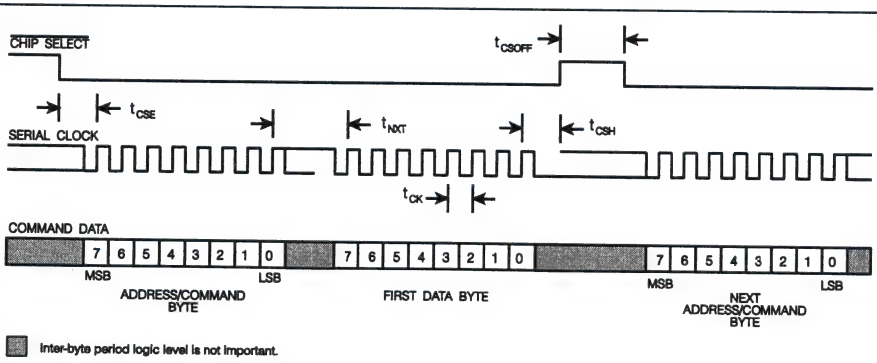


Figure 5 - Control Timing Information

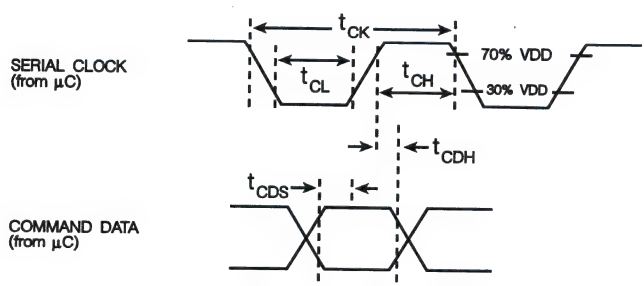


Figure 6 - Control Timing Relationships

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480070.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Frequency Responses

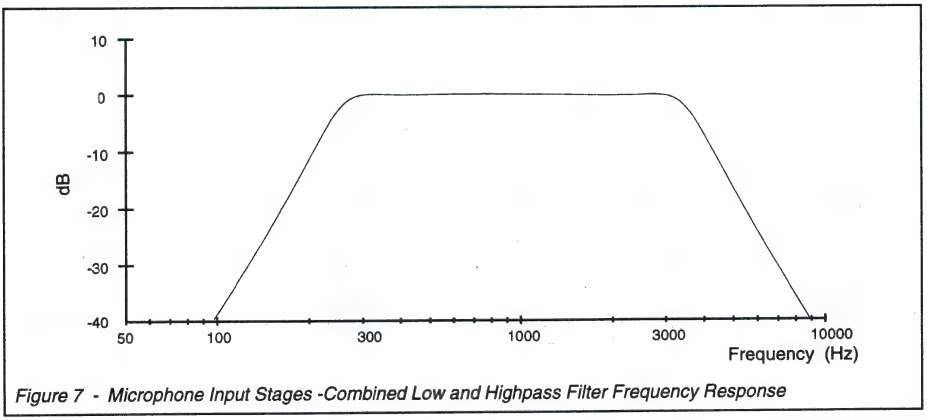


Figure 7 - Microphone Input Stages -Combined Low and Highpass Filter Frequency Response

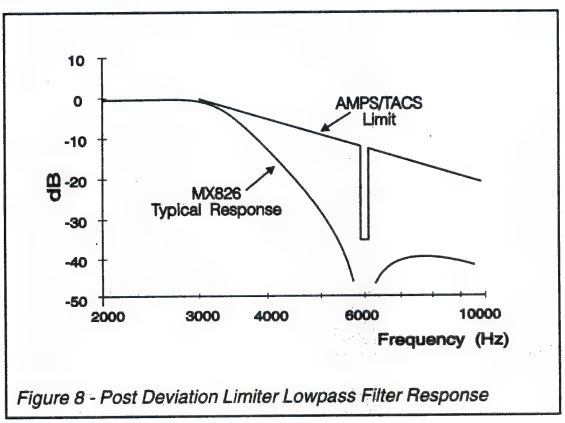


Figure 8 - Post Deviation Limiter Lowpass Filter Response

Figure 7
Mic.1/2 In to Compression Out

V_{DD} = 5.0V

Signal Input Level = 55.0mVrms

Figure 8
Dev Limiter In to TX Filter Out

V_{DD} = 5.0V

Signal Input Level = 55.0mVrms

Figure 9

RX Audio In to SAT out

V_{DD} = 5.0V

Signal Input Level = 100mVrms

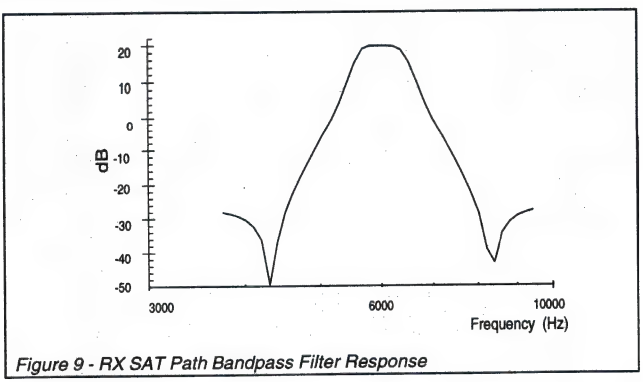


Figure 9 - RX SAT Path Bandpass Filter Response

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480070.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin	
(Ref V_{SS} = 0V)	-0.3V to (V_{DD} + 0.3V)
Sink/source Current	
(Supply pins)	±30mA
(Other pins)	±20mA
Total Device Dissipation	
@T_{AMB} 25°C	800mW max.
Derating	10mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

Operating Limits

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/clock f_{XTAL} = 4.0MHz

Audio level 0dB ref. = 308mVrms @ 1kHz

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
Operating		–	6.5	–	mA
Powersave		–	0.5	–	mA
Alias Frequency		–	63.0	–	kHz
On-Chip Xtal Oscillator					
R_{IN}		10.0	–	–	MΩ
R_{OUT}		–	10.0	–	kΩ
Inverter d.c. Voltage Gain		–	10.0	–	V/V
Gain/Bandwidth Product		–	10.0	–	MHz
TX Mix Amp (Open Loop Gain)		–	50.0	–	dB
(Bandwidth)		20.0	–	–	kHz
Analog Input Impedances					
Mic.1 & 2		–	500	–	kΩ
Play		–	500	–	kΩ
Comp In		–	500	–	kΩ
DTMF In		–	500	–	kΩ
Dev. Limiter In		–	100	–	kΩ
(Expanded) Audio In		–	47.0	–	kΩ
TX Mix In		10.0	–	–	MΩ
RX Audio In		–	100	–	kΩ
Analog Output Impedances					
Pre-Emp Out		–	600	–	Ω
TX Mod Out		–	600	–	Ω
Expand/Store		–	600	–	Ω
LS and Ear Audio		–	1.0	–	kΩ
SAT Out	3	–	1.0	–	kΩ
TX Filter Out		–	600	–	Ω
Comp Out		–	600	–	Ω
Sidetone Out		–	2.0	–	kΩ
TX Mix (Open Loop)		–	6.0	–	kΩ
(Closed Loop)		–	600	–	Ω
Switches – ON		–	1.0	–	kΩ
– OFF		10.0	–	–	MΩ

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480070.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Control Interface Parameters					
Input Logic Levels					
Logic "1"	1	3.5	–	–	V
Logic "0"	1	–	–	1.5	V
I_{IN} (logic "1" or "0")	1	-1.0	–	1.0	µA
Input Capacitance	1	–	–	7.5	pF
Channel Performances					
TX Path					
Filter Specifications					
Pre-Compression L/HPF Combination					
Passband		300		3000	Hz
Slope - below 300Hz		+24.0	–	–	dB/oct.
above 3000Hz		-24.0	–	–	dB/oct.
TX Gain Pre-Emphasis					
Gain at 1.0kHz		–	0	–	dB
Slope (300Hz - 3000Hz)		–	6.0	–	dB/oct.
Post Deviation Limiter LPF					
Attenuation Relative to 1.0kHz					
3.0kHz - 5.9kHz		-	40 log(f/3000)	-	dB
5.9kHz - 6.1kHz		-	35.0	-	dB
6.1kHz - 15kHz		-	40 log(f/3000)	-	dB
>15kHz		-	28.0	-	dB
Analog Signal Input Levels					
Mic. 1 and 2	2	–	0	–	dB
Play	2	–	0	–	dB
DTMF	2	–	0	–	dB
Comp. In	2	–	0	–	dB
TX Mix In	2	–	0	–	dB
Analog Signal Output Levels					
Pre-Emp Out	2	–	0	–	dB
TX Filter Out	2	–	0	–	dB
TX Mod Out	2	–	0	–	dB
Sidetone Out	2	–	0	–	dB
Path Gains/Levels					
TX Gain – 11_H					
Nominal Adjustment Range		-2.65	–	3.65	dB
Error of any Setting		-0.2	–	0.2	dB
Dev Limiter					
Threshold		–	1086	–	mVp-p
Symmetry		–	7.0	–	%
Mod Level Attenuation – 11_H					
Nominal Adjustment Range		-5.6		0	dB
Step Size		0.2	0.4	0.6	dB
Error of any Setting		-1.0	–	1.0	dB
Overall					
TX Distortion		–	-40.0	-32.0	dBp
TX Hum and Noise		–	-40.0	-20.0	dB
RX Signal Path					
Filter Specifications					
RX Gain De-Emphasis					
Gain at 1.0kHz		–	3.75	–	dB
Slope (300Hz - 3000Hz)		–	-6.0	–	dB/oct.
RX Channel Bandpass		300		3000	Hz
Slope - below 300Hz		+24.0	–	–	dB/oct.
above 3000Hz		-36.0	–	–	dB/oct.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480070.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Characteristics	See Note	Min.	Typ.	Max.	Unit
RX Signal Path (cont'd)					
Analog Signal Levels					
RX Audio Input Level	2	–	-7.0	–	dB
LS/Ear Audio Output Level	2	–	0	–	dB
Path Gains/Levels					
RX Gain – 12_H					
Nominal Adjustment Range		3.75		9.70	dB
Error of any Setting		-0.2	–	0.2	dB
Volume – 12_H					
Nominal Adjustment Range		-28.0		0	dB
Step Size		1.5	2.0	2.5	dB
Error of any Setting		-1.0	–	1.0	dB
Overall					
RX Distortion		–	-40.0	-32.0	dBp
RX Hum and Noise		–	-40.0	-34.0	dB
SAT Signal Path					
Bandpass Filter					
Frequency Range		5970		6030	Hz
Gain		19.0	20.0	21.0	dB

Notes

1. Serial Clock, Command Data and Chip Select inputs.
2. Levels equivalent to ±3.0kHz deviation with the settings below:
   TX Gain = 0dB *Mod Level = 0dB*
   RX Gain = 7.05dB *Volume = 0dB*
   Other levels can be achieved by adjusting the above variable gain blocks in accordance with Tables 1 to 5.
3. Recommended load >10.0kΩ.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480070.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

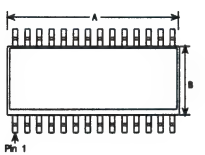
Package Outline

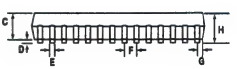
The MX826 packages available are shown below. Pin 1 is marked with an indent spot. Pins on both package styles number counter-clockwise when viewed from the top (marked side).

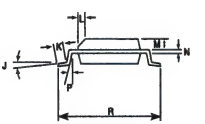
Handling Precautions

The MX826 is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

*Fig.10 **MX826DW** 28-pin Small Outline I.C. Package*



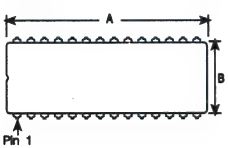


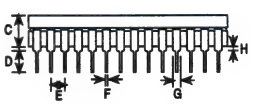


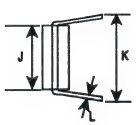
Package Tolerances

Dimension In,(mm)	Min.	Max.
A	0.698 (17.72)	0.708 (17.97)
B	0.291 (7.39)	0.299 (7.59)
C	0.092 (2.33)	typical
D	0.004 (0.102)	0.012 (0.304)
E	0.014 (0.36)	0.018 (0.46)
F	0.050 (1.27)	typical
G	0.026 (0.66)	typical
H	0.096 (2.43)	0.104 (2.64)
J	5°	typical
K	0.020 (0.51)	0.040 (1.02)
L	0.025 (0.63)	typical
M	0.041 (1.04)	typical
N	0.009 (0.23)	0.011 (0.28)
P	5°	typical
R	0.39 (9.91)	0.414 (10.51)

*Fig.11 **MX826J** 28-pin Ceramic Dual In-Line Package*







Package Tolerances

Dimension In,(mm)	Min.	Max.
A	1.44 (36.58)	1.46 (37.05)
B	0.51 (13.06)	0.53 (13.36)
C	0.18 (4.49)	0.220 (5.57)
D	0.12 (3.0)	0.15 (3.81)
E	0.10 (2.54)	typical
F	0.018 (0.45)	typical
G	0.055 (1.39)	typical
H	0.02 (.50)	0.05 (1.30)
J	0.61 (15.50)	0.62 (15.70)
K	0.670 (17.0)	typical
L	0.009 (0.25)	typical

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480070.004
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Technical Specifications

Section 9: General Purpose IC's

Device	Description	Page
Signal Processing		3
MX102	Autocorrelator	5
MX105A	Tone Detector	15
Digital Control Amplifiers		29
MX019	Quad Digitally Controlled Amplifier	31
MX029	Dual Digitally Controlled Amplifier	43
Digitally Controlled Analog I/O Processors		55
MX839	Digitally Controlled Analog I/O Processor	57

Technical Specifications

Signal Processing IC's

Device	Description	Page
MX102	Autocorrelator	5
MX105A	Tone Detector	15

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX102

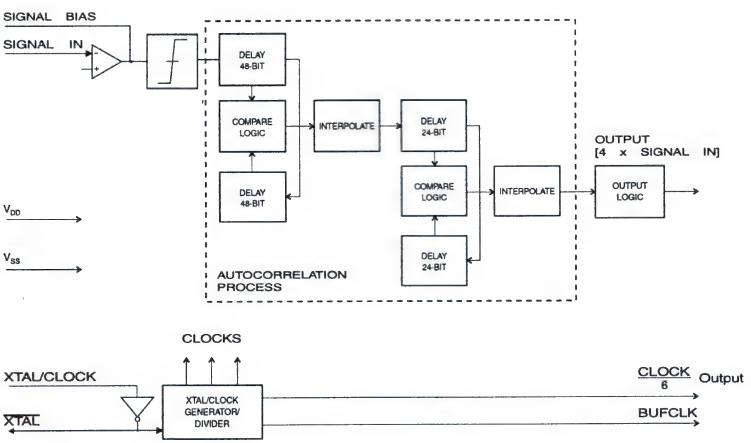
Autocorrelating Signal Processor

Features

- Low Signal Level Input of 10mVrms
- Wide Signal Frequency Range from 17Hz to 13kHz
- On-Chip Gain Amplifier
- Digital Output Signal (f_{IN} x 4)
- Divided-Down Clock Output
- Low Supply Voltage Operation of 2.5 V
- Low Current Drain

Applications

- Medical Instruments
- Sonar Detection
- Remote Signaling
- Pagers
- Mobile Radio
- Slow Data Rate Communication
- Tone Detection



The MX102 is a single-chip device to extract single periodic signals from very high random-noise environments.

Using patented autocorrelation techniques the MX102 will enhance the input signal's signal-to-noise ratio by as much as 8.5dB and provide a digital output signal centered at four times (x4) the input frequency.

The amplitude of non-periodic components of the signal is substantially reduced. The patented autocorrelator compares the incoming signal to itself; the more elements of the waveform that are seen as periodic, the higher the energy at the microcircuit output.

The MX102 cascades two autocorrelators, each one improving the signal-to-noise ratio

With a random noise input the output will swing rail-to-rail at random (peak-limited). The input/output signal delay is fixed by the choice of clock frequency and the length of the internal register. The MX102 will operate at supply voltages of between 2.5 volts and 5.5 volts and with Xtal/clock frequencies from 20kHz to 2.5MHz. Using various Xtal/clock inputs the device can be set to accept input signal frequencies, in bands, from 17.0Hz to 13.0kHz.

Two uncommitted clock outputs are available: one to supply a 'divided-down' Xtal/clock frequencies and the second is a buffered output for use in external and peripheral functions.

This MX102 is available in the following package styles: 16-pin SOIC (MX102DW) and 16-pin CDIP (MX102J).

© 1997 MX•COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc.# 20480095.003

CONTENTS

Section **Page**

1. Block Diagram **9-7**

2. Signal List **9-8**

3. External Components **9-9**

4. General Description **9-10**

4.1 Signal 9-10

4.2 Input Frequency Range 9-10

5. Performance Specification **9-12**

5.1 Electrical Performance 9-12

5.2 Packaging 9-14

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM,INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480095.003
4800 Bethania Station road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1. Block Diagram

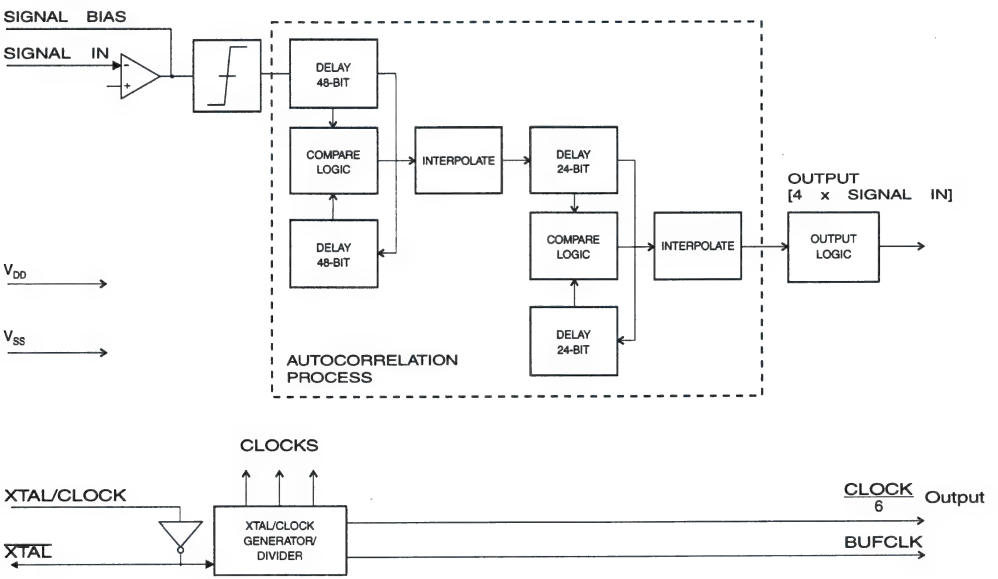


Figure 1: Device Block Diagram

© 1997 MX-COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc.# 20480095.003

2. Signal List

Packages	Signal		Description
DW/J	Name	Type	
1	Signal In	input	The inverting input to the analog amplifier/comparator. Used with the Signal Bias pin; external coupling components are required. See Figure 2
3	Signal Bias	output	The output of the analogue amplifier/comparator. Do not load this pin with peripheral circuitry; there is no drive capacity for off-chip signaling. The feedback resistor should be not less than 200kΩ. See Figure 2.
4	V_{DD}	power	Positive supply rail. A single, stable power supply is required. Note that this device has two V_{DD} pins; this input is positioned to prevent cross-talk, either or both may be connected to the host circuit's supply line. Do not attempt to draw current from either V_{DD} pin.
5	BUFCLK	output	Buffered inverter oscillator digital output. May be used as test point to align clock frequency or to drive other circuitry.
6	$\overline{XTAL}$	output	The output of the on-chip clock oscillator inverter.
8	Xtal/Clock	input	The input to the on-chip clock oscillator inverter; this may be a Xtal, resonator or clock pulse input. The selection of this frequency will affect the operational input signal bandwidth (and output frequency) of this device; refer to Table 4. Note that the choice of V_{DD} will determine the maximum Xtal/clock frequency and hence the maximum useable signal input frequency. Operation of this microcircuit without an active Xtal or clock input may cause device damage. A clock pulse input is fed directly into this pin; Xtal/clock components are not required. See Table 2.
9	V_{SS}	power	Negative Supply
11	CLK ÷ 6	output	A squarewave output clock signal at the rate of Clock/6; provided for peripheral and test purposes.
13	OUTPUT	output	(fOUT = 4 x fSIGNAL IN). The auto-correlated output signal at four times (x 4) the input signal (see Figure 3). There is a time delay between input and output signals (see Specifications).
16	V_{DD}	power	Positive supply rail. A single, stable power supply is required. Note that this device has two V_{DD} pins; either or both may be connected to the host circuit's supply line. Do not attempt to draw current from either V_{DD} pin. The choice of V_{DD} will determine the maximum Xtal/clock frequency and hence the maximum useable signal input frequency (see Figure 4).
2, 7, 10, 12, 14, 15		N/C	No internal connection. Leave open circuit

Table 1: Signal List

© 1997 MX•COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc.# 20480095.003

V_{DD} (V)	Max. Xtal/Clock Freq. (MHz)
2.5	0.625
3.0	1.0
5.0	2.5

Table 2: Maximum Usable Xtal/Clock Frequencies

3. External Components

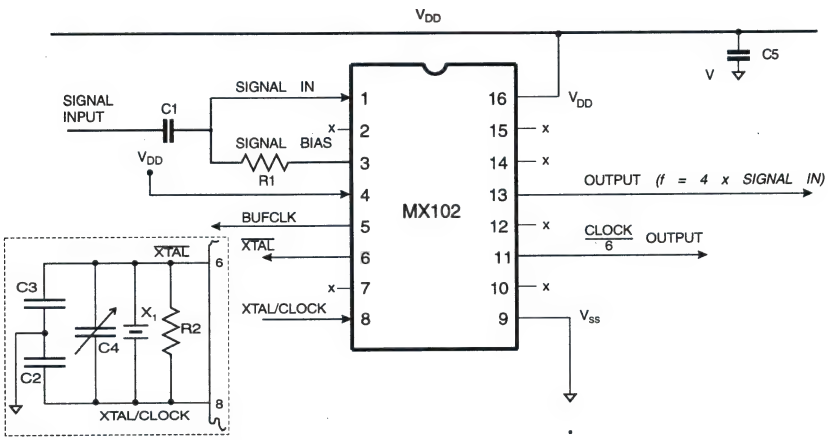


Figure 2: Recommended External Components

R1		2.2MΩ
R2		1.0MΩ
C1		0.01µF
C2	Note 1	47.0pF -see below
C3	Note 1	47.0pF -see below
C4	Note 2	5 - 65pF -see below
C5		1.0µF
X1		560kHz resonator
X1 range		20kHz to 2.5MHz

Table 3: Recommended External Components

Recommended External Component Notes:

1. Values of capacitors C2 and C3 should be reduced for higher Xtal frequencies and/or lower supply voltages (V_{DD}).
2. C4 is suggested for frequency setting when using a resonator; when a Xtal is used C4 is omitted.

© 1997 MX•COM,INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480095.003
4800 Bethania Station road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4. General Description

4.1 Signal

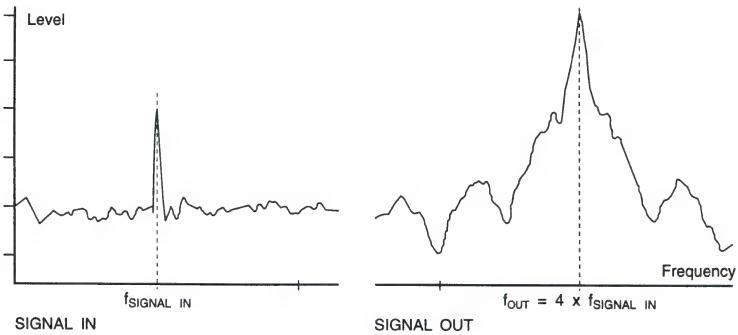


Figure 3: MX102 Input/Output Relationships

Note:

1. The frequency of the output signal is four times (x4) that of the input signal.

4.2 Input Frequency Range

The MX102 has a wide frequency range, but care must be taken to choose the Xtal frequency appropriate for your application.

Xtal/Clock Frequency (kHz)	Input Freq. (Hz)		BW (Hz)
	Min.	Max.	
20	17	105	88
100	88	526	443
200	166	1052	886
300	250	1579	1329
400	333	2105	1772
500	416	2632	2216
560	467	2947	2480
600	500	3158	2658
700	583	3684	3101
800	667	4210	3543
900	750	4737	3987
1000	833	5263	4430
2000	1667	10526	8859
2500	2083	13157	11074

Table 4: Input Signal Ranges vs Xtal/Clock Frequency

© 1997 MX-COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc.# 20480095.003

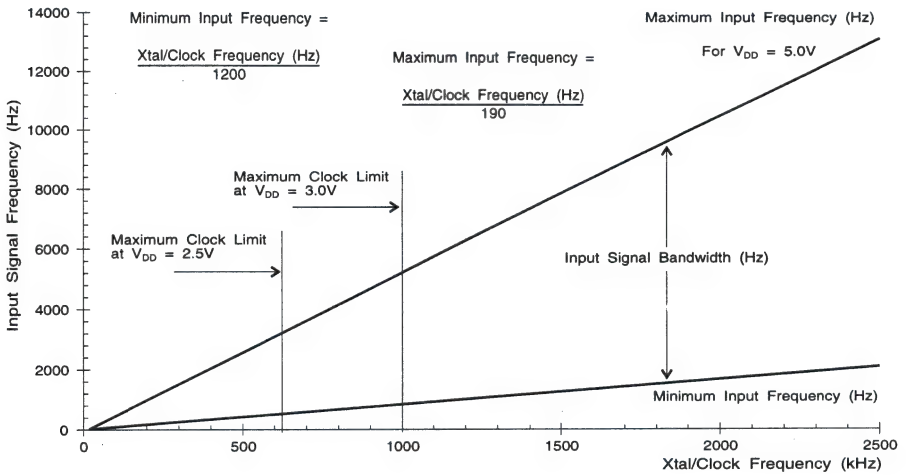


Figure 4: Input Signal Ranges vs Xtal/Clock Frequency

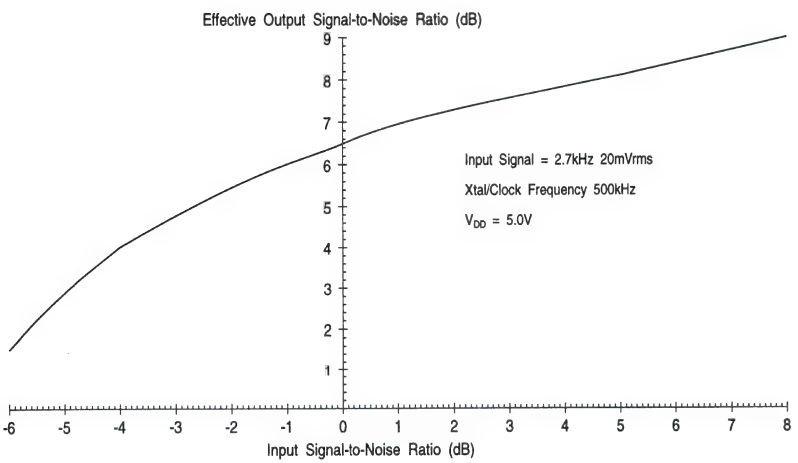


Figure 5: Enhancement of Signal-To-Noise Ratio

Note:

1. The graph shown in Figure 5 illustrates the signal-to-noise enhancement that can be obtained, under varying input conditions, from the MX102.

© 1997 MX•COM,INC. **www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054** **Doc.# 20480095.003**
4800 Bethania Station road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. Performance Specification

5.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply Voltage	-0.3	7.0 volts	V
Input Voltage at any pin	-0.3	(V_{DD}+0.3 volts)	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
Maximum Device Dissipation	100		mW
Operating Temperature	-40°	85	°C
Storage Temperature	-40°	125	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	Typ.	Max.	Units
V_{DD}	2.5	3.3/5.0	5.5	V
Xtal/Clock	20		2500	kHz
Operating Temperature	-40		85	°C

© 1997 MX•COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc.# 20480095.003

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C
Xtal/Clock = 560kHz, Input Test Signal = 200mV_{RMS}

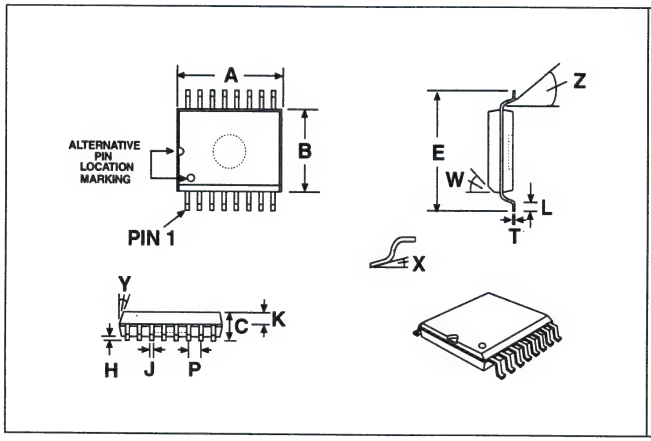
	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Current		-	1.0	2.5	mA
	2	-	4.0	-	mA
Logic '1' Level		80%	-	-	V
Logic '0' Level		-	-	20%	V
Digital Output Impedance		-	4.0	10.0	kΩ
Dynamic Values					
Signal Input	3	20.0	-	1000	mV_{RMS}
Analog (Input) Amplifier Gain	4	20.0	-	-	dB
	5	9.0	-	-	dB
	6	10.0	-	-	dB
Recommended Input Signal Duty Cycle Ratio		35	50	-	%
Frequency Out/Frequency In Ratio		4.0	-	4.0	%
Maximum Xtal/Clock Frequency	1	2.5	-	-	MHz
Minimum Xtal/Clock Frequency				20.0	kHz
Frequency Input Range					
Xtal/Clock = 560kHz	7	500	-	3000	Hz
Table 4		1/1200		1/190	Xtal/Clock
Input to Output Delay	8	-	1.4		ms
Output resolution		-	1/6	-	Xtal/Clock

Operating Characteristics Notes:

1. Maximum Xtal/clock frquency allowed varies with applied supply voltage (V_{DD}).
2. I_{DD} requirement for Xtal/clock frequency of 2.24MHz.
3. Signal input level required to provide a constant autocorrelated output.
4. Measured with a 6.0kHz sinewave at the signal input.
5. Measured with V_{DD} = 2.5 volts.
6. Measured with a 12kHz input signal.
7. Recommended input signal frequency range to correlation circuits.
8. Input (Signal In) to output (Output) time with a 2.24MHz Xtal/clock input.

© 1997 MX•COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc.# 20480095.003

5.2 Packaging

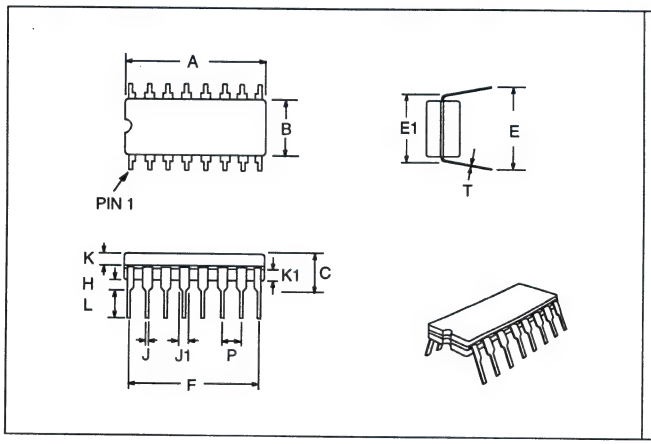


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin SOIC Mechanical Outline: *Order as part no. MX102DW*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.753 (19.13)		0.767 (19.48)
B	0.285 (7.24)		0.291 (7.39)
C	0.165 (4.19)		0.230 (5.84)
E	0.370 (9.40)		0.415 (10.53)
E1	0.300 (7.61)		0.317 (8.04)
F		0.70 (17.78)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.053 (1.33)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 16-pin CDIP Mechanical Outline: *Order as part no. MX102J*

© 1997 MX•COM,INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station road, Winston-Salem, NC 27105-1201 USA
Doc.# 20480095.003
All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

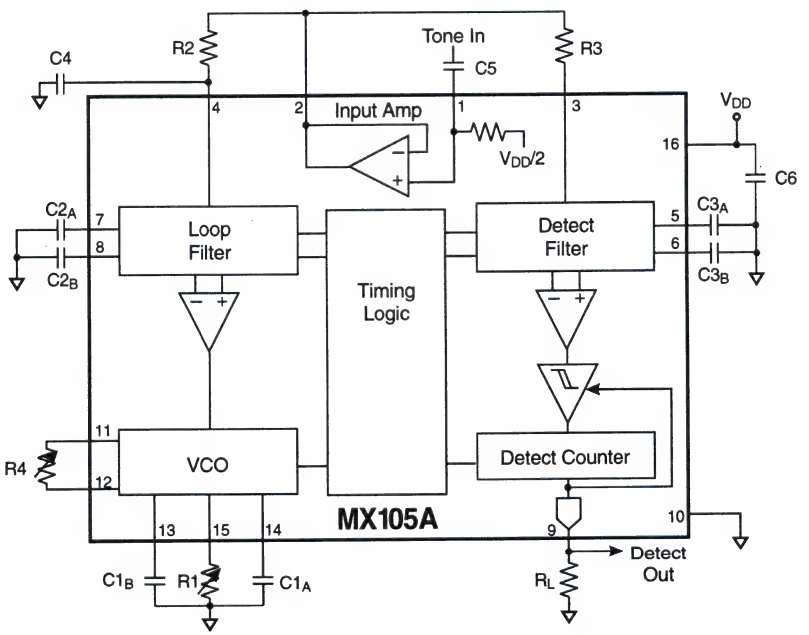
DATA BULLETIN

MX105A Tone Detector

PRELIMINARY INFORMATION

- **FEATURES**
- **Operates in High Noise Conditions**
- **≥36 dB Signal Input Range**
- **High Sensitivity**
- **Low Power Operation 2.7 V to 5.5 V**
- **Adjustable Bandwidth**
- **Adjustable Frequency**

- **APPLICATIONS**
- **Single and Multitone System Applications**



The MX105A is a monolithic CMOS tone detector for tone decoding in single and multitone signaling systems. Using phase locked loop (PLL) decoding techniques, the MX105A recognizes tones in the presence of high noise levels and strong adjacent channel tones. Detection frequency and bandwidth can each be independently adjusted. The design is immune to high levels of harmonic and sub-harmonic noise. It also maintains excellent noise immunity and constant bandwidth over a wide range of input signal levels.

The MX105A requires a voltage supply of 2.7V to 5.5V and is available in the following package styles: 16-pin SOIC (MX105ADW), 16-pin PDIP (MX105AP), and 24-pin PLCC (MX105ALH).

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc.# 20480133.003
All trademarks and service marks are held by their respective companies.

CONTENTS

Section ..... **Page**

1. Block Diagram **9-17**

2. Signal List **9-18**

3. External Components **9-19**

4. General Description **9-20**

5. Application **9-21**

5.1 Method for Calculating External Component Values 9-21
5.2 Define f_0 9-21
5.3 Calculate Minimum Usable Bandwidth 9-21
5.4 Calculate The Recommended Operating Bandwidth 9-21
5.5 Select R4 for Operating BW 9-22
5.6 Calculate $R2 \times C2_A$ 9-22
5.7 Define Maximum Allowed Response Time 9-22
5.8 Calculate $R3 \times C3_A$ 9-22
5.9 Calculate Maximum De-response Time 9-23
5.10 Calculate Signal to Noise Performance 9-24
5.11 Calculate C4 for 30° Phase Shift 9-24

6. Performance Specification **9-25**

6.1 Electrical Performance 9-25
6.1.1 Absolute Maximum Ratings 9-25
6.1.2 Operating Limits 9-25
6.1.3 Operating Characteristics 9-26
6.2 Packaging 9-27

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc.# 20480133.003

1. Block Diagram

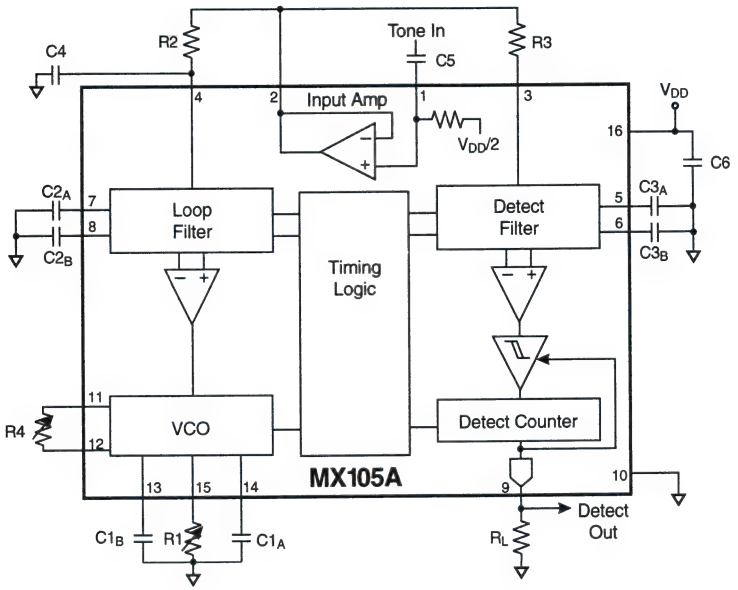


Figure 1: Block Diagram

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480133.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. Signal List

Pin No. DW/P	Pin No. LH	Name	Type	Description
1	1	INPUT AMP IN	input	AC couple to this input. Nominal input impedance is 200 kΩ.
2	3	INPUT AMP OUT	output	Nominal output impedance is 1 kΩ.
3	5	R3	input	Detect filter resistor pin.
4	6	R2	input	PLL loop filter resistor pin. For improved performance C4 may be chosen to provide 30° of phase shift at the loop filter input.
5	7	$C3_A$	output	Detect filter capacitor pin A
6	8	$C3_B$	output	Detect filter capacitor pin B
7	10	$C2_A$	output	Loop filter capacitor pin A
8	11	$C2_B$	output	Loop filter capacitor pin B
9	13	DETECT OUT	output	PMOS open drain output - active on detect.
10	14	V_{SS}	power	Ground.
11	16	$R4_A$	input	Bandwidth control resistor pin A
12	17	$R4_B$	input	Bandwidth control resistor pin B
13	19	$C1_B$	output	VCO capacitor B
14	20	$C1_A$	output	VCO capacitor A
15	22	R1	input	VCO discharge resistor. When potentiometer tuning is required, a series resistor is recommend to prevent possible shorting to ground.
16	24	V_{DD}	power	Power supply.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480133.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components

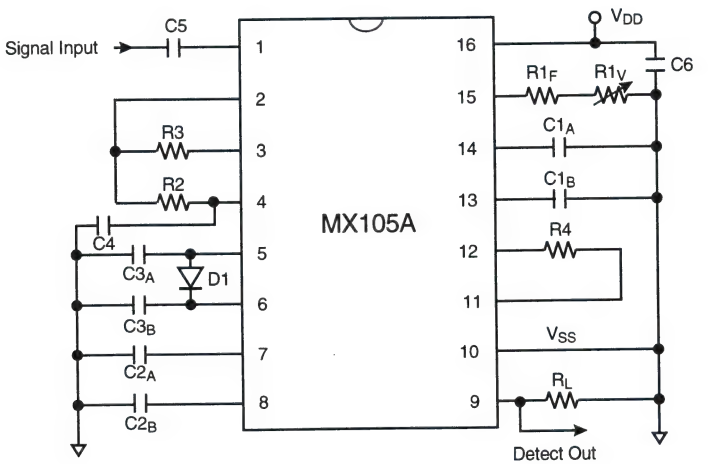


Figure 2: Recommended External Components

$R1_F$	See Section 5.2	300kΩ	
$R1_V$	See Section 5.2	100kΩ	
R2	See Section 5.6		
R3	See Section 5.8		
R4	See Section 5.5		
R_L	Note 4	20kΩ	±20%
$C1_A$	See Section 5.2 Note 2		
$C1_B$	See Section 5.2 Note 2		

$C2_A$	See section 5.6 Note 2		
$C2_B$	See Section 5.6 Note 2		
$C3_A$	See Section 5.8 Note 2		
$C3_B$	See Section 5.8 Note 2		
C4	See Section 5.11 Note 1, 2		
C5		0.27µF	±20%
C6		0.1µF	±20%
D1	See Section 5.9 Note 3	small signal diode (1N914)	

External Components Notes:

1. For improved performance, C4 may be chosen to provide 30° phase shift at the VCO loop filter input.
2. For compatibility with the MX105; capacitors (C1 - C4) may be connected to V_{DD} instead of V_{SS}.
3. For improved de-response time, a diode (D1) may be added.
4. Any value load resistance (R_L) may be used, providing the maximum load current does not exceed the value given in 'Maximum Ratings Specifications'.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480133.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4. General Description

The MX105A implements a frequency detector with a phase locked loop (PLL) and a lock detector. The voltage controlled oscillator (VCO) center frequency, detection bandwidth, loop filter, and detect filter are all independently controlled by external components.

The MX105A provides a pair of pseudo-sinewave multipliers for splitting the input signal into approximately orthogonal components. These multipliers are implemented with commutating filters (cyclically sampling filters) which translate an in band AC input signal to DC. The commutating loop filter is used as the phase detector of the PLL while the commutating detect filter provides for lock detection. Each pseudo-sinewave has a cyclic form (1 1 0 -1 -1 0) to eliminate low order harmonic responses. The loop filter produces an error signal, which when applied to the VCO input allows frequency locking. A limiter between the loop filter output and the VCO input provides tunable control of the detection bandwidth (BW). Once lock is achieved the detect filter produces a DC value proportional to the input tone amplitude. An internally generated reference is compared to the detect filter output to determine whether the PLL is locked to an input tone. Once lock is determined the internal reference is reduced by 50% to minimize output chatter with marginal input signals.

The sampling clocks of the detect filter lag those of the loop filter by 60°. To improve performance, a capacitor (C4) can be used to phase shift the input to the loop filter by 30°. This shifts all sampling clocks an additional 30° relative to the input tone to phase align the detect filter sampling clocks with the amplitude peaks of the input tone.

Figure 3 shows the sampling clocks relative to an in band input tone; this figure represents the steady state 'locked' condition without C4.

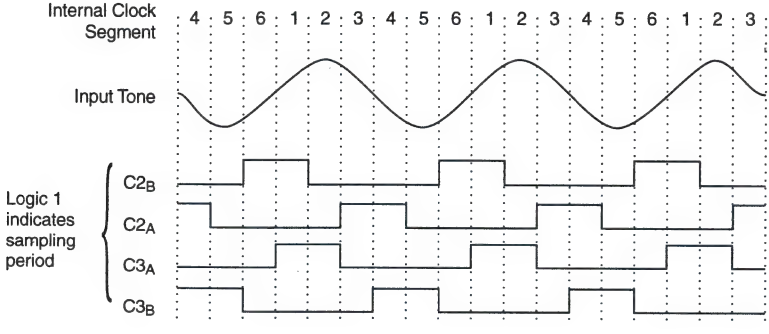


Figure 3: Sampling Clocks of Commutating Filters

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc.# 20480133.003

5. Application

The external components shown in Figure 2 are used to adjust the various performance parameters of the MX105A. The signal-to-noise performance, response time and signal bandwidth are all interrelated factors which should be optimized to meet the requirements of the application.

By selecting component values in accordance with the following formulas, optimum circuit performance is obtained for any given application.

First define the following application parameters:

A. The center frequency to be detected (f_0).

B. The MX105A Minimum Usable Bandwidth (MUBW). This is obtained by taking into account the worst case tolerances on the input tone frequency and variations in the MX105A f_0 due to supply voltage and any temperature effect of the MX105A and its supporting components.

C. The maximum permissible MX105A response time.

D. The minimum input signal amplitude.

Note: Using this information the appropriate component values can be calculated, and the signal-to-noise performance can be read from a chart. Do not add large safety margins for response time and minimum signal amplitude; reasonable margins are already included in the formulas. Excessive margins may result in reduced noise immunity.

5.1 Method for Calculating External Component Values

The examples on the following pages demonstrate the calculation of component values for any given application. For the purpose of the examples, the values below are used:

A. $f_0 = 2800$ Hz

B. $\Delta TEMP = 100\ °C$, $\Delta V_{DD} = 1V$, $\Delta f_{IN} = 0.5\%$

C. Maximum allowed response time = 50ms

D. Minimum input signal amplitude = 200 mV_{RMS}.

5.2 Define f_0

The components R1, $C1_A$ and $C1_B$ set the free running frequency of the VCO and therefore the f_0 of the MX105A. As shown below, the frequency of 2800 Hz corresponds to a capacitor value of 220pF and a resistor value of 385 kΩ. This resistance can be achieved with a 300 kΩ fixed resistor for $R1_F$ and for $R1_V$ a 100 kΩ potentiometer. The capacitance of $C1_A$ and $C1_B$ should include 10-20pF parasitic capacitance due to the device and its package plus any board parasitic capacitance.

$$f_0 = \frac{1}{K \cdot R1(C1_A + C1_B)} \Rightarrow R1 \times C1_A = \frac{1}{2Kf_0}$$

where : $K = 2.1 \pm 5\%$

$R1 = (R1_F + R1_V)$

5.3 Calculate Minimum Usable Bandwidth

Minimum Usable Bandwidth (MUBW) is the TOTAL bandwidth required for the following:

A. Input signal frequency tolerance

B. MX105A f_0 temperature coefficient ($T_C = 100$ ppm/°C)

C. MX105A f_0 supply voltage coefficient ($V_C = 5000$ ppm/V)

Note: Add A, B and C and express as TOTAL bandwidth, not as a ± percentage (%) value.

$$MUBW = \Delta f_0 + T_C \Delta TEMP + V_C \Delta V$$

$$MUBW = 0.5 + 0.01 \times 100 + 0.5 \times 1 = 2\%$$

5.4 Calculate The Recommended Operating Bandwidth

$$BW = \frac{10 + MUBW}{2} = \frac{10 + 2}{2} = 6\%$$

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480133.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.5 Select R4 for Operating BW

$$R4 = \frac{4.8 \times BW}{10.35 - BW} = \frac{4.8 \times 6}{10.35 - 6} \approx 6.8k\Omega$$

The exact bandwidth given by any value of R4 will vary slightly. In applications where an exact bandwidth is required, R4 should be a variable resistor to permit adjustment.

5.6 Calculate $R2 \times C2_A$

$$R2 \times C2_A \approx \frac{100}{3 \times f_0 \times BW}$$

For a frequency of 2800 Hz, a bandwidth of 6%, and a choice of $C2_A = 0.01\mu F \Rightarrow R_V = 200k\Omega$.

Note: Use nearest preferred values.

5.7 Define Maximum Allowed Response Time

The maximum response time (T_{ON}) is the sum of the VCO lock time (T_{LOCK}) and the DETECT integration time (T_{DETECT}). The MX105A's T_{ON} must not exceed the maximum time allowed for the application, but a value lying near the maximum gives the best S/N performance.

A. Calculate T_{LOCK}

$$T_{LOCK} = \frac{150}{f_0 \times BW}$$

Using the formula above, for a frequency of 2800 Hz and a bandwidth of 6% the approximate Lock time (T_{LOCK}) will be 9 ms. Since the maximum response time is 50 ms, a DETECT time of 41 ms is allowed.

Note: T_{LOCK} may vary from near zero to the value given, causing corresponding variations in actual T_{ON}.

B. Calculate Maximum Allowable T_{DETECT}

$$T_{DETECT} = T_{ON_{MAX}} - T_{LOCK}$$

C. Define Minimum Expected Signal Amplitude $\left(V_{IN_{MIN}}\right)$

This is used in calculating T_{DETECT} components.

5.8 Calculate $R3 \times C3_A$

$$R3 \times C3_A \approx \frac{T_{DETECT}}{-3 \times \ln\left(1 - \frac{V_{TH}}{V_{IN_{MIN}}}\right)}$$

where: V_{TH} is the detect filter sensitivity.

Note:

1. For a signal amplitude of 200 mV_{RMS}, a resistor value R3 of 510 kΩ with a 0.1μF capacitor for $C3_A$ and $C3_B$ will yield a T_{DETECT} time of 20ms. This in turn yields a response time of 9ms + 20 ms = 29ms.
2. Use nearest preferred values.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc.# 20480133.003
All trademarks and service marks are held by their respective companies.

5.9 Calculate Maximum De-response Time

$$T_{OFF} \approx -3 \times \ln\left(\frac{V_{TH}}{V_{IN_{MAX}}}\right) R3 \times C3_A$$

where: V_{TH} is the detect filter sensitivity.

For improved de-response time, a diode (1N914 or similar) can be placed between pins 5 and 6, as shown in Figure 3. The formula and figure below show the approximate time the MX105A will take to turn off after an in-band signal has been removed. The effect of this diode is to greatly reduce the turn-off time with signal input amplitudes greater than 300 mV_{RMS}. This graph is for V_{DD} = 5V; for lower V_{DD} KDT increases.

$$T_{OFF} \approx K_{DT} \times R3 \times C3_A$$

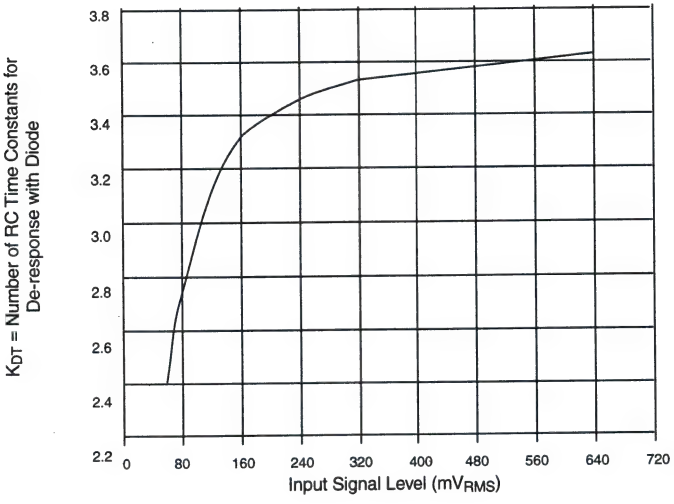


Figure 4: K_{DT} Factor for T_{OFF} vs. Signal Input Amplitude

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480133.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.10 Calculate Signal to Noise Performance

Worst-case S/N calculations depend on calculation of a value "M" using the formula shown below:

$$M = \frac{R3 \times C3_A}{3 \times R2 \times C2_A}$$

substituting example values,

$$M = \frac{510 \times 0.1}{3 \times 200 \times 0.01} = 8.5$$

By substituting this value for M in Figure 5, the minimum required S/N of an in band tone with respect to an adjacent interfering tone can be found. This then has to be increased depending on the input tone amplitude.

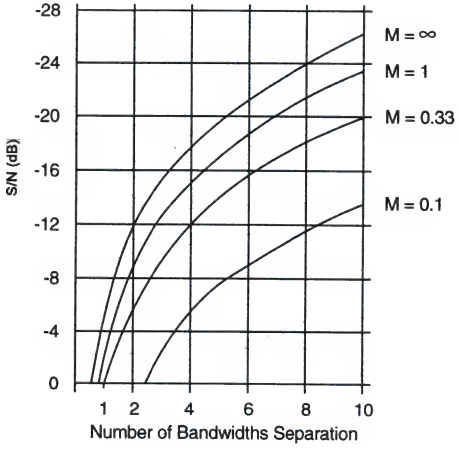


Figure 5: S/N vs. BW Separation

The following formula expresses the reduction in noise immunity as the input signal approaches the detect filter sensitivity V_{TH}.

$$\text{required } \frac{S}{N} = 20\log\left(\frac{V_{IN}}{V_{IN} - V_{TH}}\right) + \frac{S}{N}_{\text{Figure 5}}$$

If this S/N is better than required for the application, $R3 \times C3_A$ can be reduced, or the operating bandwidth can be increased to obtain a faster tone detection time.

If the S/N performance is not adequate, the operating bandwidth can be reduced toward the MUBW, or $R3C3_A$ can be increased to improve S/N performance at the expense of slower response time.

5.11 Calculate C4 for 30° Phase Shift

Capacitor C4 is used to phase shift the input to the VCO commutating filter by 30°, thereby shifting the sampling clocks by the same amount. This enables the Detect sampling filter to sample and integrate at the maximum and minimum of the input tone.

$$C4 = \frac{\tan(30°)}{2\pi \times f_0 \times R_V} \approx \frac{0.092}{f_0 \times R_V} \approx 164pF$$

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480133.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin (wrt V_{SS})	-0.3	V_{DD} + 0.3	V
Current			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
Max. Output Switch Load Current		10	mA
P/LH/DW Package			
Device Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-40	85	°C
Operating Temperature	-30	85	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD} - V_{SS})		2.7	3.3/5.0	5.5	V
Operating Temperature		-30		85	°C

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480133.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0 V @ T_{AMB} = 25°C
Load resistance on decoder output = 20kΩ.

	Notes	Min.	Typ.	Max.	Units
Static Parameters					
I_{DD}			1.0		mA
Amplifier Input Impedance		160	200		kΩ
Digital Output Impedance			500	1000	Ω
Analog Output Impedance			1000	1200	Ω
Dynamic Parameters					
Input Signal					
Frequency		40		20,000	Hz
Lowest Must Detect Level	1		30		mV_{RMS}
Highest Will Not Detect Level	1		20		mV_{RMS}
Highest Will Not Detect $f_0/2$	1, 2		30 790		dB mV_{RMS}
Highest Will Not Detect $5(f_0)$	1, 2		20 250		dB mV_{RMS}
VCO					
Frequency	3	120		120,000	Hz
Frequency Stability			100 5000		ppm/°C ppm/V
BW Limiter					
BW Range		2		10	$\%f_0$
Amplifier					
Open Loop Gain			60		dB
GBWP			1.0		MHz
Closed Loop Gain			0		dB
Detect Commutating Filter					
Sensitivity (V_{TH})	1		25		mV_{RMS}

Operating Characteristics Notes:

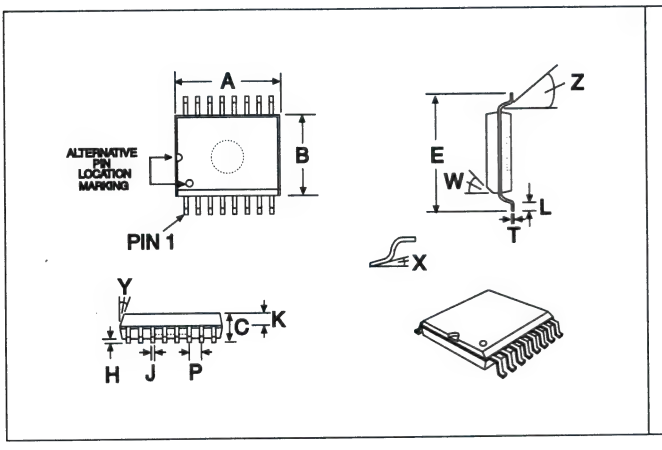
1. Multiply by V_{DD} /5V for other supply values.
2. The reference level is V_{TH}. The following formula converts dB to mV_{RMS}.

$$mV_{RMS} = 10^{(dB/20)} \times V_{TH}$$

3. Observing pins 13, 14, or 15 (DW/J package) will cause a frequency shift due to additional loading. If tuning center frequency by observing oscillator, design in a buffer amplifier between pin 15 and probe/calibration point and tune with no input signal. Otherwise, tune by observing detect output band edges while sweeping input signal. VCO center frequency is $6(f_0)$ at pin 15 while it is $3(f_0)$ at pins 13 and 14.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20480133.003
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

6.2 Packaging

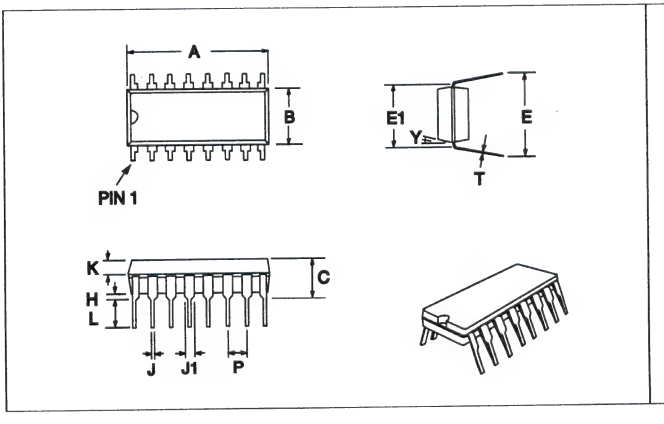


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin SOIC Mechanical Outline: *Order as part no. MX105ADW*



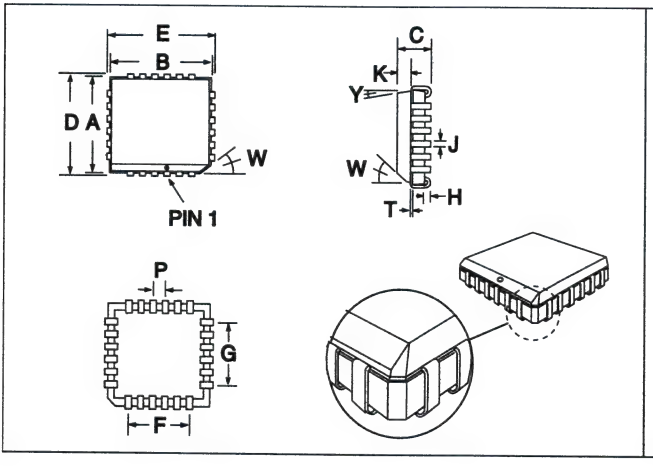
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7e	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 16-pin PDIP Mechanical Outline: *Order as part no. MX105AP*

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc.# 20480133.003



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 24-pin PLCC Mechanical Outline: *Order as part no. MX105ALH*

© 1997 MX-COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc.# 20480133.003
All trademarks and service marks are held by their respective companies.

Technical Specifications

Digital Control Amplifier IC's

Device	Description	Page
MX019	Quad Digitally Controlled Amplifier	31
MX029	Dual Digitally Controlled Amplifier	43

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX019

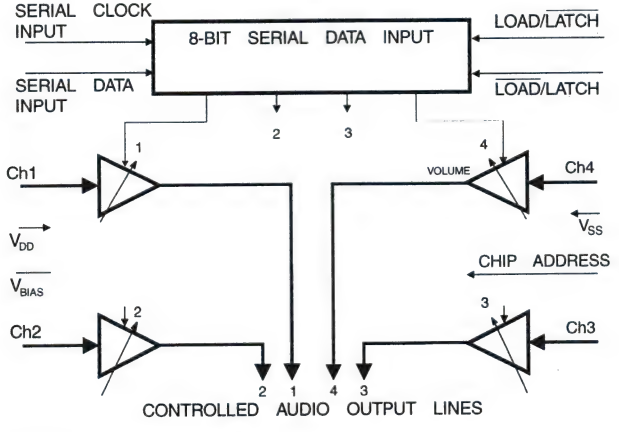
Quad Digital Control Amplifier

FEATURES

- 4 Digitally Controlled Amplifiers
- 15 Gain/Attenuation Steps
- 3 Amplifiers
  ± 3dB Range in 0.43dB Steps
- 1 'Volume' Amplifier
  ±14dB Range in 2dB Steps
- 8-Bit Serial Data Control
- Output Mute Function

APPLICATIONS

- Gain Control Applications
  Audio
  Data
- Telecommunications, Radio, & Industrial Applications



The MX019 Digitally Adjustable Amplifier Array replaces trimmer potentiometers and volume controls in Cellular, LMR, Telephony and Communication applications where voice or data signals need adjustment.

The MX019 is a single-chip LSI consisting of four digitally controlled amplifier stages, each with 15 distinct gain/attenuation steps. Control of each individual amplifier is by an 8-bit serial data stream. Three of the amplifier stages offer a ±3dB range in steps of 0.43dB, while the remaining amplifier offers a ±14dB range in steps of 2dB, and is suggested for volume control applications. Each amplifier includes a 16th 'Off' state which, when applied, mutes the output audio from that channel. This array uses a Chip Select input to select one of two MX019s in a system. The MX019 uses the host microprocessor to digitally control the set-up of all audio levels during development, production/calibration, and operation. Such applications include:

1. Control, adjustment, and set-up of communications equipment by an Intelligent ATE without manual intervention – eg. Deviation, Microphone and L/S Levels, RX Audio Level etc.
2. Automatic Dynamic Compensation of drift caused by variations in temperature, linearity, etc.
3. Fully automated servicing and re-alignment.

The MX019 is a low-power, single 5-volt CMOS device available in 24-pin TSSOP (MX019TN), 16-pin SOIC (MX019DW), 16-pin CDIP (MX019J) and 16-pin PDIP (MX019P) package versions.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20480077.005
All trademarks and service marks are held by their respective companies

CONTENTS

Section **Page**

1. Block Diagram **9-33**

2. Signal List **9-34**

3. External Components **9-35**

4. General Description **9-35**

4.1 Control Data and Timing 9-35

4.1.1 Data Loading 9-35

4.1.2 Timing 9-37

5. Application **9-38**

6. Performance Specification **9-38**

6.1 Electrical Performance 9-38

6.1.1 Absolute Maximum Ratings 9-38

6.1.2 Operating Limits 9-38

6.1.3 Operating Characteristics 9-39

6.2 Packaging 9-40

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480077.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

1. Block Diagram

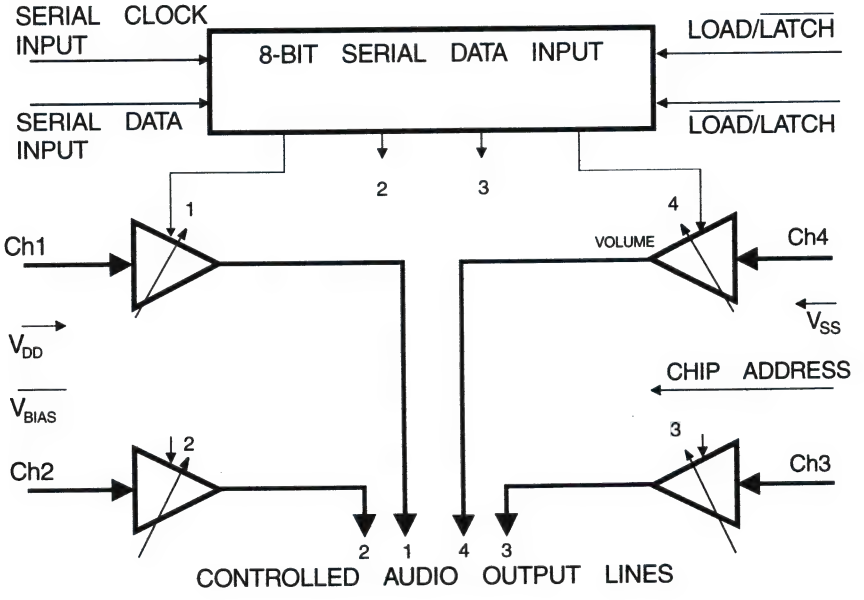


Figure 1: Device Block Diagram

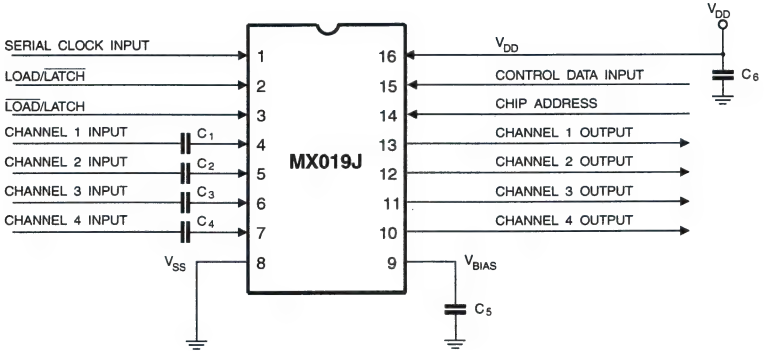
© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies
Doc. # 20480077.005

2. Signal List

Pin No.		Name	Description
J/P DW	TN		
1	1	Serial Clock	This external clock pulse input is used to "clock in" the Control Data. See Figure 3. This input has an internal 1MΩ pullup resistor.
2	2	Load/$\overline{\text{Latch}}$	This input governs the loading and execution of the control data. During serial data loading this input should be kept at a logical '0' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '0 - 1 - 0' to latch the new data in. Data is executed on the falling edge of the strobe. If the $\overline{\text{Load}}$/Latch input is used this pin should be left open circuit. This input has an internal 1MΩ pullup resistor.
3	4	$\overline{\text{Load}}$/Latch	This inverted Load/$\overline{\text{Latch}}$ input governs the loading and execution of control data. During serial data loading this input should be kept at a logical '1' to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded, this input should be strobed '1' - '0' - '1' to latch the new data in. Data is executed on the rising edge of the strobe. If the Load/$\overline{\text{Latch}}$ input is used this pin should be left open circuit. This input has an internal 1MΩ pulldown resistor.
4	5	Ch1 Input	**Analog Inputs :**
5	6	Ch2 Input	These individual amplifier inputs are self-biasing; a.c. input analog signals must be
6	7	Ch3 Input	capacitively coupled to these pins, as shown in Figure 2. Note that amplifiers
7	8	Ch4 Input	Ch1 to Ch4 are 'inverting amplifiers.'
8	12	V_{SS}	Negative supply rail (GND).
9	13	V_{BIAS}	The output of the on-chip bias circuitry, held at $V_{DD}/2$. This pin should be decoupled to V_{SS} as shown in Figure 2.
10	14	Ch4 Output	**Controlled Analog Outputs :**
11	17	Ch3 Output	These are individual "Gain Controlled" amplifier outputs. Ch1 to Ch3 range from -3dB
12	18	Ch2 Output	to +3dB in 0.43dB steps, Ch4 can be utilized as a volume control, ranging from -14dB
13	19	Ch1 Output	to +14dB in 2.0dB steps. In the "OFF" mode there is no output from the selected amplifier.
14	20	Chip Address	A logic input to select one of two MX019 ICs in a system (see Table 1). This input has an internal 1MΩ pulldown resistor.
15	23	Control Data Input	Operation of the 4 amplifier channels (Ch1 – Ch4) is controlled by the 8 bits of data entered serially at this pin. The data is entered (bit 7 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Table 1, Table 2 and Figure 3. This input has an internal 1MΩ pullup resistor.
16	24	V_{DD}	Positive supply rail. A single +5V power supply is required.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480077.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

3. External Components



C1 to C4	0.1µF	± 20%
C5	1.0µF	± 20%
C6	1.0µF	± 20%

Figure 2: Recommended External Components

Notes:

1. Channel Amplifiers 1 to 4 are inverting amplifiers.
2. Analog input capacitors C1 to C4 are only required for a.c. input signals, d.c. input signals do not require these components.

4. General Description

4.1 Control Data and Timing

The gain of each amplifier block (Channel 1 to Channel 4) in the MX019 is set by a separate 8-bit data word (bit 7 to bit 0). This 8-bit word, consisting of 4 Address bits (bit 7 to bit 4) and 4 Gain Control bits (bit 3 to bit 0), is loaded to the Control Data Input in serial format using the external data clock.

4.1.1 Data Loading

The 8-bit data word is loaded bit 7 first and bit 0 last.

Bit 7 must be a logic "1" to address the chip.

If bit 7 in the word is a logic "0" that 8-bit word will not be executed. The Chip Address input permits the use of two devices in a system by indicating to the chip what its address is, a "1" or a "0." Bit 6 in the address section of the control word is then used to select which device is being controlled. Figure 3 shows the timing information required to load and operate this device.

Data is loaded to the MX019 on the rising edge of the Serial Clock. Loaded data is executed on the falling (rising) edge of the Load/$\overline{\text{Latch}}$ ($\overline{\text{Load}}$/Latch) pulse.

Table 1 shows the format of each 4-bit Address word, Table 2 shows the format of each Gain Control word with Figure 3 describing the data loading operation and timing.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480077.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Bit 7 MSB	Bit 6	Bit 5	Bit 4 LSB	Channel Address	Chip Address	Chip Number
1	0	0	0	1	0	Chip 1
1	0	0	1	2	0	
1	0	1	0	3	0	
1	0	1	1	4	0	
1	1	0	0	1	1	Chip 2
1	1	0	1	2	1	
1	1	1	0	3	1	
1	1	1	1	4	1	

Table 1: Address Bits Format

Bit 3 MSB	Bit2	Bit 1	Bit 0 LSB	Stage 1, 2, 3 (0.43dB)	Stage 4 (2.0dB)
0	0	0	0	OFF	OFF
0	0	0	1	-3.0	-14.0dB
0	0	1	0	-2.571	-12.0
0	0	1	1	-2.143	-10.0
0	1	0	0	-1.714	-8.0
0	1	0	1	-1.286	-6.0
0	1	1	0	-0.857	-4.0
0	1	1	1	-0.428	-2.0
1	0	0	0	0	0
1	0	0	1	0.428	2.0
1	0	1	0	0.857	4.0
1	0	1	1	1.286	6.0
1	1	0	0	1.714	8.0
1	1	0	1	2.143	10.0
1	1	1	0	2.571	12.0
1	1	1	1	3.0	14.0

Table 2: Gain Control Bits Format

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies
Doc. # 20480077.005

4.1.2 Timing

Timing (Figure 3)		Min.	Typ.	Max.	Units
Serial Clock "High" Pulse Width	(t_{PWH})	250			ns
Serial Clock "Low" Pulse Width	(t_{PWL})	250			ns
Data Set-up Time	(t_{DS})	150			ns
Data Hold Time	(t_{DH})	50.0			ns
Load/Latch Set-up Time	(t_{LL})	250			ns
Load/Latch Pulse Width	(t_{LLW})	150			ns
Load/Latch Delay	(t_{LLD})	200			ns
Load/Latch Over	(t_{LLO})			50.0	ns
Serial Data Clock Frequency				2.0	MHz

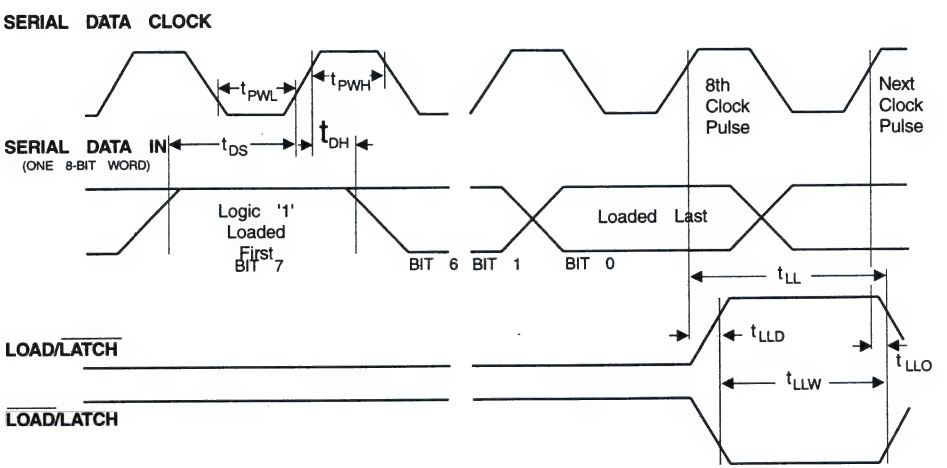


Figure 3: Serial Control Data Loading Diagram

5. Application

To avoid excess noise and instability you should take note of the following:

1. A noisy or badly regulated power supply can cause instability and/or variance of selected gains.
2. Care should be taken on the design and layout of the printed circuit board.
3. All external components (Figure 2) should be kept close to the MX019 package.
4. Inputs and outputs should be shielded wherever possible.
5. Tracks should be kept short.
6. Analog tracks should not run parallel to digital tracks.
7. A "Ground Plane" connected to V_{SS} will assist in eliminating external pick-up on the channel input and output pins.
8. Do not run high-level output tracks close to low-level input tracks.

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply Voltage	-0.3	7.0	V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3	(V_{DD} + 0.3)	V
Current			
V_{DD}		±30	mA
V_{SS}		±30	mA
Any other pins		±20	mA
J/P/DW Packages			
Total Device Dissipation @ T_{AMB} 25°C		800	mW
Derating above 25°C		10	mW/°C above 25°C
TN Packages			
Total Device Dissipation @ T_{AMB} 25°C		500	mW
Derating above 25°C		9	mW/°C above 25°C
Operating Temperature	-40	85	°C
Storage Temperature	-55	125	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	Typ.	Max.	Units
V_{DD}	4.5	5.0	5.5	V
Operating Temperature	-40		85	°C

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies
Doc. # 20480077.005

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C
Audio Level 0dB ref. = 775mV_{RMS}, Amplifier Gain Set = 0dB

	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Current			1.5		mA
Dynamic Values					
Control Functions					
Input Logic '1'		3.5			V
Input Logic '0'				1.5	V
Digital Input Impedances		0.5	1.0		MΩ
Amplifier Stages (General)					
Bandwidth (-3dB)		20.0			kHz
Output Impedance			1.0		kΩ
Total Harmonic Distortion	1		0.35	0.5	%
Output Noise Level (per stage)	2		180.0	400.0	μV_{RMS}
Onset of Clipping	3		1.73		V_{RMS}
Gain Variation	4			0.1	dB
Interstage Isolation			60.0		dB
"Trimmer" Stages (Ch1 – Ch3)					
Gain		-3.0		+3.0	dB
Gain per Step (15 in No.)			0.43		dB
Step Error				0.2	dB
Input Impedance		100.0			kΩ
"Volume" Stage (Ch4)					
Gain		-14.0		+14.0	dB
Gain per Step (15 in No.)			2.0		dB
Step Error				0.4	dB
Input Impedance		50.0			kΩ

Operating Characteristics Notes:

1. Gain Set 0dB, Input Level 1kHz -3.0dB (549mVrms).
2. With an a.c short-circuit input, measured in a 30kHz bandwidth.
3. See Figure 4.
4. Over the temperature and supply voltage range.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480077.005
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

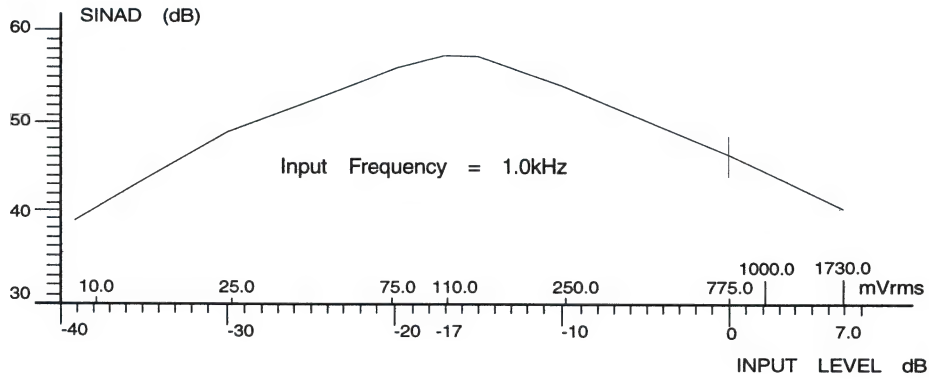
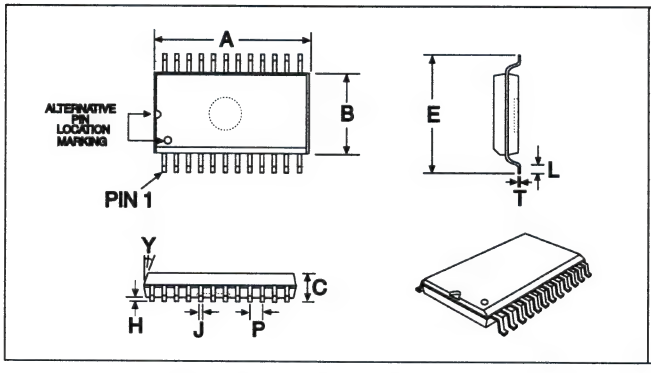


Figure 4: SINAD vs Input Level – Typical Values

6.2 Packaging



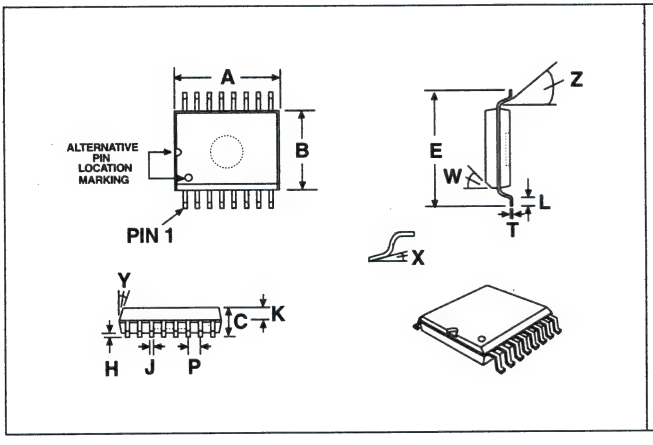
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 24-pin TSSOP Mechanical Outline: Order as part no. MX019TN

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies
Doc. # 20480077.005

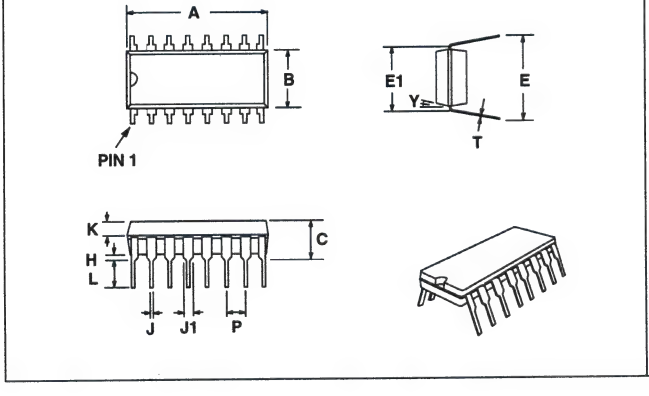


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin SOIC Mechanical Outline: Order as part no. MX019DW



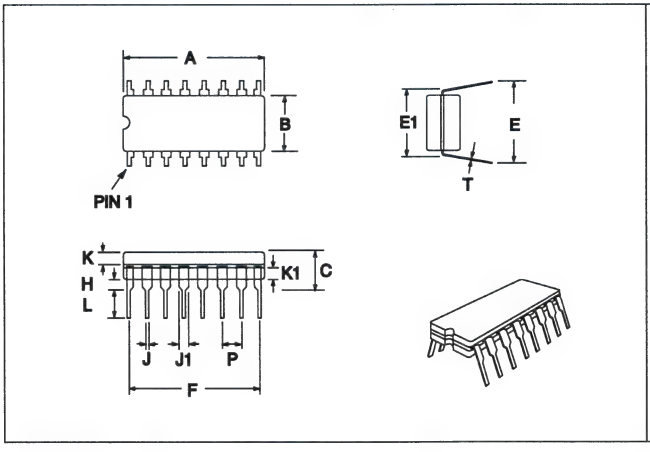
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 16-pin PDIP Mechanical Outline: Order as part no. MX019P

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies
Doc. # 20480077.005



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.753 (19.13)		0.767 (19.48)
B	0.285 (7.24)		0.291 (7.39)
C	0.165 (4.19)		0.230 (5.84)
E	0.370 (9.40)		0.415 (10.53)
E1	0.300 (7.61)		0.317 (8.04)
F		0.70 (17.78)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.053 (1.33)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 16-pin CDIP Mechanical Outline: Order as part no. MX019J

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies
Doc. # 20480077.005

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX029

Dual Digitally Controlled Amplifier

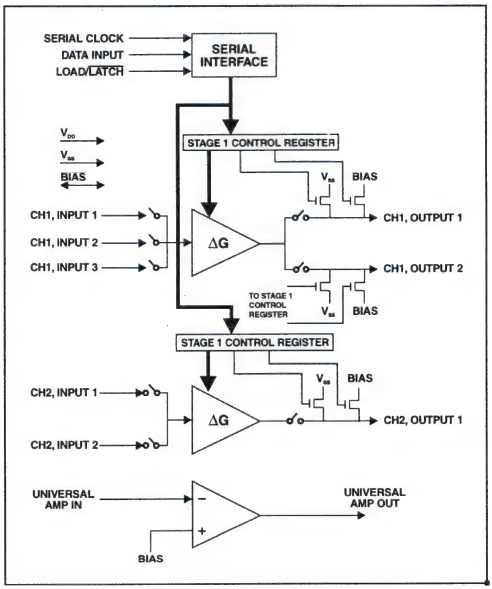
PRELIMINARY INFORMATION

Features

- 2 Digitally Controlled Amplifiers
- ±48dB Gain/Attenuation in 2dB Steps + Mute
- Individual Control with a 14-Bit Serial Word
- Separate Fixed Gain Buffer Amplifier

Applications

- Cellular and LMR Radios
- PABX's, Electronic Mail, TAM's
- Automatic Test Equipment
- Remote Gain Adjustments
- Digitally Set Audio Control Levels



The MX029 Digitally Controlled Amplifier Array replaces audio level controls in radio and wireline communications applications. It is a single-chip LSI circuit comprised of two discrete, digitally controlled gain sections. Each section has 48 distinct gain steps (+/-48dB of range in 2dB steps) plus MUTE.

As shown in Figure 1, both gain stages have switchable inputs. This switching allows for selection of three different input signals on one channel and two on the other channel. One of the channels also has output switching. In addition to two digitally controlled gain stages, there is a general purpose inverting amplifier. The gain of this amplifier is controlled externally via negative feedback. Control of each gain control section is accomplished through the serial interface. All switching is accomplished using controlled rise and fall times, thereby assuring no transients (clicks or pops).

The MX029 requires a single 5-volt supply and is available in the following packages: 16-pin SOIC (MX029DW), 16-pin CDIP (MX029J), and 24-pin TSSOP (MX029TN).

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA.
Doc. # 20480096.007
All trademarks and service marks are held by their respective companies.

CONTENTS

Section **Page**

1. Block Diagram **9-45**

2. Signal List **9-46**

3. External Components **9-47**

4. Application **9-47**

4.1 Recommendations 9-47

5. Control Data and Timing **9-48**

6. Performance Specification **9-50**

6.1 Electrical Performance 9-50

6.1.1 Absolute Maximum Ratings 9-50

6.1.2 Operating Limits 9-50

6.1.3 Operating Characteristics 9-51

6.2 Serial Interface Timing 9-52

6.3 Packaging 9-53

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480096.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

1. Block Diagram

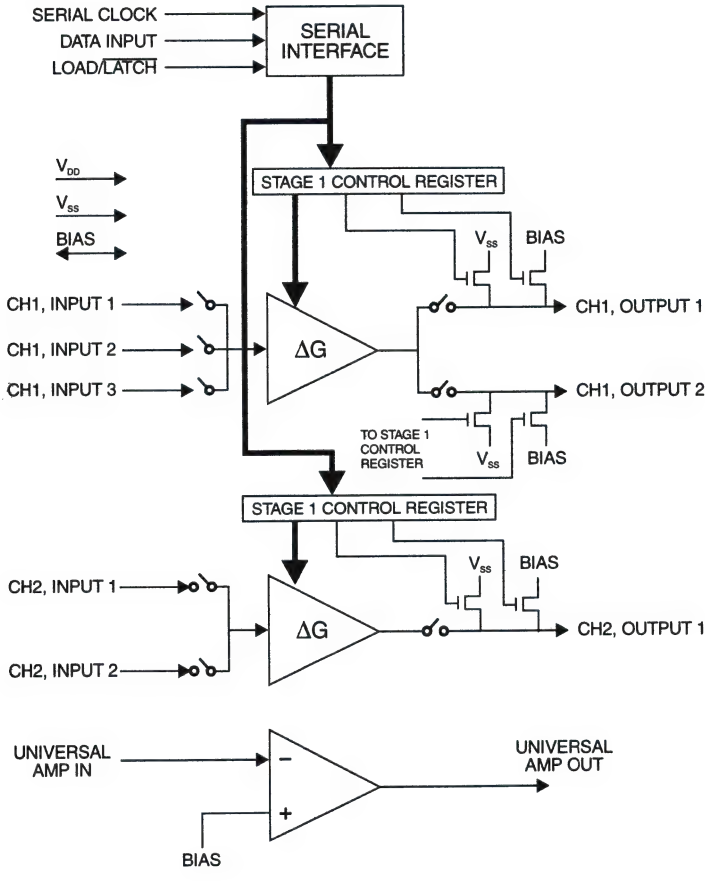


Figure 1: Device Block Diagram

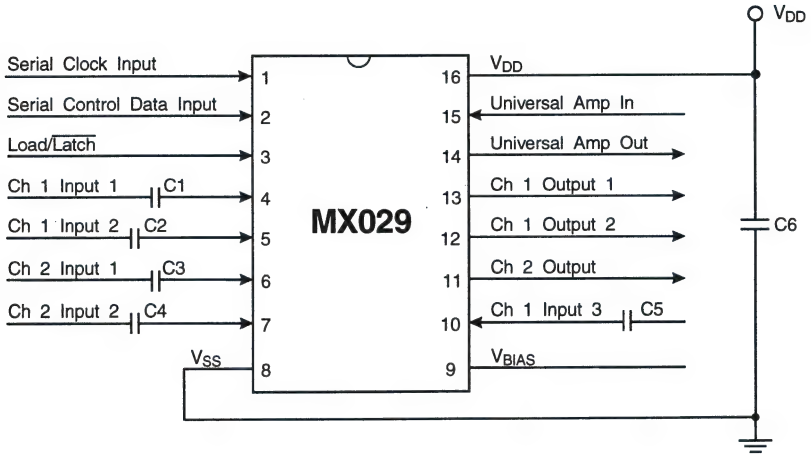
© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480096.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

2. Signal List

Pin No.		Type	Description
J, DW	TN		
1	1	Serial Clock	This external clock input is used to "clock in" the Control Data. See Figure 4 for timing information. This input has an internal 1MΩ pullup resistor.
2	4	Control (Data)	Input: Operation of the two amplifier channels (Ch1 - Ch2) is controlled by the data entered serially at this pin. The data is entered (bit 13 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1-5 and Figure 3. This input has an internal 1MΩ pullup resistor.
3	5	Load/$\overline{\text{Latch}}$	This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical "1" to ensure that data rippling past the latches has no effect. When all 14 bits have been loaded this input should be strobed "1 - 0 -1" to latch the new data in. Data is executed on the rising edge of the strobe.
4	6	Ch 1 Input 1	Analog Input.
5	7	Ch 1 Input 2	Analog Input.
6	8	Ch 2 Input 1	Analog Input.
7	9	Ch 2 Input 2	Analog Input.
8	12	V_{SS}	Negative supply (GND).
9	13	V_{BIAS}	The output of the on-chip bias circuitry, held at $V_{DD}/2$.
10	16	Ch 1 Input 3	Analog Input. Normally used for FSK data.
11	17	Ch 2 Output	Analog Output.
12	18	Ch 1 Output	Analog Output.
13	20	Ch 1 Output	Analog Output.
14	21	Universal Amp Out	Output from general purpose amplifier.
15	23	Universal Amp In	Inverting input to general purpose amplifier.
16	24	V_{DD}	Positive supply rail. A single +5-volt power supply is required.
	2, 3, 10, 11, 14, 15, 19, 22	N/C	No internal connection

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480096.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

3. External Components



C1 to C5	Note 1	0.1µF	±20%
C6		1.0µF	±20%

Notes:

1. Analog input capacitors C1 to C5 are only required for a.c. input signals; d.c. input signals do not require these components.

Figure 2: Recommended External Components

4. Application

4.1 Recommendations

To avoid noise and instability the following practices are recommended:

1. Use a clean, well-regulated power supply.
2. Keep leads short.
3. Inputs and outputs should be shielded wherever possible.
4. Analog tracks should not run parallel to digital tracks.
5. A "Ground Plane" connected to Vss will assist in eliminating external pick-up on the channel input and output pins.
6. Avoid running High Level Outputs adjacent to Low Level Inputs.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480096.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

5. Control Data and Timing

The gain and I/O signal path for each section (Channels 1 and 2) is set individually by a 14-bit data word (D0 to D13). Data is loaded on the rising edge of the Serial Clock. Loaded data is executed on the rising edge of the Load/Latch pulse. The 14-bit word consists of 1 channel address bit (D7) for selection of the channel to be programmed, 6 bits for setting the gain/attenuation level (D8-D13), 3 bits for input selection (D4 and D6), and 4 bits for output settings (D0-D3). This format is illustrated in Figure 3.

D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ΔG SET	ΔG SET	ΔG SET	ΔG SET	ΔG SET	ΔG SET	CHAN ADDR	IN SEL	IN SEL	IN "SEL	OUT SET	OUT SET	OUT SET	OUT SET
GAIN/ATTN LEVEL						CHANNEL ADDRESS	INPUT SELECT			OUTPUT SETTINGS			

Figure 3: Data Word Format

Tables 1-5 show how the data word is used to control channel selection, gain/attenuation, input selection and output settings, respectively.

To calculate the data word used to control channel gain/attenuation use the following formula:

$$25 + \left(\frac{\text{gain dB}}{2}\right) = \text{The decimal equivalent of binary Data Word}$$

For example: using a gain of +34dB,

$$25 + \left(\frac{+34\text{dB}}{2}\right) = 42 = \$2A = \frac{\text{D13-D8}}{101010}$$

D13	D12	D11	D10	D9	D8	GAIN SET (dB)
0	0	0	0	0	0	MUTE
0	0	0	0	0	1	-48
0	0	0	0	1	0	-46
0	0	0	0	1	1	-44
0	1	1	0	0	1	0
1	0	1	1	1	0	+42
1	0	1	1	1	1	+44
1	1	0	0	0	0	+46
1	1	0	0	0	1	+48
1	1	0	0	1	0	+48
1	1	0	0	1	1	+48

Table 1: Gain/Attenuation Level

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480096.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

D7	Channel Selected
0	1
1	2

Table 2: Channel Selection

D6	D5	D4	INPUTS SELECTED
0	0	0	NONE
0	0	1	1
0	1	0	2
0	1	1	1 & 2
1	0	0	3
1	0	1	1 & 3
1	1	0	2 & 3
1	1	1	1, 2, & 3

Table 3: Input Select

D3	D2	OUTPUT 2 SETTINGS
0	0	high impedance
0	1	amplifier output
1	0	V_{SS}
1	1	V_{BIAS}

Table 4: Settings for Output 2 (Ch 1 only)

D1	D0	OUTPUT 1 SETTINGS
0	0	high impedance
0	1	amplifier output
1	0	V_{SS}
1	1	V_{BIAS}

Table 5: Settings for Output 1

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480096.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Max.	Units
Supply (V_{DD}-V_{SS})		-0.3	7.0	V
Voltage on any pin to V_{SS}		-0.3	(V_{DD} + 0.3)	V
Current				
V_{DD}		-30	30	mA
V_{SS}		-30	30	
Any other pin		-20	20	mA
Total Allowable Power Dissipation at T_{AMB} 25°C			800	mW Max.
Derating above T_{AMB} 25°C			10	mW/°C above T_{AMB} 25°C
Operating temperature		-40	85	°C
Storage temperature		-55	125	°C

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	Typ.	Max.	Units
V_{DD}	4.5	5.0	5.5	V
Operating temperature	-40		85	°C

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480096.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C
Audio level 0dB ref. = 775mV_{RMS}

	Notes	Min.	Typ.	Max	Units
Current:					
All Stages Operating			3.0		mA
Digital Inputs					
Input Logic "1"		3.5			V
Input Logic "0"				1.5	V
Digital Input Impedance		0.5	1.0		MΩ
Gain Control Amplifier Stages					
Bandwidth (-3dB)	1	3.3			kHz
Output Impedance			1.0	2.0	kΩ
Total Harmonic Distortion	2, 4		0.35	0.5	%
Interstage Isolation			60.0		dB
Gain/Attenuation		46	48		dB
Gain/Attenuation Steps (48 total)			2.0		dB
Step Error				0.4	dB
Input Impedance		50.0			kΩ
Input Referred Offset Voltage (V_{IOS})			10		mV
Universal Amplifier					
Bandwidth (-3dB)	3	10			kHz
Output Impedance			1.0	2.0	kΩ
Total Harmonic Distortion	3		0.35	0.5	%
Open Loop DC Gain			60		dB

Notes:

1. Gain set to maximum (+48 dB)
2. Gain Set 0dB. Input Level 1kHz -3.0dB (549mV_{rms})
3. Gain externally set to 10 dB.
4. With a 100k load on the output.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480096.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

6.2 Serial Interface Timing

	Parameter	Min.	Typ.	Max.	Units
t_{PWH}	Serial Clock "High" Pulse Width	250			ns
t_{PWL}	Serial Clock "Low" Pulse Width	250			ns
t_{DS}	Data Set-up Time	150			ns
t_{DH}	Data Hold Time	50			ns
t_{LLH}	Load/Latch Hold Time	0			ns
t_{LLS}	Load/Latch Set-up Time	250			ns
t_{LLW}	Load/Latch Pulse Width	150			ns
	Serial Data Clock Frequency			2.0	MHz

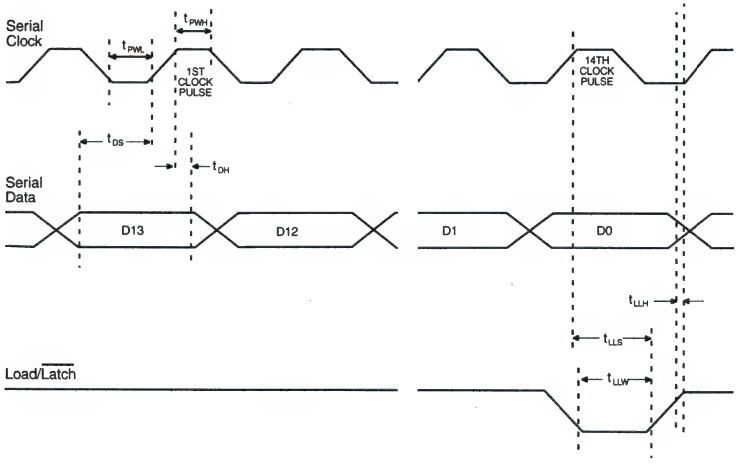
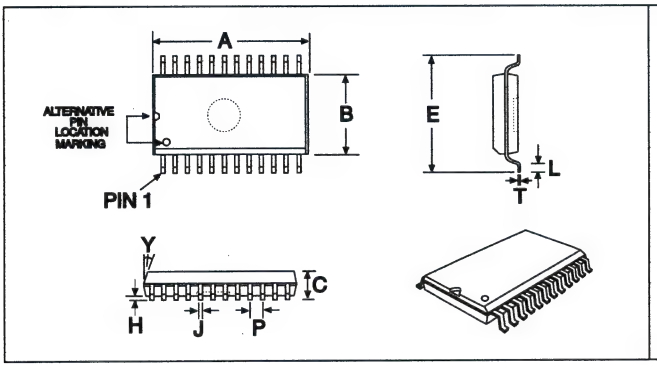


Figure 4: Serial Timing Diagram

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480096.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

6.3 Packaging

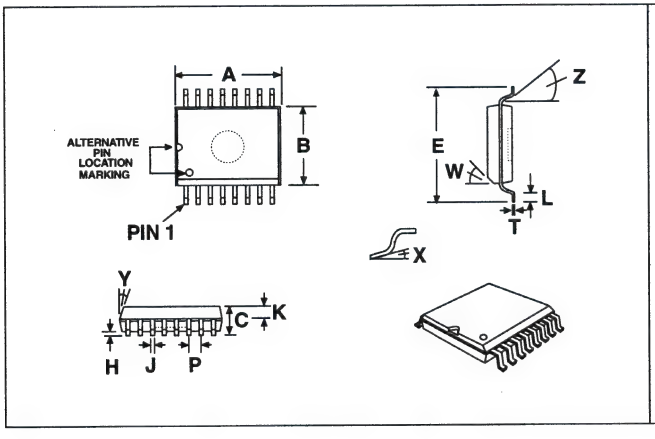


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 5: 24-pin TSSOP Mechanical Outline: Order as part no. MX029TN



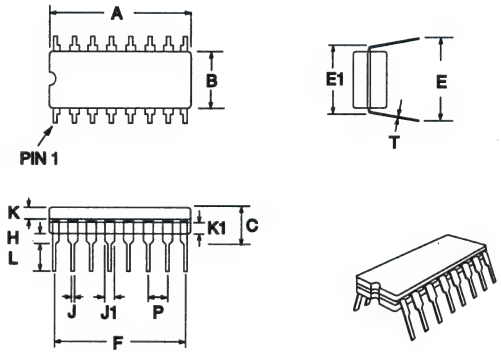
Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 16-pin SOIC Mechanical Outline: Order as part no. MX029DW

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20480096.007
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.753 (19.13)		0.767 (19.48)
B	0.285 (7.24)		0.291 (7.39)
C	0.165 (4.19)		0.230 (5.84)
E	0.370 (9.40)		0.415 (10.53)
E1	0.300 (7.61)		0.317 (8.04)
F		0.70 (17.78)	
H		0.020 (0.51)	
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.053 (1.33)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.200 (5.08)
P		0.100 (2.54)	
T	0.0098 (0.249)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 16-pin CDIP Mechanical Outline: Order as part no. MX029J

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA.
All trademarks and service marks are held by their respective companies.
Doc. # 20480096.007

Technical Specifications

Digitally Controlled Analog I/O Processor IC

Device	Description	Page
MX839	Digitally Controlled Analog I/O Processor	57

MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX839

Digitally Controlled Analog I/O Processor

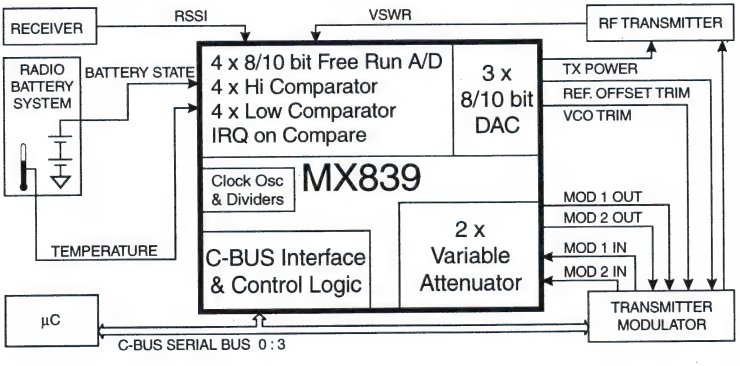
ADVANCE INFORMATION

Features

- **4 input intelligent 8/10 bit A/D monitoring subsystem**
  - **4 High and 4 Low Comparators**
  - **External IRQ Generator**
  - **Free Running Operation**
- **Three 8/10 bit DACs**
- **Two Variable Attenuators**
- **Selectable A/D Clock Frequencies**
- **Full Control via 4-wire Serial Interface**
- **Low Power 3.3V/5.0V Operation**

Applications

- **PCS, Cellular, LMR, Wireless Transceivers, and General Purpose**
- **Monitor and Control:**
  RSSI, Battery State, Temperature, VSWR, and Error Voltages
- **Digital Trim and Calibration:**
  VCOs, TCXO, Power Output, Bias, Current, IF Gain, Deviation, Modulation Depth, and Baseband Gain



The MX839 is a low power CMOS µC peripheral device which provides digitally controlled calibration, trimming, and monitoring functions for PCS, cellular, LMR, wireless transceivers, and general purpose applications.

Featuring a four input intelligent 8/10 bit A/D monitoring subsystem, an interrupt generator, three 8/10 bit DACs, and two variable attenuator functions, the MX839 automatically monitors, produces, and trims up to nine analog signals via a simple four wire serial control bus. The free running A/D intelligent monitoring subsystem includes independent high and low limit comparators for each of four analog input signals which can be configured to generate external µC interrupts.

The MX839's high level of integration reduces end product parts count, component size, and software complexity. MX839 digital trimming functions also reduce manufacturing costs by eliminating manual trimming operations.

Featuring a 3.3/5.0V supply range, the MX839 is available in 24-pin SSOP (MX839DS), 24-pin SOIC (MX839DW), and 24-pin PDIP (MX839P) packages..

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480164.001

CONTENTS

Section **Page**

1. Block Diagram **9-59**

2. Signal List **9-60**

3. External Components **9-61**

4. General Description **9-62**

4.1 Variable Attenuators 9-62
4.2 Digital to Analog Converters 9-62
4.3 Analog to Digital Converter and A/D Clock Generator 9-62
4.4 Magnitude Comparators and Interrupt Request 9-63
4.5 Software Description 9-63
4.6 Read Only Registers (8-Bit and 16-Bit) 9-65
4.7 Write Only Register Description 9-66
4.8 Read Only Register Description 9-69

5. Performance Specification **9-70**

5.1 Electrical Performance 9-70
5.2 Packaging 9-74

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480164.001

1. Block Diagram

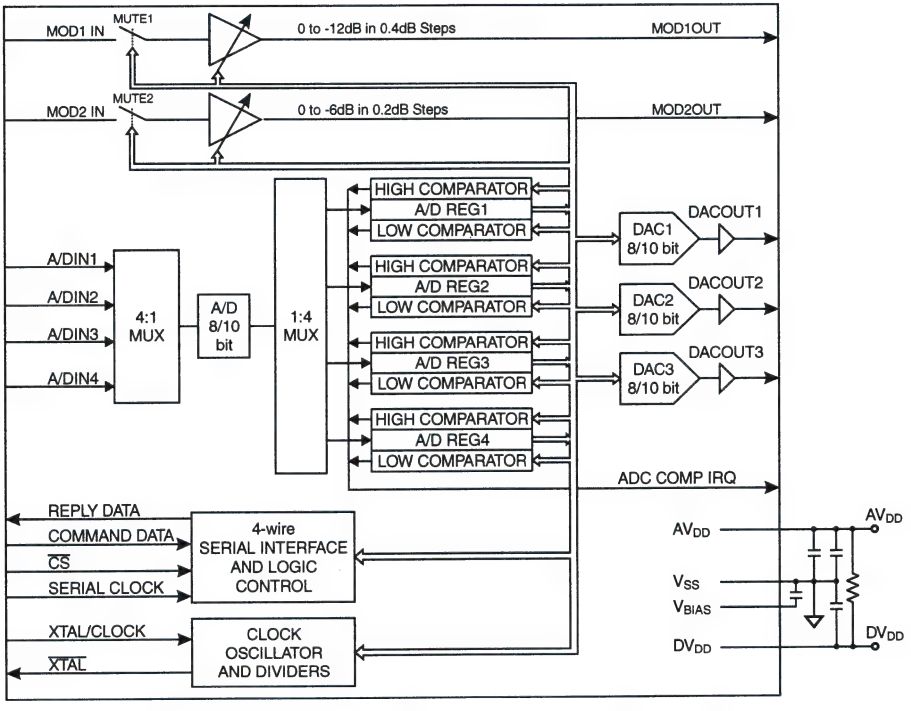


Figure 1: Block Diagram

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. Signal List

Pin No.	Name	Type	Description
1	$\overline{XTAL}$	output	The inverter output of the on-chip oscillator.
2	XTAL/CLOCK	input	The input to the on-chip oscillator, for external Xtal circuit or clock.
3	SERIAL CLOCK	input	The 'C-BUS' serial clock input. This clock, produced by the µC, is used for transfer timing of commands and data to and from the device. See Figure 4.
4	COMMAND DATA	input	The 'C-BUS' serial data input from the µC. Data is loaded into this device in 8-bit bytes, MSB (B7) first, and LSB (B0) last, synchronized to the SERIAL CLOCK. See Figure 4.
5	REPLY DATA	output	The 'C-BUS' serial data output to the µC. The transmission of REPLY DATA bytes is synchronized to the SERIAL CLOCK under the control of the $\overline{CS}$ input. This tri-state output is held at high impedance when not sending data to the µC. See Figure 4.
6	$\overline{CS}$	input	The 'C-BUS' data loading control function. This input is provided by the µC. Data transfer sequences are initiated, completed or aborted by the $\overline{CS}$ signal. See Figure 4.
7	$\overline{IRQ}$	output	This output indicates an interrupt condition to the µC by going to a logic '0'. This is a 'wire-ORable' output, enabling the connection of up to 8 peripherals to 1 interrupt port on the µC. This pin has a low impedance pulldown to logic '0' when active and a high-impedance when inactive. An external pullup resistor is required. The conditions that cause interrupts are indicated in the IRQ FLAG register and are effective if not disabled.
8	A/DIN1	input	Analog to digital converter input 1 (A/D1)
9	A/DIN2	input	Analog to digital converter input 2 (A/D2)
10	A/DIN3	input	Analog to digital converter input 3 (A/D3)
11	A/DIN4	input	Analog to digital converter input 4 (A/D4)
12	V_{SS}	power	Negative supply (ground) for both analog and digital supplies.
13	V_{BIAS}	output	An analog bias line for the internal circuitry, held at $AV_{DD}/2$. This pin must be bypassed by a capacitor mounted close to the device pins.
14	N/C		No internal connection. Do not make any connection to this pin.
15	DACOUT1	output	Digital to analog converter No. 1 output (DAC1)
16	DACOUT2	output	Digital to analog converter No. 2 output (DAC2)
17	DACOUT3	output	Digital to analog converter No. 3 output (DAC3)
18	N/C		No internal connection. Do not make any connection to this pin.
19	AV_{DD}	power	Positive analog supply. Analog levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.
20	MOD1 IN	input	Input to MOD1 variable attenuator.
21	MOD2 IN	input	Input to MOD2 variable attenuator.
22	MOD1	output	Output of MOD1 variable attenuator.
23	MOD2	output	Output of MOD2 variable attenuator.
24	DV_{DD}	power	Positive digital supply. Digital levels and voltages are dependent upon this supply. This pin should be bypassed to V_{SS} by a capacitor.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. External Components

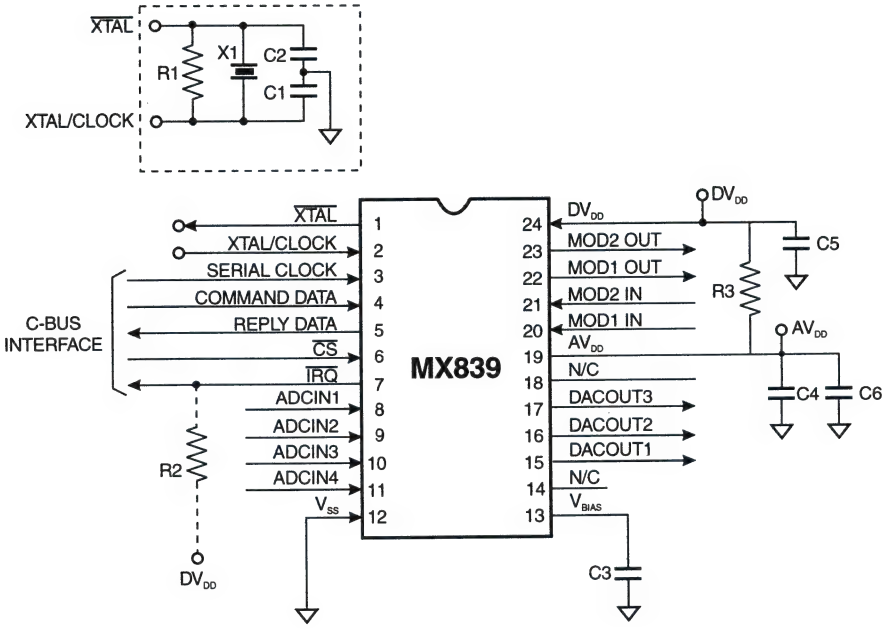


Figure 2: Recommended External Components

R1		1MΩ	±5%
R2		22kΩ	±10%
R3	Note 1	10Ω	±10%
C1		22pF	±20%
C2		22pF	±20%
C3		0.1µF	±20%

C4	Note 1	0.01µF	±20%
C5		0.1µF	±20%
C6	Note 1	10.0µF	±20%
X1	Note 2, 3	TBD	±100ppm

Table 1: Recommended External Components

Notes:

1. These values should be determined in regard to the amount of supply filtering required for D/A outputs.
2. A crystal or an external clock input to Pin 2 can be used between TBD Hz and TBD Hz. Internal programmable dividers are then set to accommodate that frequency.
3. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4. General Description

The device comprises four groups of related functions: variable attenuators, digital to analog converters, a multiplexed analog to digital converter with multiplexer, clock generator and four 8-bit magnitude comparators with variable reference levels. These functions are all controlled by the 'C-BUS' serial interface and are described below:

4.1 Variable Attenuators

The two variable attenuators have a range of 0 to -12dB and 0 to -6dB respectively and may be controlled independently.

4.2 Digital to Analog Converters

Three DACs are provided with default resolutions of 8 bits, which are defined at the initial chip reset. In this mode the 'C-BUS' data is transferred in a single byte. An option is provided to define any one or more of the DAC resolutions to be 10 bits, then the DAC requires the transfer of two 'C-BUS' data bytes.

The upper and lower DAC reference voltages are defined internally as AV_{DD} and V_{SS} respectively. The output voltage is expressed as:

$$V_{OUT} = AV_{DD} \times (DATA / 2^n) \quad [Volts]$$

Where, n is the DAC resolution (8 or 10 bits) and DATA is the decimal value of the input code. For example: n = 8 and binary code = 11111111 therefore DATA = 255

$$V_{OUT} = AV_{DD} \times (255 / 256) \quad [Volts]$$

Any one of the three DAC input latches may be loaded by sending an address/command byte followed by one or two data bytes to the 'C-BUS' interface. The data is then latched and the static voltage is updated at the appropriate output.

When a DAC is disabled its output is defined as open-circuit.

4.3 Analog to Digital Converter and A/D Clock Generator

A single successive approximation A/D is provided with four multiplexed inputs. In order to minimize the sampling time of each input channel, a Sample and Hold circuit has not been included at the input of the A/D.

For the sampling to be accurate the input signal should not change significantly during the conversion time. Since the typical application is for the monitoring of slowly changing control voltages this should not present any problems. The maximum signal 'linear rate of change', 'S', can be quantified by the following expression (for a maximum 1 bit error):

$$S = AV_{DD} \times f_{A/D\_CLK} / (2^n \times 1000 \times (n + 2)) \quad [mV/\mu s]$$

Where n is the selected resolution and f_{A/D_CLK} is the internal A/D clock frequency.

Two conversion modes are provided. The default allows a one-off conversion to be made of each active input channel, at which point the internal clock is disabled. The second mode continually converts all active input channels, cycling around each in sequence.

The programmable clock generator is intended to be flexible, making use of an external system clock signal or a dedicated crystal. This clock signal is scaled to provide the internal A/D clock frequency (f_{A/D_CLK}). The user has full control of the frequency scaling factor and this should be chosen such that the input clock frequency, at the XTAL/CLOCK pin, divided by this factor is no more than 1MHz.

The output data word can be selected to 8 or 10 bit resolution (8 bit resolution is set by default).

The microcontroller is required to wait during the conversion time, T_{CONV_MAX} (Figure 3), before issuing a 'READ A/D DATAx' command. If this is not done, then the converted data returned via 'C-BUS' will be the result of the previous conversion on the selected channel. It is possible for the data conversion rate to exceed the reply rate on 'C-BUS'. In such a case, the data returned will be the result of the most recent conversion completed.

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480164.001

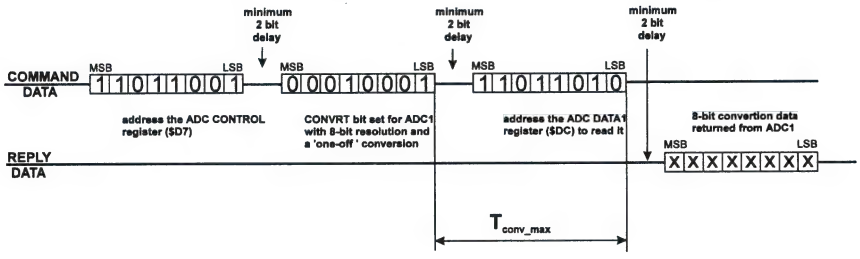


Figure 3: Example of a one-off 8-bit "conversion and read"

Note:

1. T_{CONV_MAX} is directly related to the A/D clock frequency, which in turn is set by the external clock frequency and the clock divider.

   T_{CONV_MAX} = ((n + 2) x 'NUMBER OF ENABLED MUX INPUTS' / f_{A/D_CLK}) [Seconds]

   where: n = 8 or 10 for 8 bit 10 bit conversions, respectively.

   where: $f_{A/D\_CLK} = \frac{XTAL}{DIVIDER}$, (Divider is selected by bits 0, 1, 2 in CLOCK/IRQ Control Register)

4.4 Magnitude Comparators and Interrupt Request

High and low digital comparator reference levels are provided for the four digital magnitude comparators via the 'C-BUS' interface. The digital input to the comparators is provided by the most significant 8 bits of each A/D data. The resolution of each comparator is independent of the selected output resolution of the A/D.

When the sampled data falls outside the high or low digital comparator reference levels the status register is updated and the $\overline{IRQ}$ pin is pulled low. When a reference level is set to '0', its IRQ is disabled.

4.5 Software Description

4.5.1 Address/Commands

Instructions and Data are transferred via the 'C-BUS' in accordance with the timing information provided in Figure 4.

Instruction and data transactions to and from the FX839 consist of an Address/Command byte followed by either:

(i) a control or DAC data write (1 or 2 bytes) or,

(ii) a status or A/D data read (1 or 2 bytes)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.5.2 Write Only Register (8-Bit and 16-Bit)

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$01	RESET	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	CLOCK/IRQ						DIVIDER		
$D0	CONTROL	0	0	0	0	0	BIT 2	BIT 1	BIT 0
	VARIABLE			MOD1	MOD1				
$D2	ATTENUATOR (1)	0	0	ENABLE	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	VARIABLE			MOD2	MOD2				
	ATTENUATOR (2)	0	0	ENABLE	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	DAC	NBIT	NBIT	NBIT		DAC1	DAC2	DAC3	
$D3	CONTROL	DAC1	DAC2	DAC3	0	ENABLE	ENABLE	ENABLE	0
	DAC1 DATA								
$D4	(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1								
	(2)	0	0	0	0	0	0	BIT 9	BIT 8
	DAC2 DATA								
$D5	(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1								
	(2)	0	0	0	0	0	0	BIT 9	BIT 8
	DAC3 DATA								
$D6	(1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1								
	(2)	0	0	0	0	0	0	BIT 9	BIT 8
	A/D			CONV	A/DIN1	A/DIN2	A/DIN3	A/DIN4	
$D7	CONTROL	0	NBIT SEL	MODE	ACTIVE	ACTIVE	ACTIVE	ACTIVE	CONVRT
	MAG COMP ONE	MAGNITUDE COMPARATOR UPPER LEVEL							
$D8	LEVELS (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP ONE	MAGNITUDE COMPARATOR LOWER LEVEL							
	LEVELS (2)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP TWO	MAGNITUDE COMPARATOR UPPER LEVEL							
$D9	LEVELS (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP TWO	MAGNITUDE COMPARATOR LOWER LEVEL							
	LEVELS (2)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP THREE	MAGNITUDE COMPARATOR UPPER LEVEL							
$DA	LEVELS (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP THREE	MAGNITUDE COMPARATOR LOWER LEVEL							
	LEVELS (2)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP FOUR	MAGNITUDE COMPARATOR UPPER LEVEL							
$DB	LEVELS (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	MAG COMP FOUR	MAGNITUDE COMPARATOR LOWER LEVEL							
	LEVELS (2)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Table 2: Write Only Register (8-Bit and 16-Bit)

Note

1. A second byte is expected by the 'C-BUS' interface only when the 'NBIT DAC*n*' bit of the 'DAC Control Register' is set high. Otherwise the data transfer is a single byte (Bit 7 to Bit 0).

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.6 Read Only Registers (8-Bit and 16-Bit)

HEX ADDRESS/ COMMAND	REGISTER NAME	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
$D1	IRQ FLAGS	HIRQF 4	LIRQF 4	HIRQF 3	LIRQF 3	HIRQF 2	LIRQF 2	HIRQF 1	LIRQF 1
$DC	A/D DATA1 (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1 (2)	0	0	0	0	0	0	BIT 9	BIT 8
$DD	A/D DATA2 (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1 (2)	0	0	0	0	0	0	BIT 9	BIT 8
$DE	A/D DATA3 (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1 (2)	0	0	0	0	0	0	BIT 9	BIT 8
$DF	A/D DATA4 (1)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	*See Note 1 (2)	0	0	0	0	0	0	BIT 9	BIT 8

Table 3: Read Only Registers (8-Bit and 16-Bit)

Note :

1. A second byte is available via the 'C-BUS' interface only when the 'NBIT SEL' bit of the 'A/D Control Register' is set high. Otherwise the data transfer is a single byte (Bit 7 to Bit 0).

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480164.001

4.7 Write Only Register Description

4.7.1 RESET Register (Hex Address $01)

The reset command has no data attached to it. It sets the device registers into the specific states listed below:

REGISTER NAME		BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT 3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
CLOCK/IRQ CONTROL		0	0	0	0	0	0	0	0
DAC CONTROL		0	0	0	0	0	0	0	0
DAC1 DATA[1]		0	0	0	0	0	0	0	0
DAC2 DATA[1]		0	0	0	0	0	0	0	0
DAC3 DATA[1]		0	0	0	0	0	0	0	0
A/D CONTROL		0	0	0	0	0	0	0	0
VARIABLE ATTENUATOR	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0
MAG COMP ONE LEVELS	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0
MAG COMP TWO LEVELS	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0
MAG COMP THREE LEVELS	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0
MAG COMP FOUR LEVELS	(1)	0	0	0	0	0	0	0	0
	(2)	0	0	0	0	0	0	0	0

Table 4: RESET Register (Hex Address $01)

Note

1. Default resolution is defined as 8-Bits.

4.7.2 CLOCK/IRQ CONTROL Register (Hex Address $D0)

This register controls the A/D clock divide ratio:

Bits 7 to 3	Reserved for future use. These bits should be set to '0'.
DIVIDER (Bit 2 - Bit 0)	The Xtal input clock divide ratio, which sets the A/D sample clock frequency is defined in the following table.

Table 5: CLOCK/IRQ CONTROL Register (Hex Address $D0)

Bit 2	Bit 1	Bit 0	Function
0	0	0	Powersave
0	0	1	÷1
0	1	0	÷2
0	1	1	÷4
1	0	0	÷8
1	0	1	÷16
1	1	0	÷32
1	1	1	÷64

Table 6: DIVIDER (Bit 2 - Bit 0)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.7.3 VARIABLE ATTENUATOR Register (Hex address $D2)

This is a 16-bit register. Byte (1) is sent first. Bits 0 - 5 of the first byte in this register are used to set the attenuation of the Modulator 1 amplifier and bits 0 - 5 of the second byte in this register are used to set the attenuation of the Modulator 2 amplifier, according to the tables below:

5	4	3	2	1	0	Mod. 1 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	12.0dB
1	0	0	0	1	0	11.6dB
1	0	0	0	1	1	11.2dB
1	0	0	1	0	0	10.8dB
1	0	0	1	0	1	10.4dB
1	0	0	1	1	0	10.0dB
1	0	0	1	1	1	9.6dB
1	0	1	0	0	0	9.2dB
1	0	1	0	0	1	8.8dB
1	0	1	0	1	0	8.4dB
1	0	1	0	1	1	8.0dB
1	0	1	1	0	0	7.6dB
1	0	1	1	0	1	7.2dB
1	0	1	1	1	0	6.8dB
1	0	1	1	1	1	6.4dB
1	1	0	0	0	0	6.0dB
1	1	0	0	0	1	5.6dB
1	1	0	0	1	0	5.2dB
1	1	0	0	1	1	4.8dB
1	1	0	1	0	0	4.4dB
1	1	0	1	0	1	4.0dB
1	1	0	1	1	0	3.6dB
1	1	0	1	1	1	3.2dB
1	1	1	0	0	0	2.8dB
1	1	1	0	0	1	2.4dB
1	1	1	0	1	0	2.0dB
1	1	1	0	1	1	1.6dB
1	1	1	1	0	0	1.2dB
1	1	1	1	0	1	0.8dB
1	1	1	1	1	0	0.4dB
1	1	1	1	1	1	0dB

5	4	3	2	1	0	Mod. 2 Attenuation
0	X	X	X	X	X	Disabled (V_{BIAS})
1	0	0	0	0	0	>40dB
1	0	0	0	0	1	6.0dB
1	0	0	0	1	0	5.8dB
1	0	0	0	1	1	5.6dB
1	0	0	1	0	0	5.4dB
1	0	0	1	0	1	5.2dB
1	0	0	1	1	0	5.0dB
1	0	0	1	1	1	4.8dB
1	0	1	0	0	0	4.6dB
1	0	1	0	0	1	4.4dB
1	0	1	0	1	0	4.2dB
1	0	1	0	1	1	4.0dB
1	0	1	1	0	0	3.8dB
1	0	1	1	0	1	3.6dB
1	0	1	1	1	0	3.4dB
1	0	1	1	1	1	3.2dB
1	1	0	0	0	0	3.0dB
1	1	0	0	0	1	2.8dB
1	1	0	0	1	0	2.6dB
1	1	0	0	1	1	2.4dB
1	1	0	1	0	0	2.2dB
1	1	0	1	0	1	2.0dB
1	1	0	1	1	0	1.8dB
1	1	0	1	1	1	1.6dB
1	1	1	0	0	0	1.4dB
1	1	1	0	0	1	1.2dB
1	1	1	0	1	0	1.0dB
1	1	1	0	1	1	0.8dB
1	1	1	1	0	0	0.6dB
1	1	1	1	0	1	0.4dB
1	1	1	1	1	0	0.2dB
1	1	1	1	1	1	0dB

X = don't care

MOD1 ENABLE (Bit 5, first byte)	When this bit is '1' the MOD1 attenuator is enabled. When this bit is '0' the MOD1 attenuator is disabled (i.e. powersaved).
MOD2 ENABLE (Bit 5, second byte)	When this bit is '1' the MOD2 attenuator is enabled. When this bit is '0' the MOD2 attenuator is disabled (i.e. powersaved).
(Bits 7 and 6, first and second bytes)	Reserved for future use. These should be set to '0'.

Table 7: VARIABLE ATTENUATOR Register (Hex address $D2)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.7.4 DAC CONTROL Register (Hex address $D3)

This register controls the resolution and the number of enabled DAC outputs:

NBIT DAC1, NBIT DAC2, NBIT DAC3	
(Bit 7 to Bit 5)	These bits define the input resolutions for each of the four DACs. When 'NBIT DAC*n*' is '0' the resolution of DAC*n* is 8-Bits. When 'NBIT DAC*n* is '1' the resolution of DAC*n* is 10-Bits.
Bit 4	Reserved for future use. This bit should be set to '0'.
DAC1 ENABLE, DAC2 ENABLE, DAC3 ENABLE	
(Bit 3 to Bit 1)	These bits allow any one or more of the three DACs to be powered up. When '0' the DAC*n* is powered down and the output is high impedance. When '1' the DAC is powered on and the output voltage is defined by the DAC Data Registers.
Bit 0	Reserved for future use. This bit should be set to '0'.

4.7.5 DAC1 DATA Register (Hex Address $D4)

4.7.6 DAC2 DATA Register (Hex Address $D5)

4.7.7 DAC3 DATA Register (Hex Address $D6)

The data in these three registers sets the analog voltage at the output of DAC1, DAC2 and DAC3. This data will consist of one or two bytes depending on the defined input resolution which is set by bits 7, 6 and 5 of the DAC Control Register. When operating with 10-bit resolution Bit 7 to Bit 2 of the DAC*n* DATA Register second data byte must be set to "0".

4.7.8 A/D CONTROL Register (Hex Address $D7)

This register controls the resolution, active inputs and conversion modes of the A/D as described below:

Bit 7	Reserved for future use. This bit should be set to '0'.
NBIT SEL (Bit 6)	This bit defines the output resolution for the A/D. When '0' the resolution is 8 bits. Therefore when reading the converted data the transfer is of a single data byte. When '1' the resolution is 10 bits. Therefore when reading the converted data the transfer is of two data bytes.
CONV MODE (Bit 5)	When '0' a one-off conversion is made of each active input channel, defined by Bit 4 to Bit 1, at which point the internal clock is disabled. A conversion is initiated by setting the 'CONVRT' bit (Bit 0) high. When '1' all active input channels are continuously sampled and the latest converted data stored for each channel. The 'CONVRT' bit is reset when this bit is set and it has no effect on the conversion procedure.
A/D1 ACTIVE, A/D2 ACTIVE, A/D3 ACTIVE, A/D4 ACTIVE	
(Bit 4 to Bit 1)	These bits allow any one or more of the four A/D input channels to be enabled. When '0' the A/DIN*n* input voltage is not converted. When '1' the A/DIN*n* input is defined as active and the input voltage is converted.
CONVRT (Bit 0)	This bit need only be changed when the 'CONV MODE' bit (Bit 5) is '0'. When CONVRT is set it initiates a one-off conversion of all active input channels and is internally reset when the conversions are complete. This bit remains internally reset when the 'CONV MODE' bit is '1'.

Table 8: A/D CONTROL Register (Hex Address $D7)

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

4.7.9 MAG COMP ONE LEVEL (Hex Address $D8)

4.7.10 MAG COMP TWO LEVEL (Hex Address $D9)

4.7.11 MAG COMP THREE LEVEL (Hex Address $DA)

4.7.12 MAG COMP FOUR LEVEL (Hex Address $DB)

Each address controls the relevant numbered A/D magnitude comparator.

The first byte, transmitted with the most significant bit first, sets the magnitude comparator upper reference level and the second byte sets the magnitude comparator lower reference level.

When a reference level's value is set to '0' its IRQ is disabled.

4.8 Read Only Register Description

4.8.1 IRQ FLAGS Register (Hex Address $D1)

HIRQF1 (Bit 1) HIRQF2 (Bit 3) HIRQF3 (Bit 5) HIRQF4 (Bit 7)	These bits are set if the relevant digital magnitude comparator input exceeds its upper reference level. These bits are reset to '0' immediately after reading the IRQ FLAGS register. When any of these bits are set, an interrupt will be generated if the relevant reference level is not zero.
LIRQF1 (Bit 0) LIRQF2 (Bit 2) LIRQF3 (Bit 4) LIRQF4 (Bit 6)	These bits are set if the relevant digital magnitude comparator input falls below its lower reference level. These bits are reset to '0' immediately after reading the IRQ FLAGS register. When any of these bits are set, an interrupt will be generated if the relevant reference level is not zero.

Table 9: IRQ FLAGS Register (Hex Address $D1)

4.8.2 A/D DATA1 Register (Hex Address $DC)

4.8.3 A/D DATA2 Register (Hex Address $DD)

4.8.4 A/D DATA3 Register (Hex Address $DE)

4.8.5 A/D DATA4 Register (Hex Address $DF)

This data will consist of one or two bytes depending on the defined input resolution. The input resolution is set by Bit 6 of the A/D CONTROL Register. When operating at 10-Bit resolution, Bit 7 to Bit 2 of the second data byte will be set to '0'.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. Performance Specification

5.1 Electrical Performance

5.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS}) (either AV_{DD} or DV_{DD})		-0.3	7.0	V
Voltage on any pin to V_{SS}		-0.3	V_{DD} + 0.3	V
Current				
AV_{DD}		-30	30	mA
DV_{DD}		-30	30	mA
V_{SS}		-30	30	mA
Any other pin		-20	20	mA
AV_{DD} - DV_{DD}	Note 1, 2	-100	100	mV
DW / P Package				
Total Allowable Power Dissipation at T_{AMB} = 25°C			800	mW
Derating above 25°C			13	mW/°C above 25°C
Storage Temperature		-55	125	°C
Operating Temperature		-40	85	°C
DS Package				
Total Allowable Power Dissipation at T_{AMB} = 25°C			550	mW
Derating above 25°C			9	mW/°C above 25°C
Storage Temperature		-55	125	°C
Operating Temperature		-40	85	°C

Note:

1. It is recommended that AV_{DD} be connected to DV_{DD} through a filter.
2. It is also recommended that AV_{DD} and DV_{DD} Voltages be tightly a.c. coupled to V_{SS} with a capacitor.

5.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS}) (either AV_{DD} or DV_{DD})	3.0	5.5	V
Operating Temperature	-40	85	°C
Xtal Frequency	0.5	6.0	MHz

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
AV_{DD}= DV_{DD} = V_{DD} = 3.3V to 5.0V, T_{AMB} = 25°C

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
Supply Difference (AV_{DD} - DV_{DD})		-100		100	mV
I_{DD}					
V_{DD} = 5V					
powersaved			TBD	TBD	mA
not powersaved			TBD	TBD	mA
V_{DD} = 3.3V					
powersaved			TBD	TBD	mA
not powersaved			TBD	TBD	mA
'C-BUS' Interface					
Input Logic '1'		70%			DV_{DD}
Input Logic '0'				30%	DV_{DD}
Input Leakage Current (Logic '1' and '0')		-1.0		1.0	µA
Input Capacitance				7.5	pF
Output Logic '1' (I_{OH} = 120µA)		90%			DV_{DD}
Output Logic '0' (I_{OL} = 360µA)				10%	DV_{DD}
DACs and Output Buffers (Guaranteed monotonic)					
Un-loaded Performance					
Resolution			8 or 10		Bits
Internal DAC Settling Time (to 0.5 lsb)				10.0	µs
Integral non-linearity					
8 Bit mode				±3.0	LSBs
10 Bit mode				±5.0	LSBs
Differential non-linearity					
8 Bit mode				1.0	LSBs
10 Bit mode				1.0	LSBs
Buffer Slew Rate (with 20pF load)				TBD	V/µs
Buffer Output Resistance				200	Ω
Zero Error (For 0000_{HEX} code input)		-20	0	20	mV
RMS Output Noise Voltage	1		10		µV
Loaded Performance	2				
Output voltage with 5kΩ resistive load to ground					
Digital code = $3FF_{HEX}$	3	4.79			V
Digital code = 200_{HEX} 10 Bit	3		2.495		V
Digital code = 80_{HEX} 8 Bit	3		2.495		V
Output voltage with 5kΩ resistive load to V_{DD}					
Digital code = 000_{HEX}	3			200	mV
Minimum Resistive Load	4	1.0			kΩ

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

	Notes	Min.	Typ.	Max.	Units
A/Ds and Multiplexed Inputs (Guaranteed monotonic)					
Resolution			8 or 10		Bits
Input signal 'linear rate of change' For 1 Bit error V_{DD} = 3.3V, and f_{A/D_CLK} = 1MHz					
8 bit operation				1.3	mV/µs
10 Bit operation				0.27	mV/µs
Conversion Time					
8 Bits f_{A/D_CLK} = 1MHz			10		µs
10 Bits f_{A/D_CLK} = 1MHz			12		µs
Integral non-linearity					
8 Bit mode				1.0	LSBs
10 Bit mode				2.0	LSBs
Differential non-linearity					
8 Bit mode				0.5	LSBs
10 Bit mode				1.0	LSBs
Zero error		-20		20	mV
A/D Clock Frequency (f_{A/D_CLK})			1.0	TBD	MHz
Input Capacitance			TBD		pF
Variable Attenuators					
Nominal Adjustment Range					
MOD1 Attenuator		-12.0		0	dB
MOD2 Attenuator		-6.0		0	dB
Attenuation Accuracy		-1.0		1.0	dB
Step Size					
MOD1		0.2	0.4	0.6	dB
MOD2		0.1	0.2	0.3	dB
Output Impedance	5		600		Ω
Bandwidth (-3dB)	5		100		kHz
Magnitude Comparators and Interrupt Request					
Resolution			8		Bits
Output Logic '0' at $\overline{IRQ}$ (I_{OL}= 360µA and pull-up resistor R2 = 22kΩ ± 10% to DV_{DD})				0.1 x V_{DD}	V
'Off' State Leakage Current at $\overline{IRQ}$ $V_{OUT} = DV_{DD}$				10	µA
Xtal/Clock Input					
Frequency Range		0.5		6.0	MHz
'High' pulse width		40			ns
'Low' pulse width		40			ns
Input Impedance (at 100Hz)			10		MΩ
Gain (input = 1mV_{RMS} at 100Hz)			20		dB

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Operating Characteristics Notes:

1. Measured over a 0 to 30kHz Band.
2. The extremes of the DAC output range, when resistively loaded, are affected by the output impedance of the DAC buffer. Under these conditions the output impedance can approach 200Ω. However; when the output is operating well within the supply, the output impedance will be significantly lower, thereby improving the loaded performance.
3. R_{LOAD} = 5kΩ AV_{DD} = 5.0V.
4. Loads less than 1kΩ will produce output distortion.
5. Small signal impedance, at AV_{DD} = 5V and T_{AMB} = 25°C.

5.1.4 Timing

For the following conditions unless otherwise specified:

DV_{DD} = 3.3V to 5.0V, T_{AMB} = 25°C

	Parameter	Min.	Typ.	Max.	Units
t_{CSE}	"CS-Enable to Clock-High"	2.0			µs
t_{CSH}	Last "Clock-High to CS-High"	4.0			µs
t_{HIZ}	"CS-High to Reply Output 3-state"			2.0	µs
t_{CSOFF}	"CS-High" Time between transactions	2.0			µs
t_{NXT}	"Inter-Byte" Time	4.0			µs
t_{CK}	"Clock-Cycle" time	2.0			µs

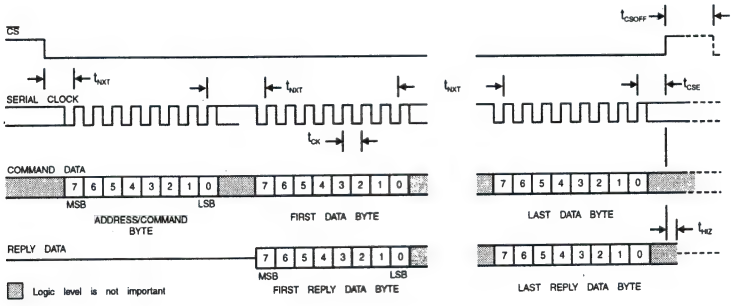


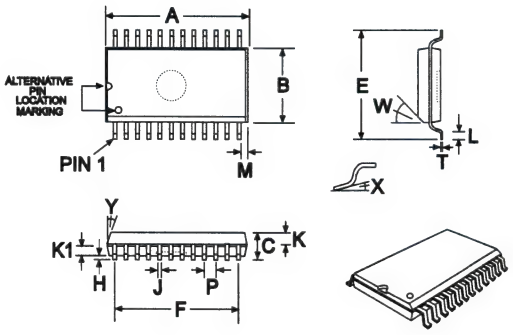
Figure 4: 'C-BUS' Timing

Timing Notes:

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into and out of the peripheral on the rising SERIAL CLOCK edge.
3. Loaded commands are acted upon at the end of each command.
4. To allow for differing µC serial interface formats 'C-BUS' compatible ICs are able to work with either polarity SERIAL CLOCK pulses.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

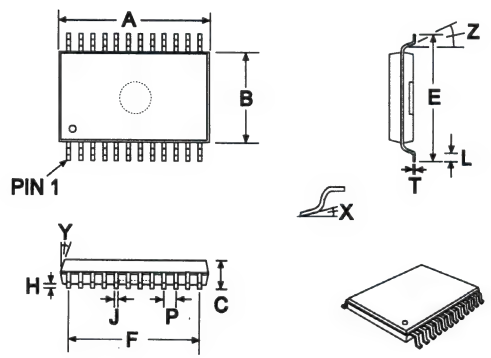
5.2 Packaging



DIM.	MIN.	TYP.	MAX.
A	0.597 (15.16)		0.613 (15.57)
B	0.291 (7.39)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.394 (10.01)		0.419 (10.64)
F		0.566 (14.37)	
H	0.004 (0.10)		0.012 (0.30)
J	0.014 (0.36)		0.018 (0.46)
K	0.036 (0.91)		0.046 (1.17)
K1	0.036 (0.91)		0.046 (1.17)
L	0.016 (0.41)		0.050 (1.27)
M	0.021 (0.53)		0.031 (0.79)
P		0.050 (1.27)	
T	0.009 (0.23)		0.012 (0.30)
W		45°	
X	0°		8°
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 5: 24-pin SOIC Mechanical Outline: *Order as part no. MX839DW*

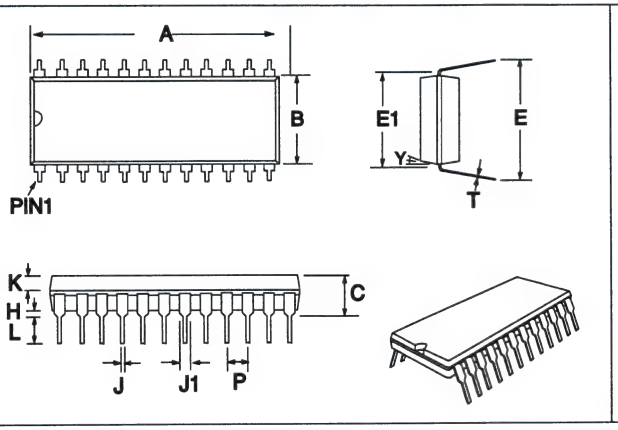


DIM.	MIN.	TYP.	MAX.
A	0.318 (8.07)		0.328 (8.33)
B	0.205 (5.20)		0.212 (5.38)
C	0.068 (1.73)		0.078 (1.99)
E	0.301 (7.65)		0.311 (7.90)
F		0.286 (7.15)	
H	0.002 (0.05)		0.008 (0.21)
J	0.010 (0.25)		0.015 (0.38)
L	0.022 (0.55)		0.037 (0.95)
P		0.026 (0.65)	
T	0.005 (0.13)		0.009 (0.22)
X	0°		8°
Y	7°		9°
Z	4°		10°

NOTE : All dimensions in inches (mm.)
Angles in degrees

Figure 6: 24-pin SSOP Mechanical Outline: *Order as part no. MX839DS*

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20480164.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.200 (30.48)		1.270 (32.26)
B	0.500 (12.70)		0.555 (14.04)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.67)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.05)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 24-pin PDIP Mechanical Outline: ***Order as part no. MX839P***

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20480164.001

Technical Specifications

Section 10: Application Notes

Description	Page
Practical GMSK Data Transmission	3
MX589 GMSK Modem Application	15
MX909A Signal Acquisition Principles	33
MX909A Fade Management, Data Detection, and Carrier Drift Management	37
MSK and its Application to Wireless Data Transmission	41
Using an MX469 MSK Synchronous Modem with an Asynchronous Data I/O	73
Continuously Variable Sloped Delta Modulation: A Tutorial	77
Audio Delay Circuit based on the MX609 CVSD Codec	93
Crystal Oscillator Circuit Design	95
Tone Generation: An Application of the MX105A	99
MX029: Dual Digitally Controlled Amplifier Application	107
MX009 and MX019 Amplifier Array Application	113
Noise Immunity Circuit for the MX633/643 Call Progress Detectors	115
SPM (Subscriber Pulse Metering) for PCMCIA, Data, and Fax Modems	119
Error Detection & Correction of MPT1327 formatted messages	121
Generation of Non-Standard CTCSS Tones	129
Switched Capacitor Interfacing	137
Variable Split Band Scrambling	147
DBS800 C-BUS System Development Overview	153

Practical GMSK Data Transmission

Introduction

The proliferation of computers in today's society has increased the demand for transmission of data over wireless links. Binary data, composed of sharp "one to zero" and "zero to one" transitions, results in a spectrum rich in harmonic content that is not well suited to RF transmission. Hence, the field of digital modulation has been flourishing. Recent standards such as Cellular Digital Packet Data (CDPD) and Mobitex* specify Gaussian filtered Minimum Shift Keying (GMSK) for their modulation method.

GMSK is a simple yet effective approach to digital modulation for wireless data transmission. To provide a good understanding of GMSK, we will review the basics of MSK and GMSK, as well as how GMSK is implemented in CDPD and Mobitex systems.

GMSK modems reduce system complexity, and in turn lower system cost. There are, however, some important implementation details to be considered. This paper will cover some of these details, focusing on interfacing a single chip baseband modem to the IF/RF section of a "typical" FM radio topology.

Background

If we look at a Fourier series expansion of a data signal we see harmonics extending to infinity. When these harmonics are summed, they give the data signal its sharp transitions. Hence, an unfiltered NRZ data stream used to modulate an RF carrier will produce an RF spectrum of considerable bandwidth. Of course, the FCC has strict regulations about spectrum usage and such a system is generally considered impractical. But if we start to remove the high frequency harmonics from the Fourier series (i.e. pass the data signal through a lowpass filter), the transitions in the data will become progressively less sharp. This suggests that pre-modulation filtering is an effective method for reducing the occupied spectrum for wireless data transmission. In addition to a compact spectrum, a wireless data modulation scheme must have good bit error rate (BER) performance under noisy conditions. Its performance should also be independent of power amplifier linearity to allow the use of class C power amplifiers.

The academic field of "Data Transmission" is loaded with modulation strategies that attempt to meet the above criteria. Most involve translation of data bits or patterns into a particular combination of phase, frequency or amplitude. Some of the more notable techniques are listed in Table 1.

** Mobitex is a trademark owned by the Telia Corporation.*

© 1997 MX-COM, Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20830067.001

MODULATION TECHNIQUE	COMMON ACRONYM
Frequency Shift Keying	FSK
Multi-level Frequency Shift Keying	MFSK
Continuous Phase Frequency Shift Keying	CPFSK
Minimum Shift Keying	MSK
Gaussian Minimum Shift Keying	GMSK
Tamed Frequency Modulation	TFM
Phase Shift Keying	PSK
Quadrature Phase Shift Keying	QPSK
Differential Quadrature Phase Shift Keying	DQPSK
Pi/4 Differential Quadrature Phase Shift Keying	Pi/4 DQPSK
Quadrature Amplitude Modulation	QAM

Table 1: Modulation formats

Each of the modulation formats listed in Table 1 is suited to specific applications. In general, schemes that rely on more than two levels (e.g. QAM, QPSK) require better signal to noise ratios (SNR) than two-level schemes for similar BER performance. Additionally, in a wireless environment, multi-level schemes generally require greater power amplifier linearity than two-level schemes. The fact that GMSK uses a two-level continuous phase modulation (CPM) format has contributed to its popularity. Another point in its favor is that it allows the use of class C power amplifiers (relatively non-linear) and data rates approaching the channel BW (dependent on filter bandwidth and channel spacing).

GMSK Basics

Prior to discussing GMSK in detail we need to review MSK, from which GMSK is derived. MSK is a continuous phase modulation scheme where the modulated carrier contains no phase discontinuities and frequency changes occur at the carrier zero crossings. MSK is unique due to the relationship between the frequency of a logical zero and one: the difference between the frequency of a logical zero and a logical one is always equal to half the data rate. In other words, the modulation index is 0.5 for MSK, and is defined as

$$m = \Delta f \times T$$

where,

$$\Delta f = | f_{\text{logic 1}} - f_{\text{logic 0}} |$$

$$T = {}^{1}/_{\text{bit rate}}$$

For example, a 1200 bit per second baseband MSK data signal could be composed of 1200 Hz and 1800 Hz frequencies for a logical one and zero respectively (see Figure 1).

© 1997 MX-COM, Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.

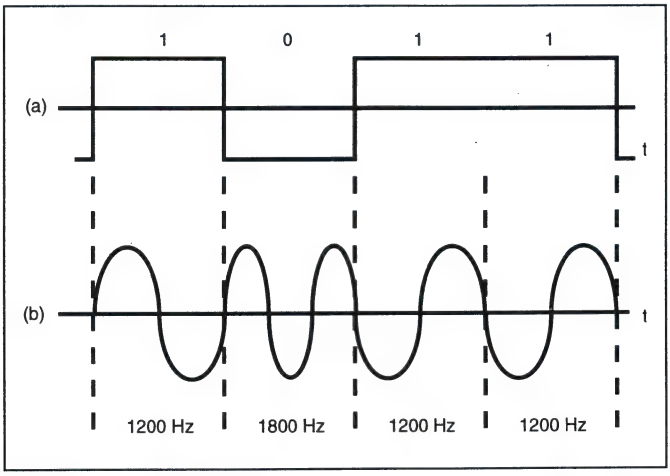


Figure 1: 1200 baud MSK data signal; a) NRZ data, b) MSK signal.

Baseband MSK, as shown in Figure 1, is a robust means of transmitting data in wireless systems where the data rate is relatvely low compared to the channel BW. MX-COM devices such as the MX429 and MX469 are single chip solutions for baseband MSK systems, incorporating modulation and demodulation circuitry on a single chip.

An alternative method for generating MSK modulation can be realized by directly injecting NRZ data into a frequency modulator with its modulation index set for 0.5 (see Figure 2). This approach is essentially equivalent to baseband MSK. However, in the direct approach the VCO is part of the RF/IF section, whereas in baseband MSK the voltage to frequency conversion takes place at baseband.

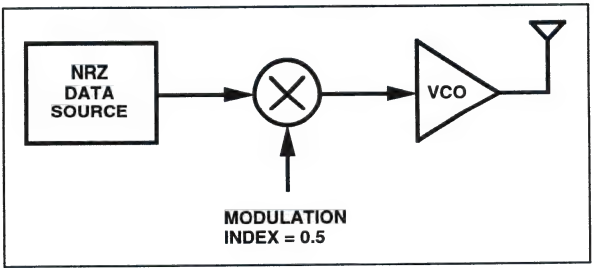


Figure 2: Direct MSK modulation.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830067.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

The fundamental problem with MSK is that the spectrum is not compact enough to realize data rates approaching the RF channel BW. A plot of the spectrum for MSK reveals sidelobes extending well above the data rate (see Figure 4). For wireless data transmission systems which require more efficient use of the RF channel BW, it is necessary to reduce the energy of the MSK upper sidelobes. Earlier we stated that a straightforward means of reducing this energy is lowpass filtering the data stream prior to presenting it to the modulator (pre-modulation filtering). The pre-modulation lowpass filter must have a narrow BW with a sharp cutoff frequency and very little overshoot in its impulse response. This is where the Gaussian filter characteristic comes in. It has an impulse response characterized by a classical Gaussian distribution (bell shaped curve), as shown in Figure 3. Notice the absence of overshoot or ringing.

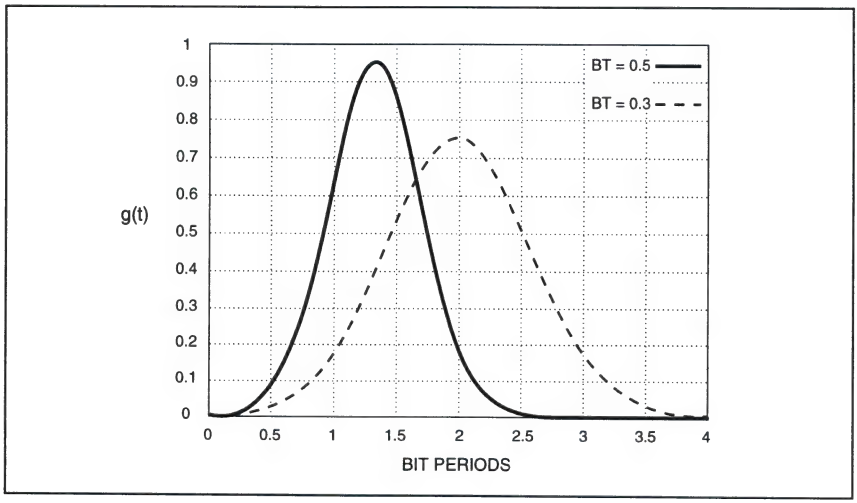


Figure 3: Gaussian filter impulse response for BT=0.3 and BT=0.5.

Figure 3 depicts the impulse response of a Gaussian filter for BT = 0.3 and 0.5. BT is related to the filter's -3dB BW and data rate by

$$BT = \frac{f_{-3dB}}{\text{BIT RATE.}}$$

Hence, for a data rate of 9.6 kbps and a BT of 0.3, the filter's -3dB cutoff frequency is 2880Hz.

Still referring to Figure 3, notice that a bit is spread over approximately 3 bit periods for BT=0.3 and two bit periods for BT=0.5. This gives rise to a phenomena called intersymbol interference (ISI). For BT=0.3 adjacent symbols or bits will interfere with each

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830067.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

other more than for BT=0.5. GMSK with BT=∞ is equivalent to MSK. In other words, MSK does not intentionally introduce ISI. Greater ISI allows the spectrum to be more compact, making demodulation more difficult. Hence, spectral compactness is the primary trade-off in going from MSK to Gaussian premodulation filtered MSK. Figure 4 displays the normalized spectral densities for MSK and GMSK. Notice the reduced sidelobe energy for GMSK. Utlimately, this means channel spacing can be tighter for GMSK when compared to MSK for the same adjacent channel interference.

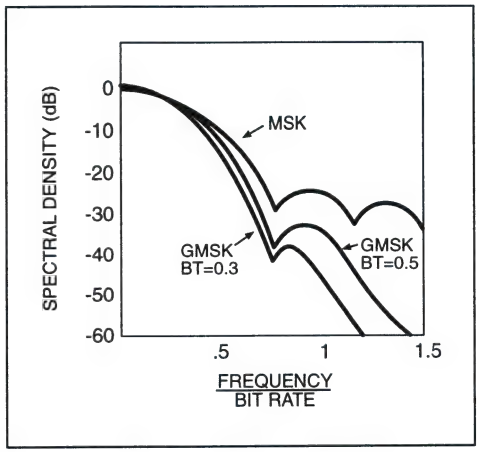


Figure 4: Spectral density for MSK and GMSK.

Performance Measurements

The performance of a GMSK modem is generally quantified by measurement of the signal-to-noise ratio (SNR) versus BER. SNR is related to E_b/N_0 by

$$\frac{E_b}{N_0} = \frac{S}{RN_0} = \frac{S}{N}\left(\frac{B_n}{R}\right)$$

where,

S = signal power
R = data rate in bits per second
N_0 = noise power spectral density (watts/Hz)
E_b = energy per bit
$B_n * N_0 = N$ = noise power
B_n = noise BW of IF filter.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830067.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Recent Standards

GMSK has been adopted by many wireless data communication protocols. Two of the systems specifying GMSK modulation are Cellular Digital Packet Data (CDPD) and Mobitex.

CDPD uses the dead air time on cellular systems by sending data packets on idle cellular voice channels. Data is transmitted at 19.2kbps using a BT of 0.5. This high data rate is facilitated by the 30kHz channel spacing of the cellular network and the spectral conservation of GMSK. Voice has priority over data and will interrupt data transmission, forcing the CDPD system to seek a new idle cellular channel. This could prove to be an obstacle to the throughput promised by its 19.2kbps data rate when implemented in a highly congested area where dead time is limited.

CDPD is being added to the existing cellular infrastructure and therefore promises to offer widespread coverage. The coverage and ease of adaptation appear to be the greatest strengths of the CDPD system. The slower-than-expected deployment of CDPD has many people anxious and perhaps a bit nervous about its potential.

Competition from dedicated data systems such as Mobitex is not insignificant. While Mobitex has a lower data rate than CDPD (8kbps), it is not sharing its channels with cellular voice transmissions. Several subtleties such as this will make it more difficult for end users to select the system best suited to their needs by obscuring the actual throughput potential of the systems. Mobitex's choice of 8kbps and a BT of 0.3 afford it a much tighter channel spacing (12.5kHz) than CDPD, but the greater intersymbol interference for BT=0.3 limits the system's tolerance to noise and distortion. The narrower channel also limits Mobitex's tolerance to frequency offsets between units.

Both CDPD and Mobitex employ forward error correction in their packetting of data. Figure 5 shows the typical packet structures of these two systems for comparison. Forward error correction (FEC) helps improve the systems' throughput when less than ideal channel conditions exist.

© 1997 MX-COM, Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20830067.001

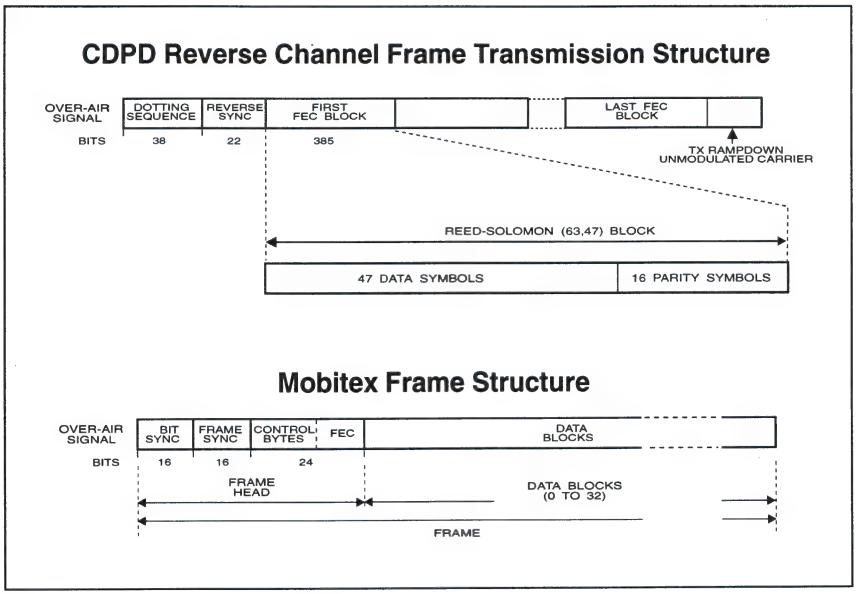


Figure 5: Typical packet structures for CDPD and Mobitex.

Implementation Considerations

The design of a GMSK modulator/demodulator appears to be a straightforward task. Most textbooks present the modulator as a "simple" Gaussian filter cascaded with a VCO. However, in practice it is generally not that simple. Many of the sections in a typical radio such as the synthesizer, IF filter, power amplfier, etc. have far from ideal behavior. In particular, the synthesizer presents a unique problem for GMSK modulation. Data patterns consisting of several consectutive ones or zeros have a spectral response extending down to near DC. Most frequency synthesizers will not respond to this low frequency signal (a typical synthesizer effectively has a highpass filter characteristic).Two of the most common modulation methods, which help considerably where the non-ideal behavior of the synthesizer is concerned, are "Two-point modulation" and "Quadrature modulation."

© 1997 MX-COM, Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20830067.001

Two point modulation

Two point modulation (see Figure 5) circumvents this synthesizer problem by splitting the Gaussian filtered signal; one portion is directed to the VCO modulation input, the other portion is used to modulate the TCXO. The TCXO is not in the frequency control feedback loop. Hence, the TCXO can be modulated by the low frequency portion of the signal, and its output is effectively summed with the signal modulating the VCO in the synthesizer. The composite signal has a spectral response extending down to DC.

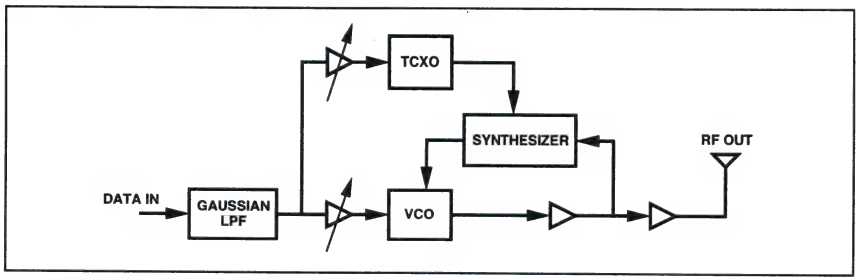


Figure 6: Two point modulation radio block diagram.

I and Q modulation

Quadrature (I and Q) modulation can also be effective in eliminating synthesizer shortcomings. In I and Q modulation, the Gaussian filtered data signal is separated into in-phase (I) and quadrature phase (Q) components. The modulated RF signal is created by mixing the I and Q components up to the frequency of the RF carrier, where they are summed together. The role of the synthesizer has now been reduced to merely changing carrier frequency for channel selection. The key to optimum performance with quadrature modulation is accurate creation of the I and Q components.

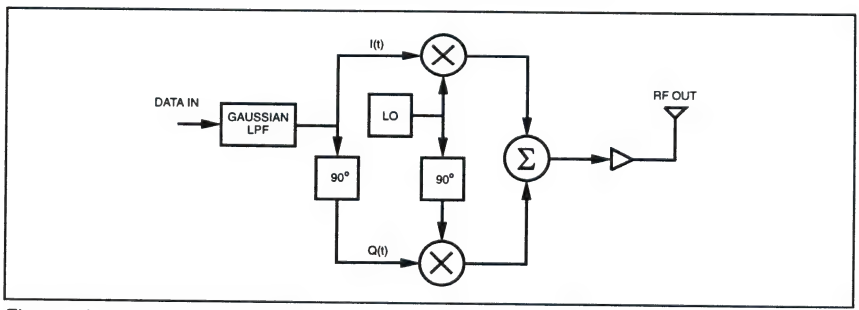


Figure 7: I and Q radio block diagram.

© 1997 MX-COM, Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20830067.001

Baseband I and Q signals can be created by using an all-pass phase shifting network. This network must maintain a 90 degree phase relationship between the I and Q signals for all frequencies in the band of interest.

Demodulation

Demodulation of the GMSK signal requires as much attention to the preservation of an unadulterated wave form as does modulation of the signal. The choice of a Gaussian shaped pre-modulation filter was made for three main reasons[1]:

1) narrow bandwidth and sharp cutoff
2) lower overshoot impulse response
3) preservation of the filter output pulse area.

The first condition gives GMSK modulation its spectral efficiency. It also improves its noise immunity when demodulating. The second condition affords GMSK low phase distortion. This is a major concern when the receiver is demodulating the signal down to baseband, and care must be taken in the design of the IF filtering to protect this characteristic. The third condition ensures the coherence of the signal. While this is quite strict and not realizable with a physical Gaussian filter, the phase response can be kept linear and therefore sufficient for coherent demodulation.

In most systems the constraints on the above goals also include
- Data Rate
- Tx filter bandwidth (BT)
- Channel Spacing
- Allowable adjacent channel interference
- Peak carrier deviation
- Tx and Rx carrier frequency accuracy
- Modulator and Demodulator linearity
- Rx IF filter frequency and phase characteristics.

These constraints are all part of the balance that must be struck to provide a robust GMSK system. The data rate, Tx BT, peak carrier deviation, and carrier frequency accuracy between receiver and transmitter all contribute to the necessary width of the IF filter. The IF filter should have sufficient width to accommodate the maximum variations in the above parameters so that the received signal will not run into the skirts of the filter. The skirts of the IF filter can introduce excessive amounts of group delay (phase distortion) in the higher frequency components of the received data. The passband of the IF filter should have little or no group delay. The more group delay introduced, the more degraded the bit error rate (BER) performance of the receiver will become. Rules of thumb for group delay dictate less than 10% of a bit time is tolerable. How happy you are with this level of performance is very dependent on the other

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830067.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

factors that influence the BER of your system: BT, signal strength, fading, etc. Phase equalization measures can also be taken to help reduce group delay, but if there is control over the IF filter's design these steps can be avoided.

The CDPD and Mobitex standards mentioned earlier are addressed by two devices manufactured by MX-COM: the MX589 and the MX909. Both devices are designed to interface to the transmitter and receiver of a system at baseband. The MX589 is a versatile device capable of operating at data rates from 4kbps-40kbps and at BT's of 0.5 or 0.3. The device is implemented in a CMOS process that allows it to operate at low supply voltages (3.0-5.0 volts) and draw little current (1.5mA @ 3.0V). The digital data interface is a synchronous serial bit stream for both receive and transmit.

The MX909, also fabricated in a CMOS process, is specifically intended for Mobitex type systems, and has a corresponding BT of 0.3. Its data rate can be varied from 4kbps-19.2kbps, but should be set to 8kbps to achieve Mobitex compatibility. It can be operated from a supply voltage of 4.5-5.5 volts and typically draws 3.0mA. The data interface is a parallel microprocessor I/O compatible bus, and the MX909 contains all the circuitry needed to implement the forward error correction encoding and decoding of the Mobitex format.

The demodulation of the baseband GMSK signal presented to these devices is accomplished using a Gaussian shaped lowpass filter, clock extraction and reference level compensation circuitry in concert with data extraction circuitry. The signal first goes through a Gaussian lowpass filter similar to that used by the transmit section. The signal's zero crossing reference and clock timing are then extracted using peak detection circuitry and a phase lock loop in coordination. This cooperative effort helps improve both section's immunity to noise. Once "lock" has been achieved accurate demodulation of data from the data extraction circuitry can be expected.

The peak detection circuitry can adjust to large changes in DC level of the signal within 1.5 bit periods. This "clamping" mode is used when the carrier is first detected by the receiver. The PLL has a wideband acquire mode that can lock onto a signal in less than 8 zero crossings. Using these two modes allows the devices to start decoding data very shortly after the receiver senses carrier. Both the phase lock loop and the peak tracking circuitry have less aggressive modes that afford better noise immunity once the initial acquire modes have obtained lock. The nature of the GMSK signal at baseband requires good response of the system near DC as mentioned in the section on modulation. A more random data pattern does not have as large a DC component and is less sensitive to the highpass characteristics of any AC coupling that might need to be used to interface the baseband signal to the GMSK modulator or demodulator. The bit error rate (BER) performance of the MX589 is shown in Figure 8. The figure shows the effect of various highpass characteristics on the BER profile of the device.

© 1997 MX-COM, Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20830067.001

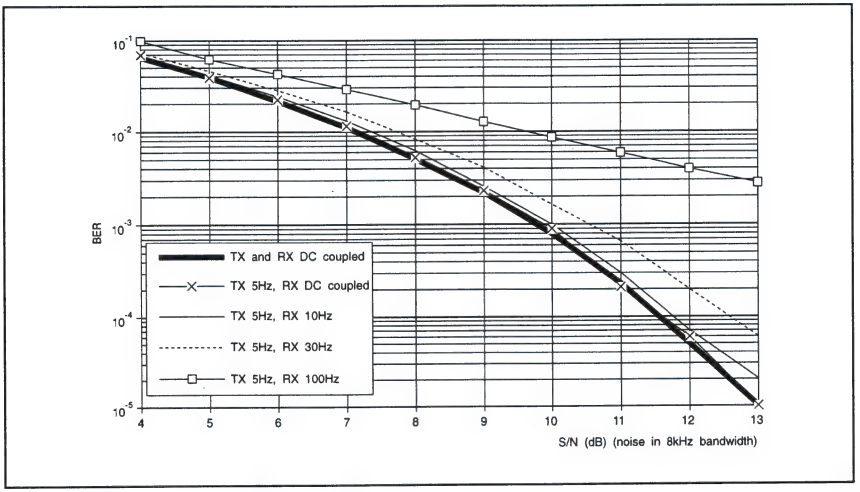


Figure 8: BER performance of the MX589.

This figure represents data taken from a static system running at 8kbps with a BT of 0.3 and a noise bandwidth equal to the bit rate. With the noise bandwidth equal to the bit rate, and assuming the noise spectrum at baseband is flat, the x-axis is in essence E_b/N_0. As an alternative to a full DSP implementation, these two devices offer cost-effective and space conservative solutions to the modulation and demodulation requirements of the CDPD and Mobitex GMSK based systems.

Summary

GMSK provides a straightforward, spectrally efficient modulation method for wireless data transmission systems (e.g. CDPD and Mobitex). MX-COM's MX589 and MX909 baseband GMSK modems offer single-chip solutions, facilitating the implementation of a GMSK system using standard FM radio topologies.

Although the MX-COM baseband modems integrate the majority of the modulation signal processing requirements, some key aspects of system design must not be neglected. For instance, the modulator configuration must have a flat spectral response down to DC. In addition, the receiver's phase response must be linear across the BW occupied by the data with special attention focused on the IF filters. Following these recommendations in conjunction with a single-chip baseband modem insures excellent BER performance, low power consumption and low cost.

© 1997 MX-COM, Inc.
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
All trademarks and service marks are held by their respective companies.
Doc. # 20830067.001

References

[1] Murota, K. and Hirade, K., "GMSK Modulation for Digital Mobile Radio Telephony," IEEE Transactions on Communications, vol COM-29, No. 7. pp. 1044-1050, July 1981.

[2] Pebbles, P. Jr., "Digital Communication Systems," Prentice-Hall, Englewood Cliffs, NJ, 1987.

[3] Sklar, B., "Digital Communications: Fundametals and Applications," Prentice-Hall, Englewood Cliffs, NJ, 1988.

[4] "Cellular Digital Packet Data System Specification, Release 1.0," 1993.

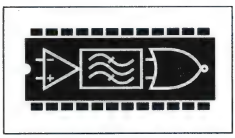
[5] "Radio/Modem Reference Design Guide, Issue 1, Revision 0," RAM Mobile Data, Woodbridge, NJ, 1991.

Authors

Fred Kostedt, Engineer for MX-COM.
James C. Kemerling, Engineer for MX-COM.

This article reprinted from Wireless Design & Development, January 1995, Volume 3 Number 1.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830067.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

MX589 GMSK MODEM Application

Introduction

This application note is to be read in conjunction with the current MX589 Data Sheet. This document is issued to clarify points in currently published documents and to present new information that will enable the user to easily understand and implement this GMSK product.

Contents

Data Transmission by FM Radio

Gaussian Filtered Minimum Shift Keying (GMSK)

GMSK in FM Radio

Implementation of GMSK using the MX589

Bitrate, BT and Bandwidth

Data Formats

Coupling of Rx and Tx Signals

Baseband and RF Bandwidth

Intersymbol Interference

FM Modulator, Demodulator and IF Performance

The EYE Pattern

Example Rx EYE Patterns

Data Sequencing

Data Randomizing (Scrambling)

Data Coding

Rx 'Acquisition' and 'Hold' Modes

Rx Acquire Sequences

'RxHold' Input

Interleaving on Systems with Forward Error Correction (FEC)

Alternative Data Rates

© 1997 MX•COM, INC.

www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA

All trademarks and service marks are held by their respective companies

Doc.# 20830074.001

Data Transmission by FM Radio

The simplest method of sending data over FM radio is to shift the RF carrier frequency in one direction to represent a logic '1' and in the other direction for a logic '0'. This direct method is known as Frequency Shift Keying (FSK); FSK can be successful but results in a very wide transmission bandwidth requirement.

To reduce the transmission bandwidth required input data may be pre-filtered prior to modulation using a specific form of lowpass filtering. One effective method is Gaussian Filtered Minimum Shift Keying (GMSK). Figure 4 is a comparison of the bandwidth requirements of direct FSK and Gaussian filtered data.

Gaussian Filtered Minimum Shift Keying (GMSK)

GMSK is a method of data modulation for sending high speed data in narrow band FM radio channels. In its simplest form GMSK involves passing a digital bitstream through a Gaussian filter before applying it to the input of a frequency modulator.

A Gaussian filter is a lowpass element which when excited by an impulse at its input, gives a Gaussian shaped output response.

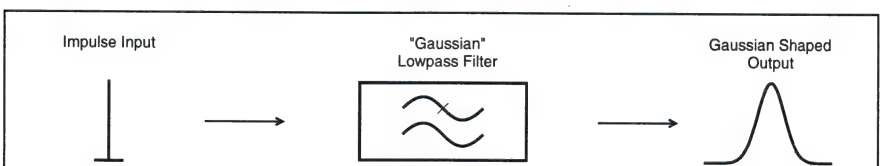


Fig.1 The "Performance" of a Gaussian Filter

GMSK in FM Radio

In an FM radio system using a GMSK modem the data flow is as shown below:

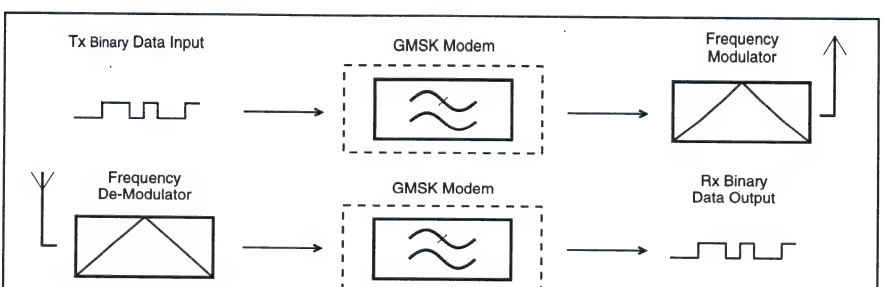


Fig.2 Data Flow in a GMSK FM Radio System

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

GMSK

The diagram below shows GMSK filter outputs for a logic input of "1 0 0 0 1 0 0 0". Note that a filter delay is present and that the individual output pulse spreads across more than one bit-period.

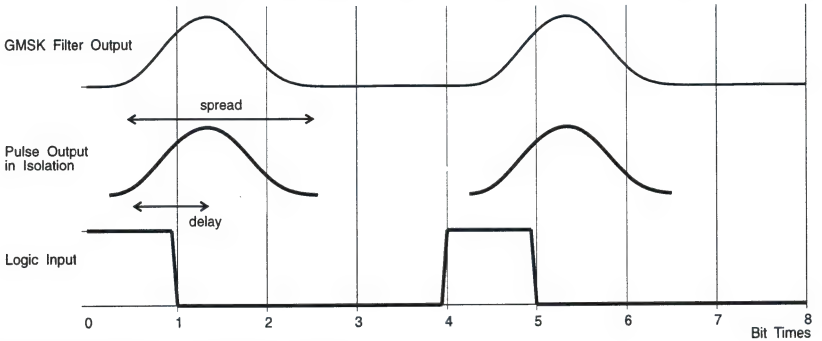
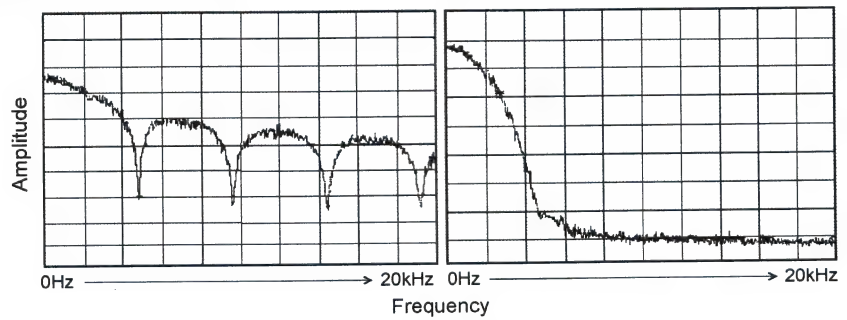


Fig.3 GMSK Filter Input/Output Relationships

True GMSK transmission, in radio, is achieved when the 'data' output of the Gaussian filter is passed through an FM modulator having a continuous phase response, with the peak deviation being set to half of the applied bit rate.

$$\text{Max deviation (Hz)} = \frac{\text{Data Rate}}{2}$$

For example, DEV_{MAX} = 2kHz for a data rate of 4kbits/sec.



Figs.4a/b Spectral Comparison of FSK and Gaussian MSK Requirements

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Implementation of GMSK using the MX589

GMSK, as a form of modulation for high-speed data transfer is relatively simple to implement as long as careful attention is paid to several points:

Bitrate, BT and Bandwidth

The maximum data rate that can be transmitted over a radio channel depends on -

- Channel spacing
- Allowable adjacent channel interference
- Tx filter bandwidth (BT)
- Peak carrier deviation (Modulation Index)
- Tx and Rx carrier frequency accuracies
- Modulator and Demodulator linearity
- Rx IF filter frequency and phase characteristics
- Use of error correction techniques
- Acceptable error-rate

Data Formats

The receive section of the MX589 gives the lowest bit error rate with data which has a reasonably 'random' structure --the data should contain approximately the same number of 'ones' as 'zeros' with no long sequences of consecutive 'ones' or 'zeroes'.

Coupling of Rx and Tx Signals

Ideally, the Rx demodulator should be dc coupled to the MX589 'Rx Signal In' pin (with a dc bias added to center the signal around V_{BIAS} [= V_{DD}/2]), however ac coupling can be used provided that -

- The 3 dB cut-off frequency is 20Hz (at 8kb/s) or below (i.e. a 0.1uF capacitor in series with 100kΩ). The cut-off frequency requirement changes proportionally with the applied data rate.
- The data does not contain long sequences (in excess of 100 bits) of consecutive ones or zeroes.
- Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of a rf carrier) for the voltage into the MX589 to settle before the 'RxDCacq' line is strobed.

In practical applications, it will usually be possible to arrange for any ac coupling between the MX589 Tx output and the frequency modulator to cut-off at a very low frequency such as 5.0Hz, but ac coupling between the receive discriminator and the input of the MX589 may need to have a shorter time constant to avoid problems with voltage steps at the output of the discriminator when changing channels or when the distant transmitter turns on.

For these reasons, as well as to maintain reasonable BER, the optimum -3dB cut-off frequencies are around 5Hz in the Tx path, 20Hz in Rx, at 8kb/s.

Figure 5 shows the typical static Bit-Error-Rate performance of the MX589 operating under nominal conditions (8kb/s, V_{DD}= 5.0V, Tamb = 25°C, Tx BT=0.3) for various degrees of ac coupling at the Rx Input and the Tx Output.

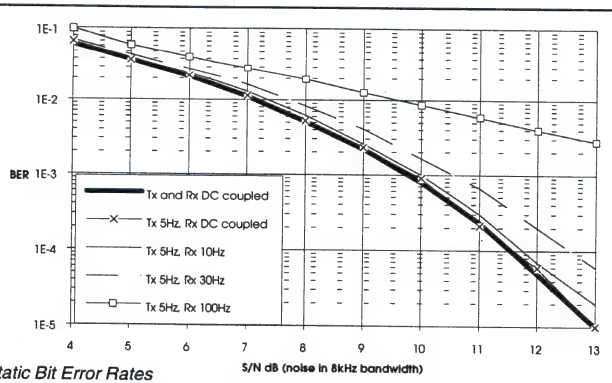


Fig.5 Typical Static Bit Error Rates

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Doc.# 20830074.001

Baseband and RF Bandwidth

The required baseband bandwidth, and hence the RF bandwidth requirement of a GMSK system is principally determined by two factors: the data rate and the system filter's response. The response characteristic with respect to an applied data rate is referred to as the system BT (bandwidth - data rate) factor.
The BT factor is the ratio of the -3dB point of the filter ($-3dBf_0$) and the applied data rate.

$$BT = \frac{-3dBf_0}{\text{Data Rate}} \qquad \text{i.e.} \qquad -3dBf_0 = BT \times \text{Data Rate}$$

As can be seen from Figure 6, a lower BT figure (0.3) allows less high-frequency components and produces, theoretically, a narrower bandwidth requirement. However the interference caused by one bit symbol overlapping another (intersymbol interference) is increased (Figure 7).

The MX589 is capable, within the current specification, of operating to data rates of between 4kbits/s and 40kbit/s at a BT of 0.3 and 0.5; Table 1 provides a very rough guide to GMSK capabilities in narrow RF bandwidths. However the details of the relevant system specification should always be adhered to.
Figure 6 shows the MX589 Tx filter response at BT values of 0.3 and 0.5.

BT	Channel Bandwidth (kHz)	Data Rate Max. (bp/s)	BT	Channel Bandwidth (kHz)	Data Rate Max. (bp/s)
0.5	12.5	4800	0.3	12.5	8000
0.5	25.0	9600	0.3	25.0	16000
0.5	50.0	19200	0.3	50.0	32000

Table 1 Typical GMSK/Bandwidth Capabilities

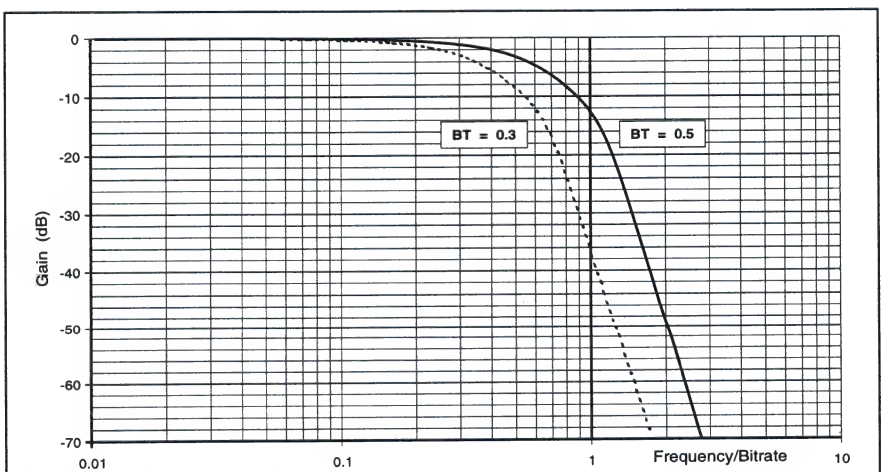


Fig.6 MX589 Tx Filter Response

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Intersymbol Interference

This is the effect of one data bit overlapping the next due to the lowpass filtering. As this effect becomes more pronounced the receiving modem may have trouble deciding whether the bit is a '1' or a '0'.

Figure 7 shows the output of the GMSK modem for an input of "1 1 0 1 1 1 1 1" with BT settings of 0.5 and 0.3; the increasing effect of intersymbol interference can be clearly seen.

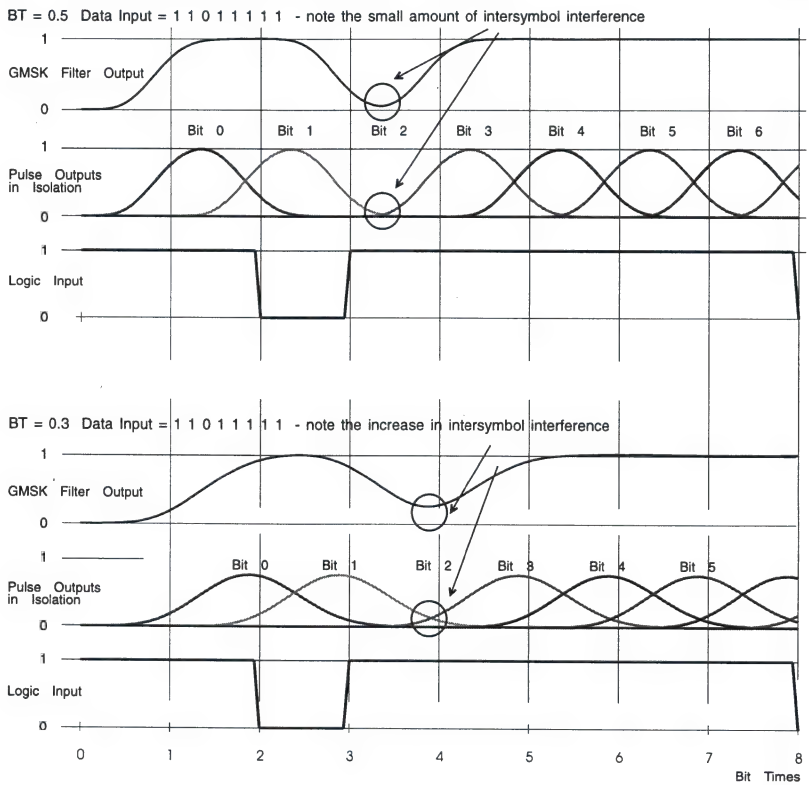

BT = 0.5 Data Input = 1 1 0 1 1 1 1 1 - note the small amount of intersymbol interference
GMSK Filter Output
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Pulse Outputs in Isolation
Logic Input
BT = 0.3 Data Input = 1 1 0 1 1 1 1 1 - note the increase in intersymbol interference
GMSK Filter Output
Pulse Outputs in Isolation
Logic Input
0 1 2 3 4 5 6 7 8
Bit Times

Fig.7 Illustration of Intersymbol Interference Increase due to Decrease in BT Value

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

FM Modulator, Demodulator and IF Performance

The EYE Pattern

The EYE pattern diagram is an oscilloscope-type trace of the baseband signal (at the input to the FM modulator or at the output of the FM discriminator).
It is an indication of the condition of the signal and its path and therefore the FM modulator, demodulator, IF circuit and channel circuit performance.

The EYE diagram provides information about the following parameters of the signal and/or system:

Channel signal/noise conditions -

Channel amplitude and phase responses -

For optimum performance, the EYE pattern of the received signal applied to the MX589 for random transmitted data should be as close as possible to the examples given in Figure 9.

Of particular importance are general symmetry, cleanliness of the zero-crossings, and for a BT of 0.3, the relative amplitude of the inner eye opening (which should be approximately 0.48 of the total for a BT of 0.3, about 0.9 for a BT of 0.5).

To achieve this, attention must be paid to -

- Linearity and frequency/phase response of the Tx frequency modulator and discriminator. The modulator frequency response should extend down to a few Hertz; two-point modulation is necessary for synthesized radios.
- Bandwidth and phase response of the Rx IF filters.
- Accuracy of the Tx and Rx carrier frequencies -any difference will shift the received signal towards one of the skirts of the IF filter response.

The diagrams on the following pages provide examples of various EYE patterns and their causes.

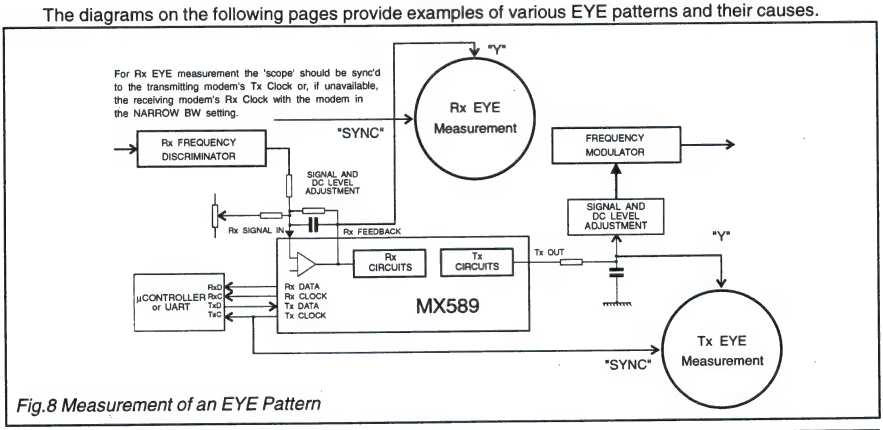


Fig.8 Measurement of an EYE Pattern

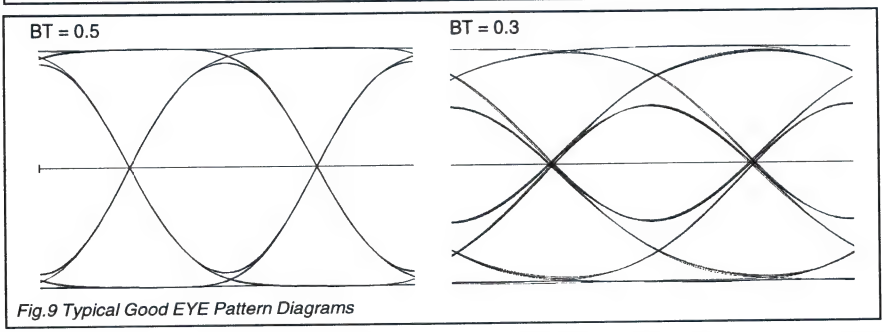


Fig.9 Typical Good EYE Pattern Diagrams

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Example Rx EYE Patterns

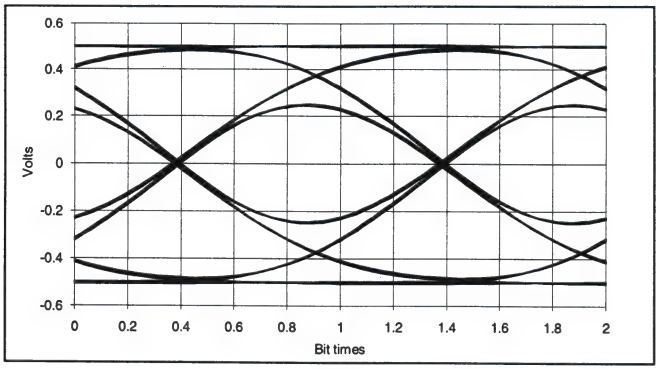


Fig.10 Good Rx EYE
(BT = 0.3)

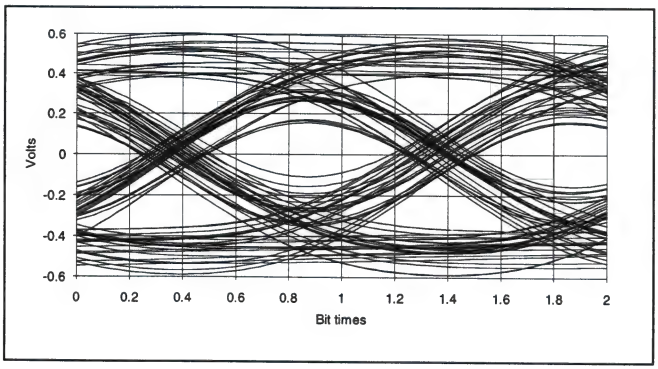


Fig.11 Effect of AC Coupling
(BT = 0.3)
(corner frequency approx. 1% of bitrate)

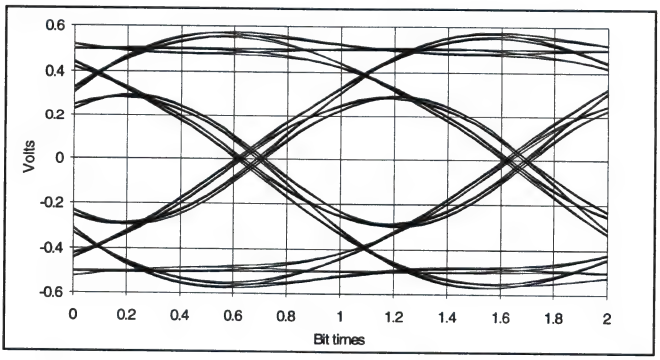


Fig.12 Effect of Poor Channel Amplitude and Phase Response
(BT = 0.3)

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Example Rx EYE Patterns .....

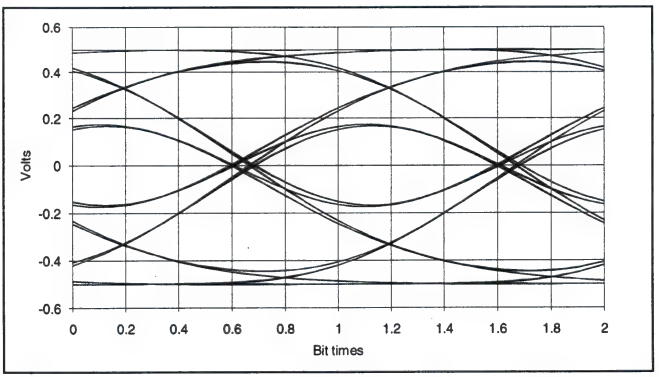


Fig.13 Effect of Slight High Frequency Attenuation

(BT = 0.3)

(6dB/octave low pass filtering, -3dB at 0.5 x bitrate

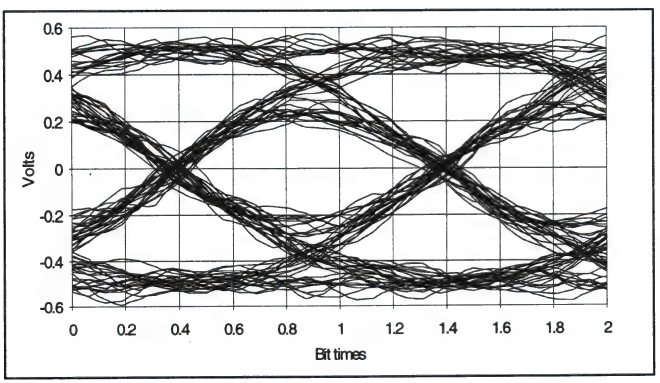


Fig.14 Effect of Noise

(BT = 0.3)

(noise bandwidth = 2 x bitrate; S/N = 25dB)

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Data Sequencing

To ensure that the MX589 Rx clock recovery and Rx level circuits are given the best opportunity to operate correctly the receive section works best with data which has a reasonably 'random' structure. The data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences of consecutive 'ones' or 'zeroes'. Also, long sequences (>100 bits) of '10101010 ...' patterns should be avoided. For this reason, it is recommended that data is scrambled in some manner before transmission.

A string of logic 1's will be modulated as a single frequency shift at the beginning of the string and a single frequency shift at the end; no frequency changes will occur. This will appear at the Rx modem as near dc and can result in the receiver not being able to track the incoming signal correctly. Both bit timing and level information can be lost.

Particularly when a BT value of 0.3 is being used problems also occur when single bits bounded by their complement are being sent repeatedly ('0 0 0 0 0 1 0 0 0 0' or '1 1 1 1 0 1 1 1 1' note however, that these are not the only patterns to give problems); these sequences sent many times over can cause the GMSK demodulator to give out bits in error.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble should be at least 16 bits long, and should preferably consist of alternating pairs of '1's and '0's i.e. '110011001100 .....'; the pattern '10101010 ....' should be avoided, particularly when BT = 0.3.

Many FSK and FFSK data systems use a '1 0 1 0 1 0 1 0 . . .' pattern as a synchronizing preamble, Figure 15a shows the resultant output from a system using BT values of both 0.5 and 0.3.
In this case the output of a BT = 0.3 system does not provide true level information for the level measuring circuits to lock onto. When the BT is 0.5 the output does not display the problem to the same degree .

Figures 15b, 15c and 15d show outputs from inputs of '1 1 0 0 1 1 0 0 ....' , '1 1 1 1 0 0 0 0 1 1 1 1 ...' and '0 1 0 0 0 0 1 0 0 ...' respectively. Where it is impossible for data to be provided to the modem within the above guidelines, it is recommended that external sequencing is used; i.e. scrambling or data coding.

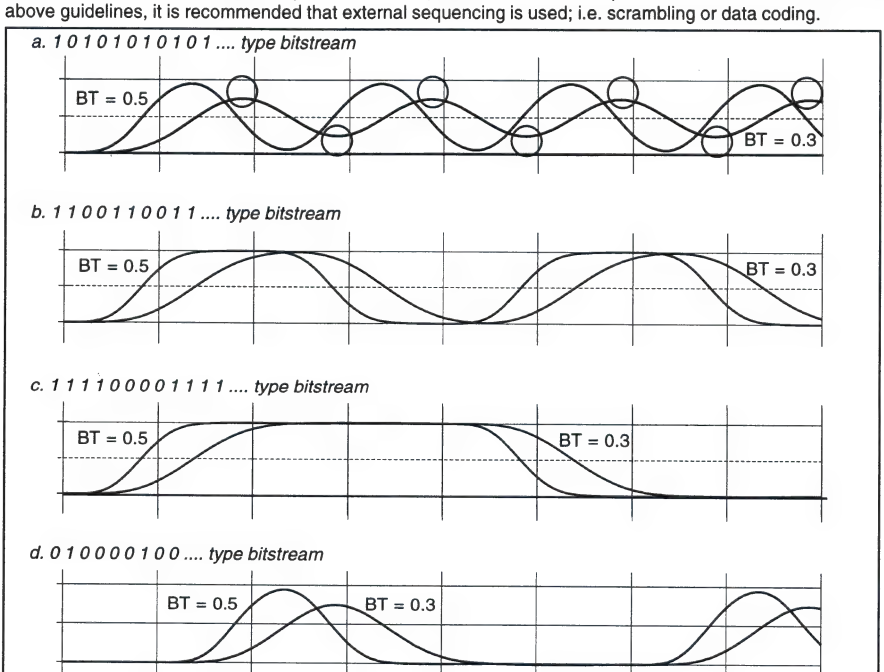

a. 1 0 1 0 1 0 1 0 1 0 1 .... type bitstream
BT = 0.5
BT = 0.3
b. 1 1 0 0 1 1 0 0 1 1 .... type bitstream
BT = 0.5
BT = 0.3
c. 1 1 1 1 0 0 0 0 1 1 1 1 .... type bitstream
BT = 0.5
BT = 0.3
d. 0 1 0 0 0 0 1 0 0 .... type bitstream
BT = 0.5
BT = 0.3

Fig.15 GMSK Output Levels for Various Input Bit Configurations

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Data Randomizing (Scrambling)

As previously discussed, the receive section of the MX589 prefers data which has a reasonably 'random' structure.

Whether the applied data (digital bits) originate from a computer type system or by voice digitization, it is not always possible to ensure that streams of constant-'sense' Rx data are avoided.
One way however is to randomize the data before applying it to the 'modem'.

Illustrated below are two simple ways to randomize data:

1. Exclusive-OR the input binary data with a pseudo-random binary data stream.
   This method will require both Rx and Tx pseudo-random codes to be in sync.

2. Exclusive-OR the input binary data with a shifted input data stream.
   A self-synchronizing method which exclusive-OR's the Rx input data with a time-shifted version of itself. This method of randomizing will propagate bit errors as any Rx bit in error will be duplicated with each EX-OR function in the loop. This method is in accordance with CCITT recommendations (V.26 ter).

Preamble bits and/or SYNC words should not, of course, be randomized.

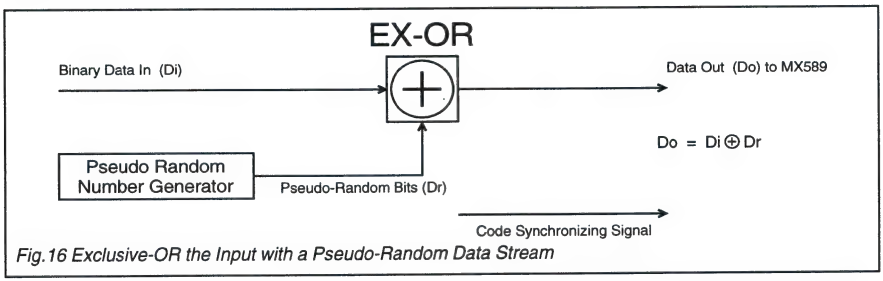


Fig.16 Exclusive-OR the Input with a Pseudo-Random Data Stream

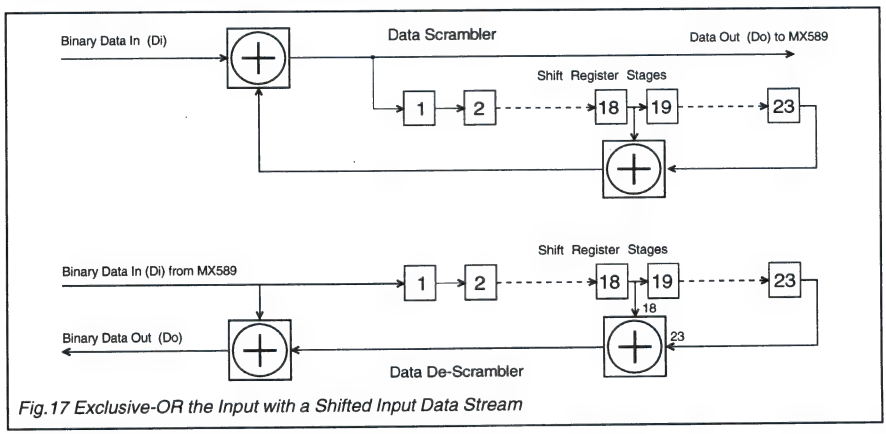


Fig.17 Exclusive-OR the Input with a Shifted Input Data Stream

Data Coding

If it is important, for hardware or system interface considerations, that the lower frequency limit of a GMSK signal is kept above a specific frequency it is possible to deliberately encode the data prior to modulation; for instance where ac coupling is employed or there are PLL control limits.

This entails ensuring that sequences (blocks) of bits that contain low-frequency components are altered to produce the required overall output. This coding can be carried out in software or hardware, as appropriate. It should be noted that if coding that results in an increase in the number of bits is used this will reduce the actual system 'data rate' unless the bit rate is increased, which in turn may take the system outside the bandwidth specification.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Rx 'Acquisition' and 'Hold' Modes

The MX589 may be expected to receive data efficiently under several different signal and configuration conditions depending upon the system formatting and the device coupling methods.

Conditions identified so far are:

Rx with Carrier Detect Indication

Rx with No Carrier Detect Indication

The upper and lower voltage levels of the input signal, after internal filtering, are stored on external capacitors connected to the Doc1 and Doc2 pins. These are used to generate levels inside the device to enable the detection of zero-crossings and to extract the received binary data.

As data is received, the values stored on these capacitors are updated to track amplitude variations and drift, unless 'Hold' is selected in which case the voltages will decay very slowly towards V_{BIAS}.

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude.
Note however, that these pins are driven from very high-impedance circuits, so that the dc load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

Rx Acquisition with Carrier Detect Indication

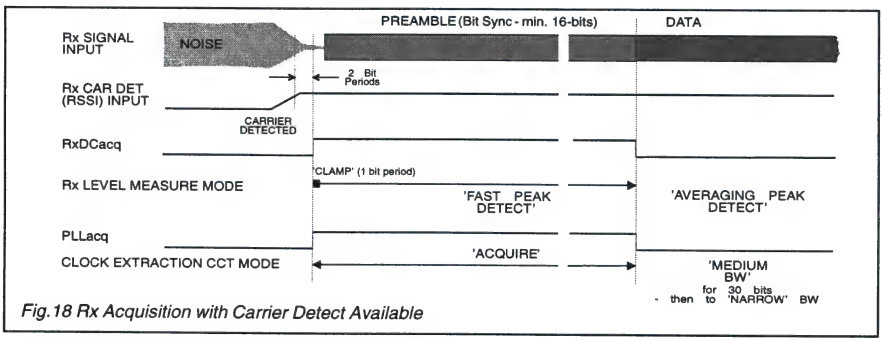


Fig.18 Rx Acquisition with Carrier Detect Available

The MX589 can tolerate dc offsets in the received signal of at least +/- 10%V_{DD} with respect to V_{BIAS}, however to ensure that the dc offset compensation circuit operates correctly and with minimum delay, 'Low' to 'High' transitions of the 'RxDCacq' and 'PLLacq' inputs should occur after the mean input voltage to the MX589 has settled to within about 0.1V of its final value (Note that this can place restrictions on the value of any series signal coupling capacitor).

1. MX589 connected as Figure 2 in the current Data Sheet; inputs RxDCacq and PLLacq 'Low';
2. At the receipt of an RF carrier detect indication to the µC: wait two bit periods; place RxDCacq and PLLacq 'High' ('clamp' - Doc1 and Doc2 capacitors are rapidly charged towards a voltage midway between the Rx signal level and V_{BIAS}). The 'RxDCacq' and 'PLLacq' inputs must be placed 'High' for a minimum of 16 bits at the start of reception to ensure that the dc measurement and timing extraction circuits lock on to the received signal correctly. To confirm that 'lock' has been achieved it may be necessary to employ additional methods of sync detect; such as a frame detection or MX589 S/N output monitoring.
3. To give the MX589 a satisfactory reference level to 'clamp' to, it is recommended that the transmitting station is configured to provide a short period of blank carrier before the data starts.
   To calculate this period the following system parameters should be considered: Tx power-up time + Rx demodulator settling time + Rx ac coupling values [+ 2 bit times].
4. When lock is confirmed the above inputs should be taken 'Low' again and the acquisition circuits operated as described in the Data Sheet.

In most applications, there will be a dc step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the distant transmitter is turned on. Every time a channel change occurs, the preamble/acquire sequence (steps 1 - 4) should be performed.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Rx Acquire Sequences

Rx/Data Carrier Indication Available

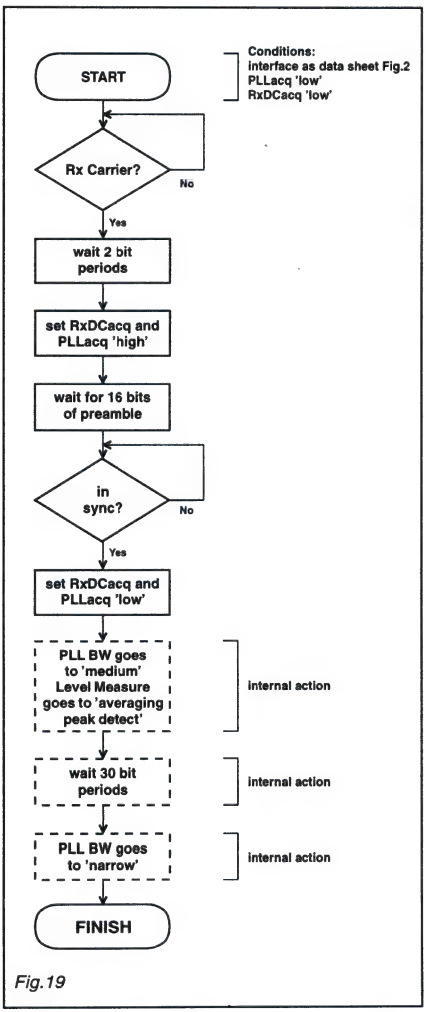


Fig.19

No Rx/Data Carrier Indication Available

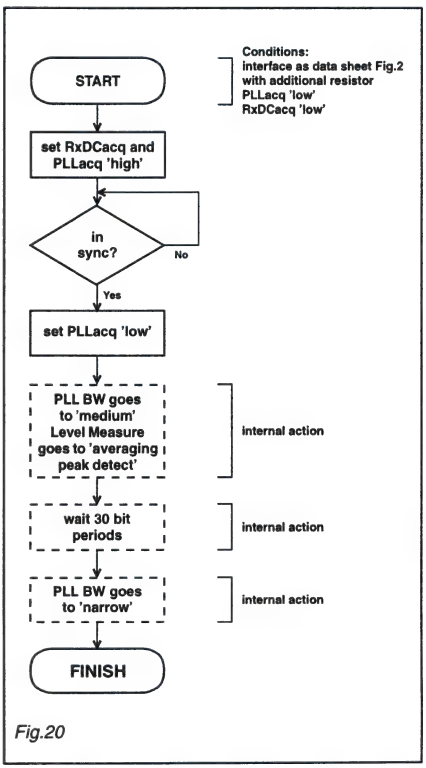


Fig.20

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

'RxHold' Input

As well as using the 'Rx Hold' input to freeze the Level Measuring and Clock Extraction circuits during a signal 'fade', it may also be used in systems which employ a continuously transmitting control channel to freeze the receive circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this, the MX589 'Xtal' clock needs to be accurate enough that the derived 'RxClock' output does not drift by more that about 0.1 bit time from the actual received data timing during the time that the 'RxHold' input is 'Low'.
The 'RxDCacq' input, however, may need to be pulsed 'High' to re-establish the level measurements if the 'RxHold' input is 'Low' for more that a few hundred bit-times.

Rx Acquisition with No Carrier Detect Indication

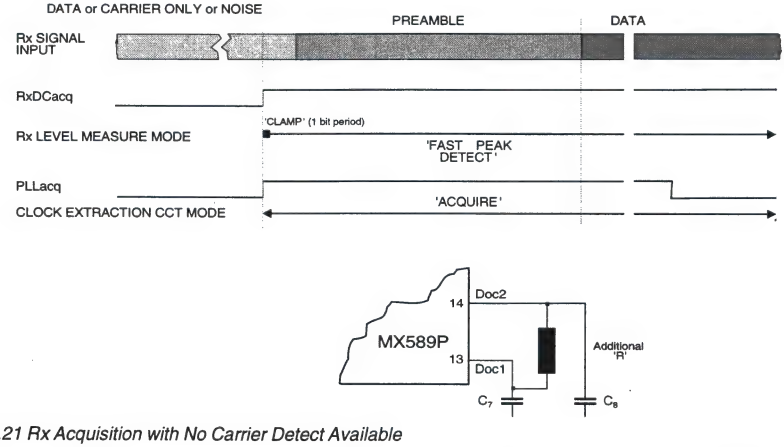


Fig.21 Rx Acquisition with No Carrier Detect Available

If the receive system has no method of indicating when the RF carrier or signal preamble will start it is recommended that:

1. With reference to the current MX589 Data Sheet, Figure 2, a new component, resistor R, of value between 1.0MΩ and 2.0MΩ, should be connected across output pins Doc1 and Doc2.
2. RxDCacq and PLLacq inputs set 'Low'.
3 Before or when the required signal is expected to appear: Set RxDCacq and PLLacq 'High'; the modem acquisition circuits will clamp and then lock and track the data. The RxDCacq pin setting may remain in this position for the duration of operation.
4. The PLLacq pin should be taken 'Low' when lock has been confirmed to improve the signal-to-noise performance by reducing the PLL bandwidth. With the additional resistor, R, connected, there is no advantage in taking the RXDCacq input 'Low' again to attain the Averaging Peak Detect mode.
5. If the received signal has a long preamble sequence, e.g. 100bits, RxDCacq and PLLacq settings may remain low; the circuitry will eventually attain lock.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Interleaving on Systems with Forward Error Correction (FEC)

Data for transmission, with its FEC overhead, is loaded to the MX589 serially. If, during transmission, a section of data bits (block) is corrupted by some external disturbance (ignition interference etc.) there is a possibility that a whole block (or blocks) of data will be damaged making large amounts of data at the Rx uncorrectable and therefore unreadable. This will result in a request for a re-transmission and reduction in the overall data rate.

If however, prior to loading to the modem, the data bits within blocks are interchanged between blocks (interleaved), then if external disturbance is experienced and a section is damaged, when the blocks are rebuilt (de-interleaved) at the receiver only one or two of the bits in each original block of data will be in error therefore allowing the FEC system a better chance of correction.

With reference to the example in Figure 22, interleaving is carried out externally, prior to loading the modem. Data is supplied to the interleaving process in the following sequence (real data):

A1, A2, A3, A4, ...H9, H10

and read-out from the process in the following sequence (interleaved data):

H1, G1, F1, E1, ...H2, G2, ... B10, A10.

De-interleaving is the reverse process.

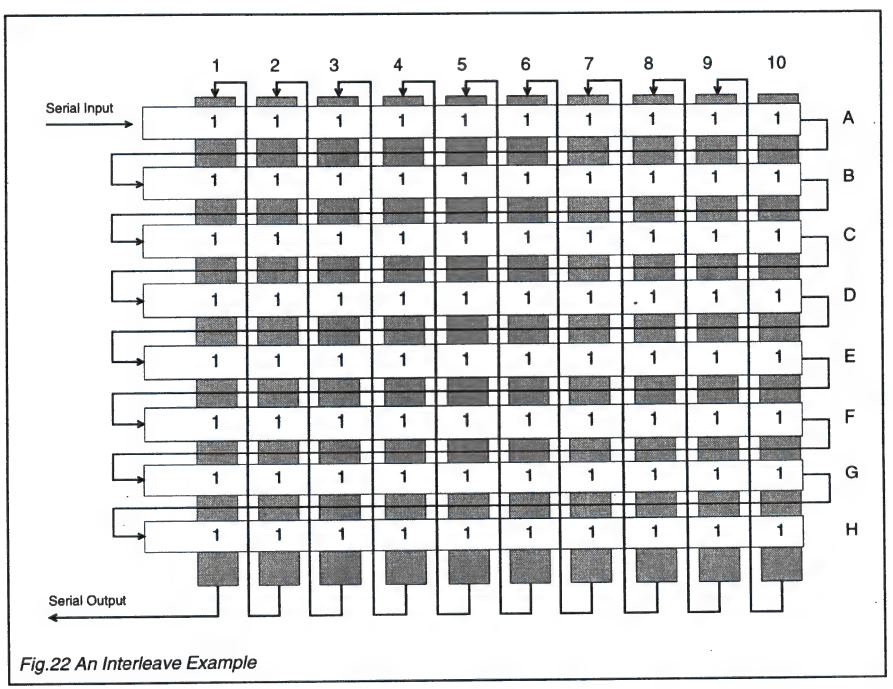


Fig.22 An Interleave Example

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc.# 20830074.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Alternative Data Rates

The current MX589 Data Sheet specifies device operation at data rates of between 4kbps and 64kbps at 5.0 volts and Xtal/clock frequencies of between 1.0MHz and 8.2MHz.

To enable this device to be used, efficiently, in the maximum number of data transfer applications, this Application Note details tables that are intended to provide more information to operate at data rates other than those illustrated in the data sheet.

With due regard to the operating V_{DD} values recommended in the Data Sheet, the following parameters control/affect the data rate operation of this device:

Clock Oscillators and Dividers.

Tx OUT output external component (R_1 and C_1) values.

The values of Doc1 and Doc2 capacitors (C_7 and C_8). Note that peripheral components to the Rx Level Measurement circuitry, should also be considered.

Clock Oscillator and Dividers

The Tx and (nominal) Rx data rates are determined by division of the frequency present at the Xtal pin, which may be generated by the on-chip Xtal oscillator or be derived from an external source. Any Xtal/clock frequency in the range 1.0MHz to 5.0MHz (V_{DD} = 3.0V) or 1.0MHz to 8.2MHz (V_{DD} = 5.0V) may be employed, depending upon the desired data rate.

A division ratio to facilitate data-rate setting is controlled by the logic level inputs on the ClkDivA/B pins. The formula below is employed to calculate the data rate:

$$\text{Data Rate} = \frac{\text{Xtal/Clock Frequency}}{\text{Division Ratio (ClkDivA/B)}}$$

Tx OUT Output Components R_1 and C_1

The RC network formed by R_1 and C_1 is required between the Tx OUT pin and the input to the modulator. This network, which can form part of any dc level shifting and gain adjustment circuitry, forms an important part of the transmit signal filtering. The ground connection to the capacitor C_1 should be positioned to give maximum attenuation of high-frequency noise into the modulator. The component values should be chosen so that the product of the resistance (Ohms) and the capacitance (Farads) is:

BT of 0.3 = 0.34/bit rate (bits/second)
BT of 0.5 = 0.22/bit rate (bits/second)

Doc1 and Doc2 Capacitor (C_7 and C_8) Values

Note the Data Sheet recommendations with regard to these two components:
C_7 and C_8 should both be 0.015µF for a data rate of 8kb/s, and inversely proportional to the data rate for other data rates, e.g. 0.030µF at 4kb/s, 3000pF at 40kb/s.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies

Alternative Data Rates .....

For a Xtal/clock value of 3.6864MHz					
Data Rate (bits/sec)	**ClkDiv** A	**ClkDiv** B	**BT**	**R_1** (kΩ)	**C_1** (pF)
7200	1	0	0.3	100	470
7200	1	0	0.5	62	470
14400	0	1	0.3	130	180
14400	0	1	0.5	130	120
28800	0	0	0.3	62	180
28800	0	0	0.5	62	120

Table 2

For a Xtal/clock value of 4.096MHz					
Data Rate (bits/sec)	**ClkDiv** A	**ClkDiv** B	**BT**	**R_1** (kΩ)	**C_1** (pF)
4000	1	1	0.3	120	680
4000	1	1	0.5	120	470
8000	1	0	0.3	91	470
8000	1	0	0.5	120	220
16000	0	1	0.3	47	470
16000	0	1	0.5	91	150
32000	0	0	0.3	47	220
32000	0	0	0.5	47	150

Table 3

For a Xtal/clock value of 4.9152MHz					
Data Rate (bits/sec)	**ClkDiv** A	**ClkDiv** B	**BT**	**R_1** (kΩ)	**C_1** (pF)
4800	1	1	0.3	100	680
4800	1	1	0.5	100	470
9600	1	0	0.3	91	390
9600	1	0	0.5	47	470
19200	0	1	0.3	100	180
19200	0	1	0.5	91	120
38400	0	0	0.3	47	180
38400	0	0	0.5	47	120

Table 4

For a Xtal/clock value of 8.192MHz					
Data Rate (bits/sec)	**ClkDiv** A	**ClkDiv** B	**BT**	**R_1** (kΩ)	**C_1** (pF)
64000	0	0	0.5	47	82

Table 5

Note that this Application Note is intended to be used in conjunction with the current MX-COM Product Data Sheet; printed Specifications apply. MX-COM does not assume any responsibility for the use of any circuitry described. No circuit patent licences are implied and MX-COM reserves the right at any time without notice to change the said circuitry.

MX909A Signal Acquisition Principles

1. Introduction

This Application Information publication provides guidance on the correct way of using the automatic level and timing extraction sequences of the MX909A as triggered by the AQLEV and AQBC bits of the Command Register.

The techniques detailed should work in most radio systems but slightly different operation could lead to worthwhile improvements for specific cases. Experimentation will be necessary to evaluate the performance of the procedures in comparison with system requirements.

2. Bit Clock Extraction and Receive Level Measurement Principles

The clock extraction circuits operate by storing on-chip a current best estimate of the bit timing of the received signal. These clock extraction circuits track the timing of the input signal by monitoring the data zero-crossings. They will eventually lose track of the timing if these do not occur for extended periods.

As data is received the device continually updates the current best estimate, unless the 'Hold' setting is selected in which case the estimate is frozen. The input signal can change the internal estimate at a speed related to the bandwidth set (PLLBW).

During acquisition the PLLBW is initially set to 'Wide' and the input signal can then rapidly alter the internal estimate. As the clock extraction circuits home-in on the received data timing the bandwidth is automatically switched to 'Medium' for 30 bits to reduce the amount of jitter and hence improve the BER performance; the setting is then changed to the residual value (as set by the Control Register, PLLBW bits).

The 'Hold' setting is intended to enable clock retention during short fades.

The upper and lower voltages of the input signal, after internal filtering, are stored on external capacitors connected to the DOC1 and DOC2 pins. These are used to generate levels inside the device to enable the detection of zero-crossings and to extract the received binary data. As data is received, the values stored on these capacitors are updated to track amplitude variations and drift, unless 'Hold' is selected in which case the voltages will decay slowly towards VBIAS.

During acquisition the two capacitors are rapidly charged toward the input voltage over 1-bit period (Clamp), the capacitor voltages then follow the input signal using Lossy Peak Detect to quickly establish the upper and lower levels. As the signal is acquired the mode automatically changes to the residual setting (as set by the Control Register, LEVRES bits). The 'Hold' setting is intended to enable level retention during short fades.

Note that to operate correctly in the 'Peak Averaging' mode it is required that bit timing has already been established.

The level extraction circuits require the voltages present during pairs of '1's' and '0's', i.e. the upper and lower values. If '00' and '11' sequences do not occur for periods greater than approximately 100 bits the levels stored will not accurately reflect those of the input wave.:

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA.
All trademarks and service marks are held by their respective companies.
Doc. # 20830075.001

3. Acquisition Operation

The acquisition sequences available to the user of the MX909A are intended for 2 types of system:

1. 'Mobitex' type systems with some form of carrier or signal detect facility.
2. Systems with no carrier or signal detect indication.

In both cases it is assumed that the incoming signal to be detected consists of a bit sync pattern (..11001100..) followed by a system synchronization pattern and that the device is set to raise an interrupt when this occurs (an SFS or SFH task has been set). The following techniques should lead to reliable detection and acquisition of the start of isolated data for most radio systems. (See note on ac coupling).

3.1 'Mobitex-Type' - Carrier Detect Indication Available

The device must lock-on to the incoming signal within the 16 bits of bit sync; to achieve this it is necessary to activate both AQBC and AQLEV acquisition sequences at or before the start of the bit sync, typically during a period of unmodulated carrier which precedes messages. In this case the AQBC and AQLEV automatic sequences can be used with the residual settings for the PLLBW = 'Medium' or 'Narrow' and LEVRES = 'Peak Averaging'. The BER will improve toward its steady value over a period of approximately 30 bits from the start of the bit-sync.

It is important that when the AQLEV acquisition sequence is started the voltage level of the input wave is within, or at worst just outside, the extremes of a '11110000' data pattern.

3.2 No 'Carrier Detect' Available

Where no carrier or signal detect circuitry is available the device has to lock onto the incoming signal with little or no cue from the controlling device, this will of course mean that acquisition will take longer and that decoding errors are more likely.

The MX909A must track the incoming signal continuously for a data signal and the best settings to achieve this will be PLLBW = 'Wide' and LEVRES = 'Lossy Peak Detect'. To initiate this the AQBC and AQLEV bits would need to be set with the residual PLLBW = 'Medium' or 'Narrow' and LEVRES = 'Lossy Peak Detect' or 'Peak Averaging'.

When the synchronization pattern is successfully detected the PLLBW and LEVRES functions will automatically sequence to the residual setting.

Where the device is required to detect a signal in this way it is recommended that the bit sync sequence of repetitive '..0011..' bits is extended from 16 (Mobitex spec.) to ≥64 or that the pre-message unmodulated carrier period is extended. Also it may be found advantageous to lengthen the frame sync sequence to reduce the possibility of frame sync falsing.

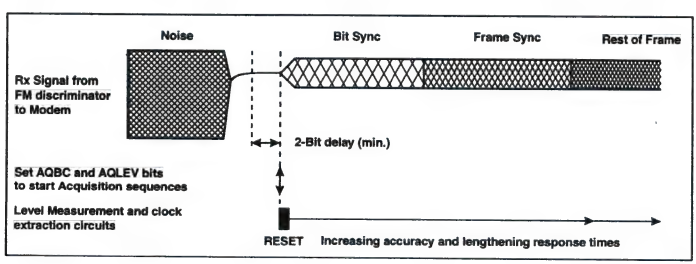

Noise
Bit Sync
Frame Sync
Rest of Frame
Rx Signal from FM discriminator to Modem
2-Bit delay (min.)
Set AQBC and AQLEV bits to start Acquisition sequences
Level Measurement and clock extraction circuits
RESET
Increasing accuracy and lengthening response times

Figure 1: Bit Clock and Level Acquisition Example

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830075.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

4. Acquisition Notes

4.1 Frame Sync Falsing

When noise or an unmodulated carrier is fed into the device the output of the internal bit decode circuits will effectively be random data. This will have the effect of triggering the frame-sync detect circuit whenever this random data matches the frame-sync bytes programmed. There is little possibility of this happening if a Search for Frame Head or Search for Frame Sync task is set just before the beginning of the frame-sync bytes.

However if the device is set to detect a message a long time before it appears, and no carrier detect is available, the possibility of falsing is increased. This problem is aggravated in the case of the Mobitex system which specifies that the frame sync must be detected with up to any one bit in error; this raises the probability of falsing, due to random data, from 1 in 2^{16} bits to 17 in 2^{16} bits.

The user can significantly reduce the chances of falsing by providing extra frame sync bits after those programmed in the MX909A. For example, when receiving a signal with 4 bytes of frame sync the receiving device is programmed with the first two bytes (LFSB), when these are detected using the SFS task, two RSB tasks are issued.

Decoding of the signal only continues if these next 2 bytes match the last two bytes of the 4 byte frame sync otherwise the search would be restarted.

4.2 Short Unmodulated Carrier and Bit Sync Sequences

The most critical case to be met is to use the MX909A in a system where no carrier detect or signal presence indicator is available, the frame-sync is short and the unmodulated carrier is present for a short period.

The device is required to lock-on to the incoming signal within 16 bits whilst also dealing with the potentially large dc and level changes that can occur just before the message is received.

Operating to such a system may result in some proportion of received messages being missed due to frame sync falsing and missing the frame sync bytes due to decoding errors. It is therefore recommended that the MX909A is used in systems with a short unmodulated carrier and bit sync sequences, only if a carrier detect or similar indication is available.

4.3 AC Coupling

The effect of ac coupling is to reduce the static BER performance for a given S/N ratio as it causes low frequencies to be attenuated and cause dc changes to appear as a decaying voltage superimposed upon the signal. A carrier, giving a dc shift, coming on near the start of a message will have the effect of confusing the level detection circuitry and hence cause errors in extracting data. It would be better to delay the message appearing until any dc shift had decayed thus improving the likelihood of correct acquisition. In either case the automatic acquisition sequences can be used.

4.4 Automatic Acquisition Sequences

Sequences of operation for automatic acquisition. For situations when a bit sync pattern is not being searched for (SFS or SFH is not set) the MX909A uses a fixed number of bits delay in switching between the modes:

4.4.1 AQLEV

SFH or SFS is set within 28 bits of AQLEV being set:

1 bit of clamp
Lossy peak detect until frame sync is detected
Residual setting

SFH or SFS is not set: 1 bit of clamp

30 bits of Lossy peak detect
Residual setting

4.4.2 AQBC

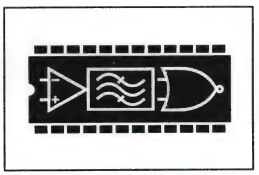
SFH or SFS is set within 14 bits of AQBC being set:

'Wide setting' until frame sync detected
30 bits of 'Medium setting'
Residual setting

SFH or SFS is not set: 16 bits of 'Wide setting'

30 bits of 'Medium setting'
Residual setting

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830075.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.



MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

MX909A Fade Management, Data Detection, and Carrier Drift Management

Introduction

The MX909A is a full function baseband GMSK modem suitable for use in MOBITEX[1] and general purpose wireless packet data applications. It provides several automated functions to support robust, high performance, wireless data links. This document describes issues and strategies relating to fading applications, data detection in continuous carrier systems, and transmit/receive r.f. carrier drift. It also describes pertinent MX909A features and controls which may be used in an MX909A based system.

Fade Management

Synchronous Decoding & Receiver Training

In order to accurately decode a received data stream, a synchronous modem must properly recover its clock and signal components which are then interpreted to reconstruct the transmitted data. Because transmit and receive modems are independent circuits (having separate and different local clock frequencies and signal levels) a receiving modem must be trained or synchronized, immediately prior to each data transfer, to establish a common and coordinated sense of bit timing. In addition, the receiver must also be trained to establish a sense of nominal signal amplitude against which the received data signal is compared to properly interpret its data bit values.

Training is performed by transmitting a specific data stream, the preamble, which provides evident and consistent timing (zero crossing) and amplitude (maximum peak-to-peak range) characteristics. During the training period, a receiving modem adjusts its local clock and level circuits until the known preamble data stream is accurately reconstructed. Once this adjustment is complete, the transmit and receive modems are synchronized and user data can be reliably transferred. (Note that data transfer must immediately follow the preamble or synchronization could be lost due to relative clock and level drift between transmit and receive modems.)

In mobile wireless applications, dynamic changes in the radio channel alter the frequency, phase, and amplitude of transmitted signals. In order to maintain its synchronization through these changes, a receiving synchronous modem may use feedback techniques to dynamically revise its local clock and level circuits according to the changing nature of the received signal.

The Fading Problem

A particularly challenging situation occurs when multipath interference[2] and receiver shadowing dramatically reduce received signal strength, resulting in a loss of input signal required to drive the synchronization feedback system. This can cause a loss of synchronization as the feedback system blindly hunts. Once synchronization is lost, the receiving modem cannot accurately interpret the signal even after sufficient signal strength returns upon exiting from a fade. Through this mechanism, the loss of synchronization can cause the loss of a significant portion (or all) of the 'post-fade' section of a transmission.

Fade Management Strategies

Fades occur in virtually all mobile wireless systems. This has given rise to countless fade management strategies. Three different fade management strategies which may be used individually or in combination are described below.

---

[1] MOBITEX is a trademark of the Telia Corporation.

[2] Multipath interference is the result of a radio signal propagating via multiple paths to reach the same receiver. The multiple paths can be created by reflecting objects which produce an indirect path from transmitter to receiver. Because the multiple paths may be of different lengths the multipath signals, originating from the same source, will likely be out of phase at the receiver's location. At the extreme, the phases of the multiple paths cancel to produce an effective blanking of the received signal.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA.
Doc. # 20830076.001
All trademarks and service marks are held by their respective companies.

Receiver Diversity

Diversity uses multiple receive paths (antennae, etc.) to ensure that at least one of the paths receives a strong signal at all times. Because of its high cost, diversity is usually reserved for special, high availability wireless links.

Limit or Lock Tracking Systems During Fades

Another strategy attempts to maintain synchronization through a fade by constantly or momentarily disabling or limiting the dynamic response of synchronization tracking circuits. If an impending fade can be detected before it becomes too severe, locking or holding the receiver tracking circuits may sustain synchronization until the fade passes. If the hunt rate of the tracking circuits is continuously limited, the total tracking error which accumulates during a fade may be insufficient to cause a loss of synchronization. This approach eliminates the need to anticipate a severe fade.

Tolerate Synch Loss During Fades But Quickly Resynchronize Thereafter

A third strategy uses rapid tracking response to quickly resynchronize after a fade. The rapid response can be applied only upon detecting a fade or it may be constantly used at the expense of a reduced BER[3] in the presence of noise during non-fade periods.

Strategy Selection

Optimum strategies can be based on a combination of the strategies described and can vary widely depending upon the dynamics of the entire system. Fade probability, depth, frequency, and attack/decay rates along with the dynamic response of the complete receiver system (including radio circuits) all influence a wireless link's performance. Aside from diversity techniques, fade management generally involves tuning selected dynamics in the receiver system to best balance performance tradeoffs.

Using the MX909A

The MX909A provides direct program control of the dynamics of its clock and level synchronization and tracking circuits. In addition, it provides automatic macro sequencing of clock and level modes to support a typical frame start synchronization process without the need for low level program supervision. While the automatic operation of synchronization functions is usually preferred, the MX909A provides users the flexibility to implement custom fade management strategies.

Receiver Clock PLL Controls for Acquisition/Tracking

The MX909A uses a phase locked loop (PLL) to adjust and maintain its receiver clock. To most rapidly lock onto a received signal, the PLL dynamic response would be very fast. This can be achieved by using a wide bandwidth feedback system in the PLL. To sustain PLL lock and lowest BER, however, the optimal PLL dynamic response would usually be slower in order to be more stable in the presence of noise. The latter can be achieved by using a relatively narrow bandwidth feedback system in the PLL.

To support optimum system performance, the MX909A PLL provides four dynamic response modes which can be selected at any time under software control. The modes are: Wide Bandwidth, Medium Bandwidth, Narrow Bandwidth, and Hold. The Hold mode stops all PLL tracking adjustments while the others provide varying response.[4] The automatic clock acquisition (synchronization) process first operates the PLL in the Wide Bandwidth mode in order to most quickly lock onto the receive clock signal. At specific times[5], the mode is automatically changed to the next slower bandwidth until the user's previously configured 'normal' (slowest allowed) mode is reached.

---

[3] Bit Error Rate: That proportion of total transmitted bits which are received in error.

[4] It should be noted that differences between transmit and receive clock frequencies will cause a receiver to eventually lose synchronization if the PLL is kept in Hold mode.

[5] Refer to the MX909A data bulletin for a more detailed description of mode shift timing.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830076.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

Level Acquisition and Tracking

The MX909A uses two capacitors, Doc1 and Doc2, on which the peak maximum and minimum ('peak' and 'valley') received signal voltages are integrated and held. These voltages, taken together, establish a sense of nominal peak-to-peak signal amplitude and d.c. level by which to interpret received signals. Each of the peak and valley integration circuits uses a 'leaky' RC filter, comprising one of the 'Doc' capacitors in series with an internal resistor as shown in Figure 1. This method allows the reference levels on the Doc capacitors to adapt as the received signal's amplitude and d.c. bias change.

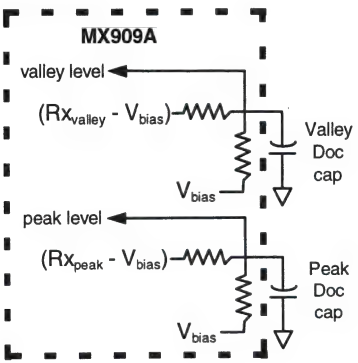


Figure 1, Simplified Schematic of Level Circuit

The MX909A provides four level circuit modes of successively slower response: Lossy Peak Detect, Peak Detect, Peak Averaging, and Hold. Hold disables any capacitor voltage level updates and the capacitor level decays toward V_{bias} at the slowest available rate. These modes provide a range of responses which can be used to both rapidly acquire and subsequently sustain receive signal levels. While an automatic sequence of modes is usually preferred to acquire level voltages, program control can be used to dynamically select different modes to achieve special tuning requirements.

Data Detection

The automatic level tracking functions of the MX909A adapt to receive signal level variations to maintain good BER performance under realistic wireless link conditions. These level tracking and other modem functions are typically activated when link activity is indicated by radio frequency carrier detect circuits. Other systems, however, transmit a continuous carrier which is intermittently modulated with a data stream. In such systems, the automatic level detect functions of the MX909A can adapt to the low receive input signals produced by the discriminator and cause the MX909A to demodulate the quiet channel's noise. Because of the random nature of this noise, occasional frame synchronization patterns may occur and be detected. Such continuous carrier systems require a baseband data detect function to qualify whether frame synchronization search functions should be initiated.

A simple data envelope detect circuit can be constructed using the voltages produced by the level acquisition and tracking circuits inherent in the MX909A (see 0, Level Acquisition and Tracking). Such a circuit observes the Doc1 and Doc2 voltages with a high impedance circuit to ensure that the received signal envelope, indicated by those voltages, is sufficiently high to warrant a frame synchronization search.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830076.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

Extreme Carrier Drift

Although the MX909A tolerates significant transmit carrier/receiver local oscillator frequency differences, a system may desire additional tolerance to compensate for excessive receive local oscillator frequency shifts which can be caused by extreme environmental factors. Such a system requires a signal to indicate the relative error between transmit and receive oscillators. This 'oscillator error' signal can then be used in a local oscillator adjustment circuit to track the transmit carrier frequency.

Relative oscillator error is indicated by a d.c. level shift, relative to V_{bias}, in discriminator output (the MX909A's receive signal input). A simple high input impedance opamp circuit can be constructed to produce such a 'clock error' output signal from the Doc1 and Doc2 voltage levels (see 0, Level Acquisition and Tracking).

Conclusion

The MX909A provides a rich combination of features to support high performance wireless data modem designs. Using the methods described above, a choice of automatic or user defined strategies can be implemented to optimize designs and meet the needs of realistic, high performance, wireless data systems.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830076.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

MSK and its Application to Wireless Data Transmission

1. Introduction

Bandwidth Efficient methods for transmission of data have been and continue to be of great importance to the data dependent community. A community that is experiencing exponential growth. Minimum Shift Keying (MSK) is a continuous phase modulation (CPM) technique that offers advantages in performance and ease of implementation. This paper will provide some insight as to how a simplified MSK modem can be implemented and modeled. The model presented is suitable for a system simulator such as *Ptolemy* from UC Berkeley.

1.1 Background

The academic field of "Data Transmission" is loaded with modulation schemes. Most involve translation of data bits or patterns into a unique combination of phase, frequency or amplitude. Some of the more notable techniques are listed in Table 1.

MODULATION TECHNIQUE	COMMON ACRONYM
Frequency Shift Keying	***FSK***
Multi-level Frequency Shift Keying	***MFSK***
Continuous Phase Frequency Shift Keying	***CPFSK***
Minimum Shift Keying	***MSK***
Gaussian Minimum Shift Keying	***GMSK***
Tamed Frequency Modulation	***TFM***
Phase Shift Keying	***PSK***
Quadrature Phase Shift Keying	***QPSK***
Differential Quadrature Phase Shift Keying	***DQPSK***
$\pi/4$ Differential Quadrature Phase Shift Keying	***$\pi/4$ DQPSK***
Quadrature Amplitude Modulation	***QAM***

Table 1: Modulation formats [6].

Each of the modulation formats listed in Table 1 is suited to a specific application. In general, schemes where two or more bits are represented by a symbol (e.g. QAM, QPSK) require better signal to noise ratios (SNR) than two-level (binary) schemes for similar bit error rate (BER) performance. Additionally, in a wireless system, schemes that have more than two levels (m-ary) generally require greater power amplifier linearity.

Most implementations of the modulation formats listed in Table 1 are synchronous. When data rates exceed 1200 bits/second or when the transmission medium is subject to non-ideal affects (e.g. fading or SNR < 25 dB) synchronous data transmission is preferred over asynchronous. Synchronous data transmission is characterized by the presence of a clock which is synchronous to the data. The clock is embedded in, and therefore recoverable from, the modulated signal. MSK is a synchronous modulation format.

Another important consideration in data transmission is bandwidth. Digitally modulated data, composed of sharp "one to zero" and "zero to one" transitions, results in a spectrum rich in harmonic content that is not well suited to RF transmission. Hence, digital modulation formats that minimize bandwidth (BW) consumption are in vogue. As implied earlier, digital modulation involves the mapping of changes in data states to changes in amplitude, frequency, phase, or some combination of the three. After smoothing the transitions (discontinuities) in phase, frequency or amplitude, we can see, through Fourier analysis, BW consumption is reduced. An entire family of modulation formats, categorized as

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

continuous phase modulation (CPM) minimize BW consumption by eliminating phase discontinuities. CPM state changes are represented by non-abrupt changes in phase and frequency while the amplitude of the carrier envelope remains constant (i.e. phase modulation or frequency modulation).

1.2 Theory of Continuous Phase Modulation

The simplest form of constant envelope modulation is binary FSK. This type of modulation is composed of two sinusoids

$$s_1(t) = \cos \omega_1 t \tag{1}$$

and

$$s_2(t) = \cos \omega_2 t \,. \tag{2}$$

Where $s_1(t)$ is selected for a logic zero and $s_2(t)$ is selected for a logic one. An implementation of the this type of FSK system would appear as shown in Figure 1.

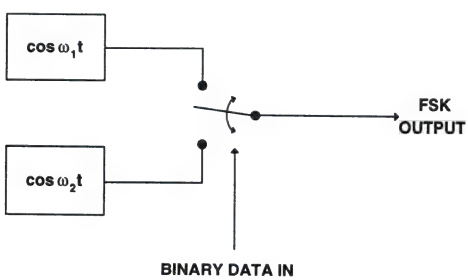


Figure 1:Discontinuous phase FSK modulator.

This type of FSK is referred to as "discontinuous phase" or "non-coherent" FSK because there is no coherence between the phase of ω_1, ω_2 and the modulating signal (BINARY DATA IN). CCITT standard V.21 (300 baud) is an example of non-coherent FSK (f_1 = 1080 Hz and f_2 = 1750 Hz) it has also been applied to other low data rate systems where bandwidth efficiency is not an issue.

An alternative method, to that depicted in Figure 1, for generating FSK is to use a voltage controlled oscillator (VCO) or frequency modulator. The key aspect of the VCO is, for instantaneous frequency deviation proportional to the modulating signal *m(t)*, the phase must be proportional to the integral of the modulating signal. In mathematical terms

$$e(t) = \mathrm{Re}\{A_C \exp[j\phi(t)]\} \tag{3}$$

where, $\phi(t) = \omega_C t + \phi_C + \psi(t)$

$e(t)$ = modulated carrier (FM is a type of angle modulation)

A_C = amplitude of unmodulated carrier

ω_C = angular frequency of unmodulated carrier

ϕ_C = initial carrier phase angle

$\psi(t)$ = instantaneous phase angle due to the modulating signal $m(t)$.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Rewriting equation (3) applying Euler's equation for exponential relations,

$$e(t) = A_C \cos[\omega_C t + \phi_C + \psi(t)] \tag{4}$$

where,

$$\psi(t) = K \int_{-\infty}^{t} m(\tau) d\tau . \tag{5}$$

Here, *m(t)* is the modulating signal and *K* is a constant of proportionality. Substituting (5) into (4) yields the equation for continuous phase FSK (CPFSK).

$$e(t) = A_C \cos[\omega_C t + \phi_C + K \int_{-\infty}^{t} m(\tau) d\tau] . \tag{6}$$

In the case where *m(t)* is bipolar (logic 1 = +1, logic 0 = -1) the integration in equation (5) can be carried out as follows. First we must have an expression which represents the bipolar data signal as shown below.

$$m(t) = \sum_{n=-\infty}^{+\infty} S_n r(t - nT) \tag{7}$$

where, $S_n = \pm 1$, according to bipolar data polarity

r(t) = rectangular pulse with amplitude *1/(2T)* and duration *T*.

Substituting (7) into (5) yields

$$\psi(t) = K \int_{-\infty}^{t} \sum_{n=-\infty}^{+\infty} S_n r(\tau - nT) d\tau \tag{8}$$

$$\psi(t) = K \sum_{n=-\infty}^{+\infty} S_n \int_{-\infty}^{t} r(\tau - nT) d\tau . \tag{9}$$

For the interval $0 \le t < T$

$$\psi(t) = K \sum_{n=-\infty}^{+\infty} S_n \int_{0}^{t} \frac{1}{2T} d\tau \tag{10}$$

$$\psi(t) = K \sum_{n=-\infty}^{+\infty} S_n \frac{1}{2T} t . \tag{11}$$

Using the result from equation (11), equation (6) can be written as

$$e(t) = A_C \sum_{n=-\infty}^{+\infty} \cos[\omega_C t + K S_n \frac{1}{2T} t + \phi_n] . \tag{12}$$

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Where, $nT \leq t < (n+1)T$ and ϕ_n is adjusted according to the phase of the previous symbol ϕ_{n-1}. As a result, if the modulating signal (NRZ binary data) has no impulses, the modulated carrier *e(t)* will not have phase discontinuities. A general representation for CPFSK modulator is shown in Figure 2.

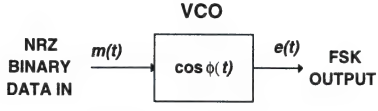


Figure 2:CPFSK generation.

Looking at the term *K* in equation (12)—referred to as a constant of proportionality earlier—for constant envelope modulation systems (e.g. FM) *K* is proportional to the peak frequency deviation of the VCO. For CPFSK, the modulation *m(t)* is NRZ data and

$$K = 2\pi f_d T \tag{13}$$

Where, $f_d = |f_2 - f_1|$

T = symbol or bit period

f_1 = logic zero (S_n=-1)

f_2 = logic one (S_n=+1).

The term f_dT is commonly known as the modulation index *h*. Substituting $2\pi h$ for *K* in (12) yields

$$e(t) = A_C \sum_{n=-\infty}^{+\infty} \cos[2\pi f_C t + \frac{\pi h S_n}{T} t + \phi_n] \tag{14}$$

for, $nT \leq t < (n+1)T$.

For MSK, $h = 0.5$ so (14) can be written as

$$e(t) = A_C \sum_{n=-\infty}^{+\infty} \cos[2\pi \left(f_C t + \frac{S_n}{4T} \right) t + \phi_n] \tag{15}$$

for, $nT \leq t < (n+1)T$.

Consequently, if S_n is +1, the frequency of the carrier is shifted higher to

$$f_2 = f_C + \frac{1}{4T}. \tag{16}$$

When S_n is -1, the frequency of the carrier is shifted lower to

$$f_1 = f_C - \frac{1}{4T}. \tag{17}$$

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Subtracting (17) from (16) yields,

$$f_2 - f_1 = \frac{1}{2T} \tag{18}$$

Equation (18) states, for $h = 0.5$, the frequency separation between f_1 and f_2 is equal to half the bit rate. Figure 3illustrates a set of four waveforms for a typical MSK modulator.

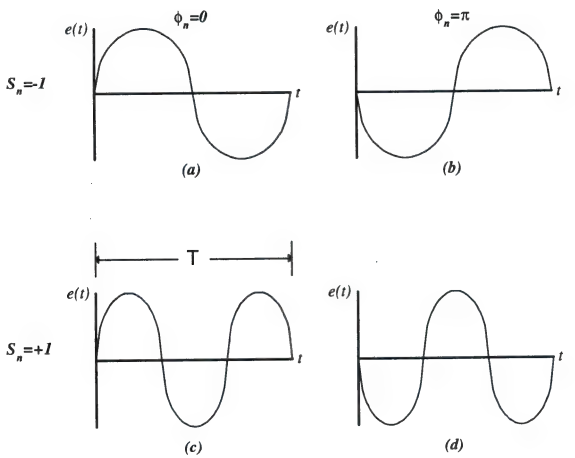


Figure 3: Typical MSK modulator outputs for (a) logic 0 and fn=0, (b) logic 0 and fn=p, (c) logic 1 and fn=0, and (b) logic 1 and fn=p.

In Figure 3 it should be noted that *e(t)* for a logic 1 (S_n= +1) has only one more zero crossing than a logic 0 (S_n= -1). In other words, zero crossing detector must discriminate down to the occurrence of a single zero crossing in order to accurately demodulate the data signal. According to [7], a non-coherent zero crossing detection scheme will perform nearly as well as a coherent detector if the FSK signals are orthogonal. For two signals to be orthogonal over an interval *T*, their inner product must be zero,

$$\int_0^T x(t)y^*(t)dt = 0 \tag{19}$$

where, $y(t) \neq x(t)$ and $y^*(t)$ is the complex conjugate of $y(t)$. If $x(t)$ and $y(t)$ are real then (19) becomes

$$\int_0^T x(t)y(t)dt = 0\,. \tag{20}$$

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

For any FSK system where $\omega_1=2\pi f_1$ and $\omega_2=2\pi f_2$, equation (20) can be written as

$$\int_0^T \cos(\omega_1 t)\cos(\omega_2 t)dt = 0. \quad (21)$$

Performing the integration in (21) yields

$$\frac{\sin(\omega_1-\omega_2)T}{2(\omega_1-\omega_2)}+\frac{\sin(\omega_1+\omega_2)T}{2(\omega_1+\omega_2)}=0. \quad (22)$$

For MSK equation (18) can be rewritten in terms of radian frequency

$$\omega_1-\omega_2=\frac{\pi}{T}. \quad (23)$$

And the radian carrier frequency is

$$\omega_C=\frac{\omega_1+\omega_2}{2}. \quad (24)$$

Substituting (23) and (24) into (22) yields

$$\sin(2\omega_C T)=0. \quad (25)$$

Which has the solution

$$\omega_C=\frac{k\pi}{2T}. \quad (26)$$

Where k is an integer.

As a result, if equation (26) is satisfied, f_1 and f_2 will be orthogonal. In fact, equation (23) represents the "minimum" separation between f_1 and f_2. Hence, the name Minimum Shift Keying. This modulation scheme was first proposed by Doelz and Heald [3] which resulted in a US Patent, assigned to the Collins Radio Company. Figure 4 is a simplified block diagram for a MSK modulation system.

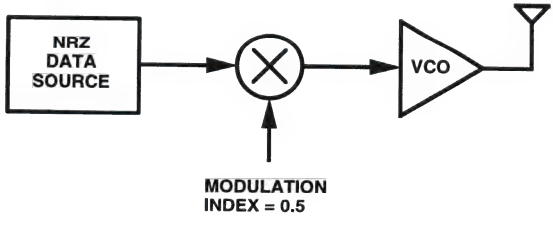


Figure 4: MSK modulator.

A modulation scheme is of little practical value if it can not be demodulated in an efficient manner. The definition of efficiency is somewhat application dependent—in general cost, size, and power consumption must be minimized while performance must be maximized. The performance of a MSK demodulator can be quantified by measurement of the

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

signal-to-noise ratio (SNR) versus BER. SNR is considered by some as an inaccurate method for comparison of performance because of its dependence on noise BW. In other words, the SNR can be significantly altered by varying the system BW. Unless all systems have identical BW it is difficult to make comparisons. A more accepted measure of performance is E_b/N_0 versus BER. E_b/N_0 is related to SNR as shown below,

$$\frac{E_b}{N_0} = \frac{S}{RN_0} = \left(\frac{S}{N}\right)\left(\frac{B_n}{R}\right). \tag{27}$$

Where, S = signal power

R = data rate in bits per second

N_0 = noise power spectral density (watts/Hz)

E_b = energy per bit

$B_nN_0 = N$ = noise power

B_n = noise BW of IF filter.

Figure 5 is a plot of typical performance characteristics for ideal coherent and non-coherent MSK detectors.

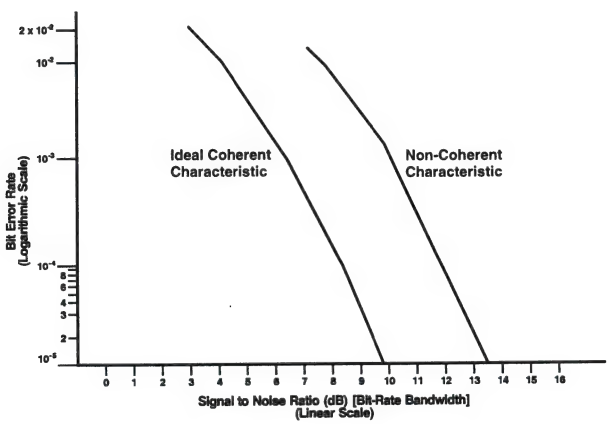

Ideal Coherent Characteristic
Non-Coherent Characteristic
Bit Error Rate (Logarithmic Scale)
Signal to Noise Ratio (dB) [Bit-Rate Bandwidth] (Linear Scale)

Figure 5: BER versus SNR where noise BW equals the bit rate.

2. Implementation

In this section we describe the implementation of a 1200/2400 bit/second MSK modem. That is, a MSK modulator and demodulator including carrier detection and data synchronization.

2.1 MSK modulator

Depending on selected bit rate and digital data input, the modulator generates one of the 1200 Hz, 1800 Hz, or 2400 Hz frequencies. The frequencies for different data rates and bit polarity (logic one or zero) are given in Table 2.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Baud rate (BPS)	TX data in	MSK tone frequency
1200	1	1200 Hz
1200	0	1800 Hz
2400	1	2400 Hz
2400	0	1200 HZ

Table 2: Tone frequencies for 1200/2400 bps MSK modem.

The modulator generates tones that are phase continuous and change frequency at the zero crossings as shown in Figure 6.

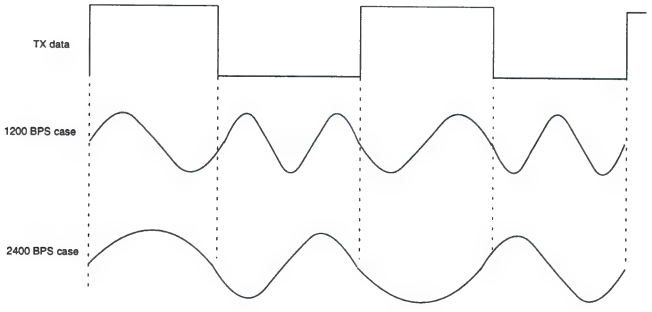


Figure 6: MSK modulator output waveforms.

The modulator block diagram is shown in Figure 7. Primarily, the modulator consists of a digitally controlled oscillator and a low pass filter. The modulation index is 0.5 and the carrier frequency is 1500Hz for 1200 baud and 1800Hz for 2400 baud case. This way of implementing the modulator is sometimes referred to as serial modulation.

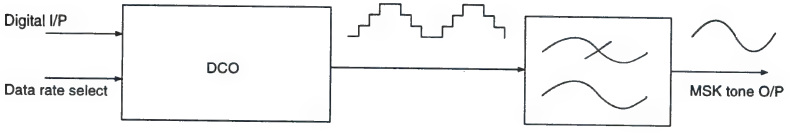


Figure 7: MSK modulator block diagram.

2.2 MSK demodulator

Demodulation is the process of converting the MSK sinusoidal signals to digital ones and zeros. Figure 8 below shows the block diagram of a non-coherent detector. The front end of this detector consists of a band pass filter whose frequency response plot looks similar to Figure 15 for 1200 bps and Figure 16 for 2400 bps. The filter output is sliced to produce a digitized form of the MSK signal, with positive half of the sine wave transformed into high going pulse and the negative half into low going pulse. The monostable is a zero crossing indicator, it produces a pulse every time the input signal changes polarity. The frequency discriminator then differentiates between the two MSK tones based on the zero crossing signal

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

frequency. This detection scheme is non-coherent because the receiver is neither phase nor time synchronized to the transmitter.

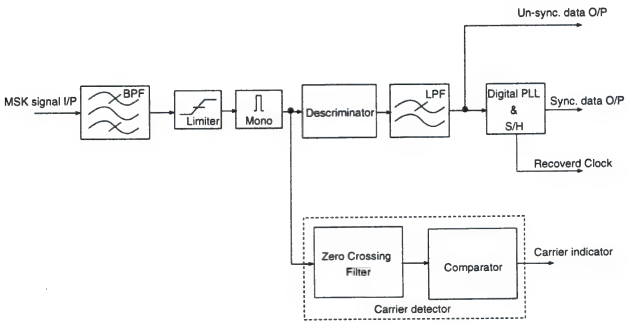


Figure 8: Non-coherent MSK demodulator.

The carrier detector output indicates if MSK signal is being received. The carrier detector works off of the zero crossing indicating signal. The zero crossing filter discriminates between good and bad occurrences of the zero crossings and counts the bad zero crossing occurrences over a pre-defined period. The comparator compares the bad zero crossing count with a pre-set limit to make a decision on the carrier detector output.

The phase locked loop generates a reference clock running at the selected baud rate. The unclocked data output is sampled on the rising edge of this clock to provide synchronized data output. The period of this synchronous clock is adjusted every once per cycle if required to line up the rising edge of the clock with the middle of the unclocked data output.

2.3 Transmit and Receive Synchronization

The modulator provides a transmit reference clock to the user, this clock needs to be used to feed the digital input data to the device.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

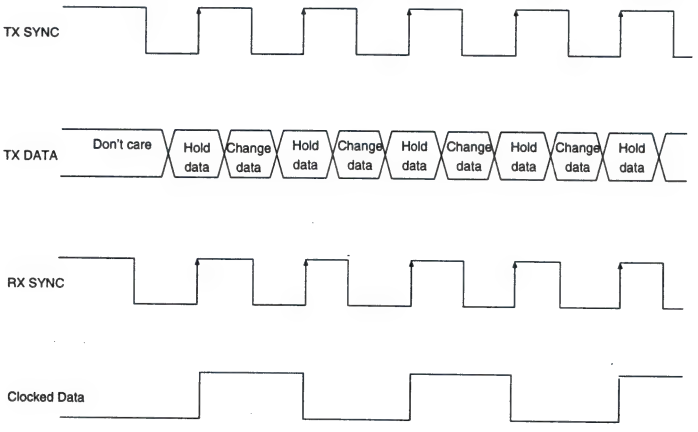


Figure 9: Transmit and receive timing diagrams.

The de-modulator provides the recovered clock and data in reference to this clock. The timing diagrams of the TX and RX sync clocks are shown above. These two clocks can be used to enable synchronous communication between the modem and data terminal equipment.

Figure 10below illustrates an example of how the modem can communicate synchronously with any instrument that has synchronous RS-232C interface.

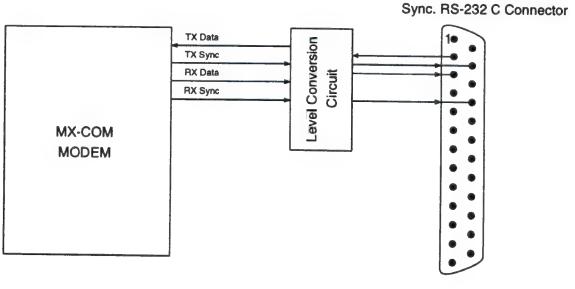


Figure 10: Synchronous RS-232C interface.

2.4 Carrier Detector

The carrier detector is an important feature of the de-modulator. The carrier detect indicator may be used to wake-up or shut down some circuitry in the system to reduce the power consumption.

The carrier detector response time is user controllable via an external input. By altering the state of the external input the user is able to trade sensitivity for response time. In other words, the faster the response the more likely the carrier detect will false on noise and if falsing must be minimized then response time must be compromised.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3. Modeling

With increasing demand to move products quickly to market and to keep costs down, verifying a design through simulation before building a breadboard saves time and money. The rapid growth of PC based simulation tools brings modeling capability to a larger number of design engineers. The verification process can be broken down into three steps:

1. **Creating a model of the design** - Software modeling is a process of emulating hardware blocks of a design. Models can be designed on a hierarchical building block approach. The lowest level models may emulate simple hardware functions such as filters, amplifiers, or digital gates. Several lower level models can be joined together to create more complex models such as modulators or demodulators. These higher level models can be joined together to create even higher level models such as a complete communication system.
2. **Simulating the function of the model** - Simulation is the process of stimulating a model with various inputs and observing the models response. The response of the model can be recorded in plots and data files for analysis.
3. **Analyzing the plots and data collected from the simulation** - Analysis is the process of verifying the plots and data against design goals. This process helps the designer ensure correctness of or see how changes may improve the design.

The models, simulation, plots and pseudo code included in this section were derived using a modeling tool called Ptolemy. Ptolemy is a UNIX based modeling tool that has been ported to run on a PC based UNIX system called Linux. Linux and Ptolemy are freeware software packages and are available to be downloaded from several sites on the internet. One such site is *sunsite.unc.edu*. The Ptolemy home page is http://ptolemy.eecs.berkeley.edu. Other archives sites can be found using a web browser search engine. There are several other PC based modeling tools available from various software companies.

The scope of this document is to model an MSK communications scheme. Each topics will be broken up by function. The topics will include modeling MSK generation and detection (including a description of bit synchronization and carrier detection) and modeling MSK at the system level. The conclusion will review the topics and results presented in this document.

Discrete Time Models

All the models presented below are in the discrete time domain with successive samples uniformly spaced in time. The complete transmitter->channel->receiver model is a multirate system, meaning that different sampling rates are used at various stages in the model. For example the input data bits to be transmitted are sampled at the baud rate either 1200 or 2400 samples per second. The transmitter model's output sample rate is N times the baud rate. The majority of the receiver also runs at this N times rate. We typically used N=60 for the simulation results presented below. The emphasis of this section is on modeling the basic functions included in a typical serial MSK modem offered by MX-COM. RF interfaces and channel models are discussed to aid the reader in developing a complete system model however they are not fully developed. In order to simulate frequency offsets between the transmitter and receiver an interpolating/decimating block that changes the sample rate by M/N can be inserted between the transmitter and receiver. For a 0.1% frequency offset let M=1000 and N=999. For in-depth coverage of multirate processing see [2].

In the following sections, pseudo-code is provided to show the algorithm or function performed by each of the blocks in the model. The authors hope the pseudo-code will aid the readers in modeling and performing simulations of their system designs. The pseudo-code is presented in a simple manner ignoring certain programming considerations such as memory allocation, minimal buffering, type declaration, and scheduling of execution sequence. The models below focus on the core algorithm not the implementation details. Various system simulation environments such as Ptolemy have their own unique ways of dealing with these considerations which are beyond the scope of this paper.

The following conventions are used in the pseudo-code.

// starts a comment which ends at the end of the line

= assignment or comparison depending on context

+ , - , × , / all have their normal meaning. Division is also shown as $\frac{x}{y}$ and multiplication as $x \cdot y$

Y[x] x is the index of array Y, x and Y are used here as an arrays. When referring to an input or output, increasing values of x progress forward in time. Thus Input[x-1] would refer to the previous input to the model at sample x. If a block is multirate, then it consumes more or fewer input samples than it creates output samples. For example the MSK modulator model creates N output samples for every input bit. That is upon processing Input[i], it will create $\text{Output}[N \cdot i]$, $\text{Output}[N \cdot i + 1]$, $\text{Output}[N \cdot i + 2]$, up to $\text{Output}[N \cdot (i+1) - 1]$

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

F(x) function F( ) evaluated with parameter x. For example:

sin(x) is the sinusoidal function of trigonometry

cos(x) is sin(x + π/2)

sinc(x) is sin(x)/x and has the value 1 at x equal 0

sign(x) returns 1 for 0 and positive x and -1 for negative x

for i=0 to N-1 { command sequence } iterates command sequence N times with i increasing by 1 each iteration.

while (expression) { command sequence } repeats command sequence as long as expression remains true.

if (expression) { seq. 1 } else {seq. 2} executes seq. 1 if expression is true otherwise executes seq. 2.

3.1 MSK Modulation

MSK modulation is the process of converting digital data to sinusoids that represent digital data values. In MSK modulation digital data must be converted to a bipolar representation of the data. The bipolar data is then modulated with a modulation index of 0.5. The resulting frequencies are equal to the carrier frequency plus and minus one forth of the baud rate. The initial phase constant of the VCO determines whether data transitions occur at the signal peak (i.e. cos MSK) or the zero crossing (i.e. sin MSK).

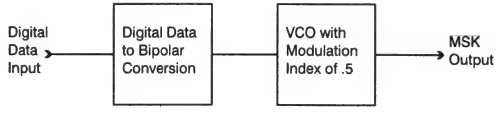


Figure 11: Typical MSK Modulator.

3.1.1 1200 Baud MSK Signals

Figure 12 shows 1200 baud MSK data modulated with a 1500 hertz carrier. MSK sine waves are continuous phase and can only start at zero for a phase constant of zero and pi radians. The first four traces show the sin MSK symbol shapes for data 1 and 0, while the fifth one shows the eye diagram. See Figure 19 for a sequence of bits at 1200 baud.

3.1.2 2400 Baud MSK Signals

Figure 13 shows 2400 baud MSK data modulated with a 1800 hertz carrier. All four symbol shapes are shown followed by the corresponding eye diagram. See Figure 20 for a sequence of bits at 2400 baud.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Pseudo-Code Listing 1 MSK Modulation Model

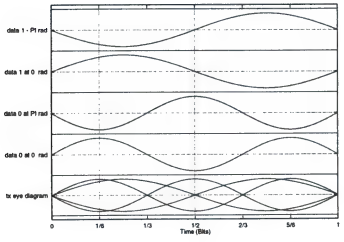


Figure 12: 1200 Baud sin MSK.

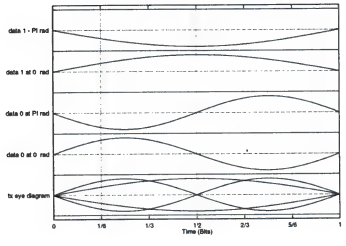


Figure 13: 2400 Baud sin MSK

I/O, Variables, and Constants

```
input[ ]      // transmit data bit array
output[ ]     // output array
N             // interpolation rate -> output sample rate = N x baud rate
2πp[i]        // phase constant in radians  0,π for sin MSK  π/2, 3π/2 for cos MSK
p[i]          // phase constant at sample i has value of  0 or  0.5
Map[0] = 1    // input data 0 mapped to bipolar data 1
Map[1] = -1   // input data 1 mapped to bipolar data -1
c             // carrier normalized to the baud rate
              // 1200 Baud Value = 1.25 = 1500(Carrier)/1200(Baud Rate)
              // 2400 Baud Value = 0.75 = 1800(Carrier)/2400(Baud Rate)
```

Pseudo-Code for MSK modulator

```
dk = Map[input[i]];          // Map input data value (dk) for this symbol.
for n=0 to N-1 {             // Generate N output samples per input bit
```


All trademarks and service marks are held by their respective companies.

$$\text{output}[N \cdot i + n] = \sin\left(2\pi\left[\left(c + \frac{dk}{4.0}\right) \cdot \frac{n}{N} + p[i]\right]\right);$$

}

$$p[i+1] = \text{fractional remainder of } \left(p[i] + c + \frac{dk}{4.0}\right); \qquad \text{// calculate phase constant for next input bit}$$

3.2 MSK Demodulation

MSK Demodulation is the process of converting Sinusoids to digital data. MSK demodulation looks for specific frequencies that represent digital data. Shown in Figure 14is a block diagram for a typical MSK demodulator. MSK demodulation can be broken down in to three sections, signal demodulation, bit synchronization and MSK carrier detection.

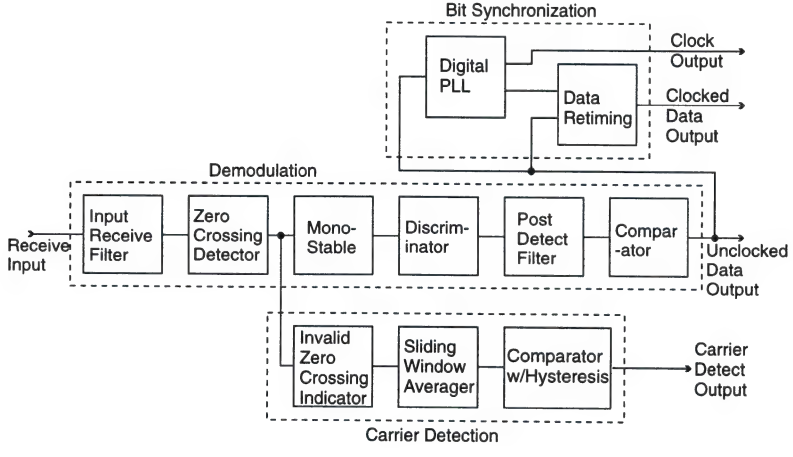


Figure 14: MSK Demodulation Block Diagram.

3.2.1 Demodulator

The MSK detector demodulates the digital information from the received analog signal. There are six blocks that make up the detector. Each block processes the output of the previous block. The output of the sixth block is recovered digital data. The blocks are listed below and will be discussed in order of signal progression.

(a) Input Receive Filter

(b) Zero Crossing Detector

(c) Monostable

(d) Discriminator

(e) Post Discriminator Low Pass Filter

(f) Data Slicer/Comparator

3.2.1.1 RX Filter

The receiver's input filter is a band pass filter centered around the main lobe of the MSK spectrum. It is designed to have a passband width equal to the bit rate (i.e. 2100-900 = 1200Hz and 3000 - 600 = 2400Hz). The frequency domain

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

impulse responses for both baud rates are shown below in Figure 15 and Figure 16. These graphs show the magnitude responses of linear phase finite impulse response (FIR) filters. The filter weights are based on a windowed difference of sinc( ) functions such as:

$$\left[\operatorname{sinc}\left(\frac{2\pi \cdot f_H \cdot t}{f_S}\right) - \operatorname{sinc}\left(\frac{2\pi \cdot f_L \cdot t}{f_S}\right)\right] \cdot \text{window\_function}(t) \qquad (28)$$

where:

f_H is the upper cutoff frequency of the bandpass filter

f_L is the lower cutoff frequency of the bandpass filter

f_S is the sampling frequency of the bandpass filter

Most system simulation packages include tools for generating filter coefficients based on spectral templates, thus coefficients are not tabulated. If an infinite impulse response (IIR) filter is used then it should be group delay equalized over the passband. See section 3.4 for a simple model of an FIR filter.

For thorough coverage of digital filters refer to a digital signal processing text book such as [2],[5] or [8].

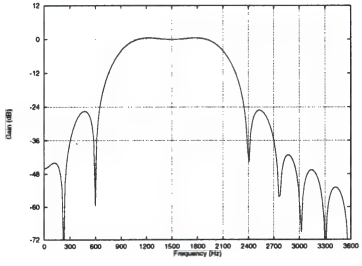


Figure 15: Rx 1200 Baud Filter.

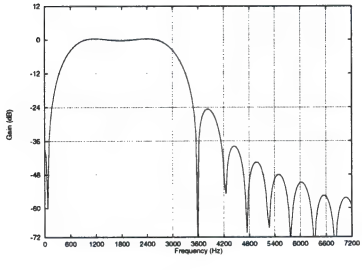


Figure 16: Rx 2400 Baud Filter.

3.2.1.2 Zero Crossing Detector

The zero crossing detector monitors the incoming sinusoid signal from the RX input filter at a rate of N samples per symbol. When the signal passes through zero the output is pulsed high for one sample period. The zero crossing detector then monitors for the next zero crossing.

All trademarks and service marks are held by their respective companies.

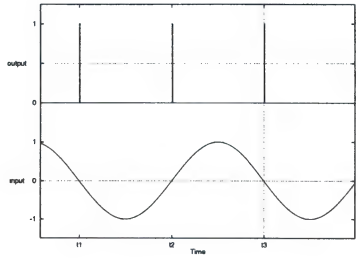


Figure 17:Plot of Zero Crossing Function.

Pseudo-Code Listing 2 Zero Crossing Detector

I/O

input[i] = current input sample

output[i] = current output sample

Pseudo Code

```
if sign(input[i]) != sign(input[i-1])
    output[i] = 1;
else
    output[i] = 0;
```

3.2.1.3 Monostable

The monostable monitors the pulsed output signal from the zero crossing detector. When a pulse is detected the output of the monostable is set high and the timer is restarted. The value of the timer is set to 1/3 a symbol time for 1200 baud and 1/2 symbol for 2400 baud. When the time-out period of the monostable expires the output is set low. If a new pulse is detected on the input before the timer has expired, the timer is restarted and the output remains high. Figure 18 shows the function of the monostable.

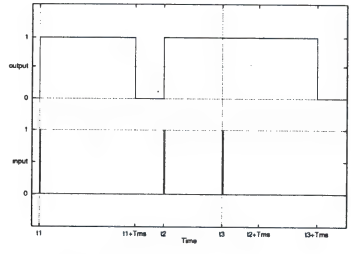


Figure 18: Plot of Monostable Function.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Pseudo-Code Listing 3 Monostable Model

I/O, Variables, and Constants

```
input[i]          // Current input sample
output[i]         // Current output sample
Tms = N/3         // 1/3 Bit time @ 1200 Baud
Tms = N/2         // 1/2 Bit time @ 2400 Baud
timer = 0         // initialize timer first time
```

Pseudo Code for Monostable

```
if input[i] = 1   then   timer = Tms;
if timer > 0      then   output[i] = 1;
                  else   output[i] = 0;
if timer > 0      then   decrement timer;
```

3.2.1.4 Discriminator

The discriminator uses the output signal of the monostable to reconstruct the digital information. In Figure 19 and Figure 20, the operation of the discriminator is displayed. The signals in these figures are under perfect conditions without passing through the receive filter. Under more realistic conditions the output the discriminator looks much less perfect and hence needs to pass through the Post Discriminator Filter to look more like the transmitted bits. See the discriminator output trace in Figure 31 to understand the need for the low pass filter.

3.2.1.4.1 1200 Baud Case

In Figure 19, the TX data in signal is included as a reference to the digital data being decoded. The TX MSK out signal is the modulated signal that is applied to the zero crossing detector. As seen in this signal, a data bit one has 2 zero crossings while a data bit zero has 3 zero crossings per bit time. The monostable output signal is the input to the discriminator. (Refer to the monostable for an explanation of it's output signal). The input signal to the discriminator is time shifted to create two additional signals. The first is shifted by one sixth of a bit time and the second is shifted by one third. These three signal are logically NANDed together to produce the discriminator's output signal. For a logic one the zero crossings are spaced such that the output of the monostable is low for one sixth of a bit time before the middle of the bit and again before the end of the bit. The logical NANDing of the three signals creates a pulse width equal to one half of the bit period for each of the two zero crossings in a logic one. This creates a digital one with the appropriate bit timing. For the zero bit, the zero crossings keep the monostable output high so the NAND output stays low.

3.2.1.4.2 2400 Baud Case

In Figure 20, the TX data in signal is included as a reference to the digital data being decoded. The TX MSK out signal is the transmitted signal for which the discriminator is decoding. As seen in this signal, a data bit with the value of one has 1 zero crossings and a data bit with the value of zero has 2 zero crossings per bit time. The monostable output signal is the input to the discriminator. The input signal to the discriminator is time shifted by one half of a bit period and is logically NANDed with the input. The logical NANDing of the two signals creates the proper bit period. For a zero, the zero crossings keep the monostable output high so the output of the NAND stays low.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

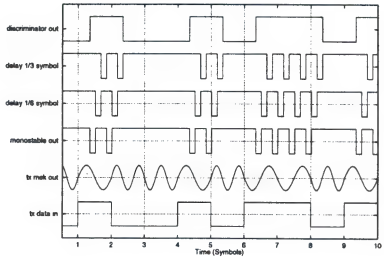


Figure 19:1200 Baud Discriminator Signals.

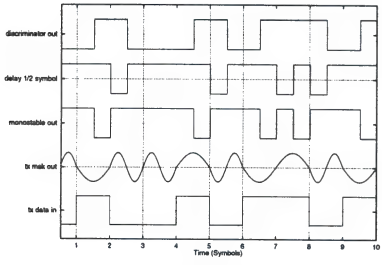


Figure 20: 2400 Baud Discriminator Signals.

Pseudo-Code Listing 4 Discriminator Model

```
I/O, Variables and Constants

    input[i]                        // current input sample
    output[i]                       // current output sample
    Taps[]      = {0, N/6, N/3}     //1200 Baud
                = {0, N/2}          // 2400 Baud
    state                           // variable used to compute logical And of delayed inputs

Pseudo Code for Discriminator       // runs at N x baud rate
    state = 1                       // initialize to true for each input sample.
    for x = 0 to size of Taps-1
        state = state & input[i - Taps[x]]       // compute logical And of each delayed input

    output[0] = complemented value of state      // logical Invert
```

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.2.1.5 Discriminator Low Pass Filter

The discriminator low pass filter is designed to pass frequencies up to half the bit rate. This corresponds to the highest frequency needed to pass an NRZ data sequence 101010... As seen in spectral plots in Figure 21 and Figure 22, the discriminator low pass filter rolls off sharply beyond its cutoff to remove high frequency noise out of the discriminator. These plots depict a finite impulse response filter with weights of a windowed sinc( ) function. See section 3.4 for a finite impulse response filter model.

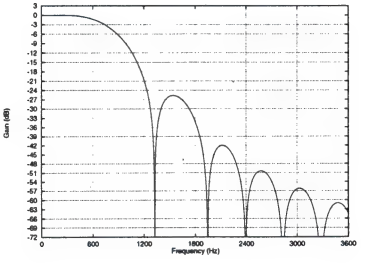


Figure 21: 1200 Baud LPF.

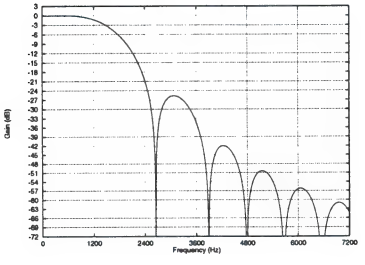


Figure 22: 2400 Baud LPF.

3.2.1.6 Bit Slicer

The bit slicer is simply a comparator with a threshold half way between a one and a zero. That is it outputs 1 for inputs greater than 0.5 and output 0 for inputs less than 0.5. Section 3.4 shows pseudo-code for a comparator. That model provides for hysterisis; however for use as a bit slicer both the upper and lower threshold can be set to 0.5 to essentially eliminate the hysterisis.

3.2.2 MSK Carrier Detection

The carrier detector is made up of three blocks, the bad zero crossing detector, sliding window filter and Comparator with hysterisis. The carrier detect section monitors the information out of the zero crossing detector to determine whether the zero crossing are timed properly for a 1200 or 2400 baud MSK signal. If the zero crossings are properly spaced a logic level is output to indicate that a valid MSK signal is being received.

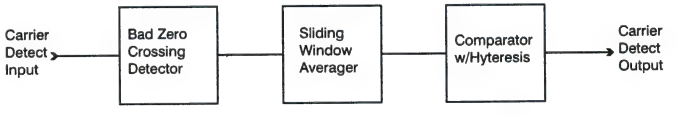


Figure 23: Carrier Detect Block Diagram.

3.2.2.1 Bad Zero Crossing Detector

The Bad Zero Crossing Detector monitors the zero crossings of the filtered input signal. The time between zero crossings is compared against a referenced. If the Bad Zero Crossing Detector determines that a zero crossing is not properly time spaced the output pulses high, otherwise the output remains low. Figure 24 and Figure 26 show the timing windows used for 1200 and 2400 baud. Figure 25 and Figure 27 show that with a properly timed input signal (i.e. zero crossings within the window) the output is low. With an improperly timed input (i.e. zero crossing outside the window or end of window reached) the output pulses high. The windows are based on the ideal zero crossing spacings +/- 5% of the bit time. Thus each baud rate would have two valid windows, however the receive input filter introduces a slight intersymbol interference at symbol boundaries and thus the windows need to widen towards each other to account for this. Since the windows of the 1200 Baud case become very close, a single window is used.

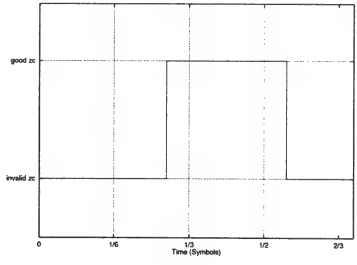


Figure 24: 1200 Baud Valid Zero Crossing Window

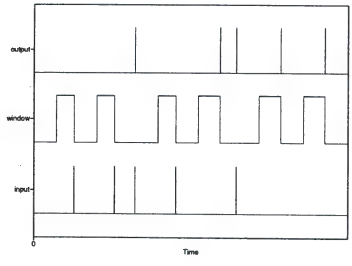


Figure 25: 1200 Baud Bad Zero Crossing Detector.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

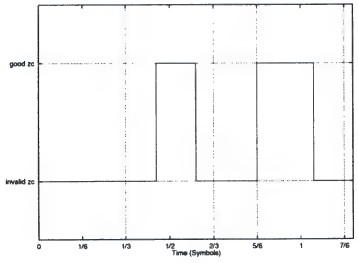


Figure 26: 2400 Baud Valid Zero Crossing Window.

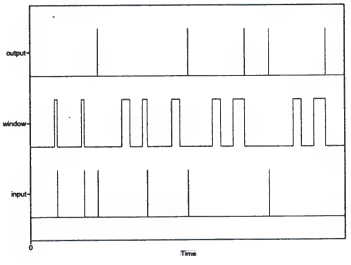


Figure 27: 2400 Baud Bad Zero Crossing Detector.

Pseudo-Code Listing 5 Bad Zero Crossing Detector

```
I/O, Variables and Constants
    input[i]            // current input sample
    output[i]           // current output sample
    START               // Array of valid-window START times
        {Nx0.2833}              // 1200 baud - one window
        {Nx0.45, Nx0.8}         // 2400 baud - two windows
    STOP                // Array of valid-window STOP times
        {Nx0.55}                // 1200 baud - one window
        {Nx0.6, Nx1.05}         // 2400 baud - two windows
    counter             // used to keep track of time since last zero crossing occurred
    OK                  // flag used to indicate properly timed zero crossing
```

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Pseudo-Code for Bad Zero Crossing Detector

```
OK = TRUE;                                  // flag defaults TRUE for no zero crossing input
if (input[i] = 1) {                         // if zero crossing occurs this sample
    OK = FALSE;                             // then flag defaults FALSE and window is checked
    for j=0 to size of STOP and START arrays        // loop over all valid-windows
        if ((counter >= START[i]) & (counter <= STOP[i])) // check if counter is in window
            then OK = TRUE;                         // set flag TRUE if in window
    reset counter;                          // counter is reset at every zero crossing
    }
if (counter > max. value in STOP array)
    then    { OK = FALSE; reset counter; }  // window expired -> spacing is too large for MSK
    else    increment counter;
output[i] = logic inverse of OK;            // output pulses high for bad zero crossings
```

3.2.2.2 Carrier Detect Sliding Window Filter

The sliding window filter maintains a count of the number of bad zero crossings within the last L samples. It can be modeled as a finite impulse response filter of length L with all coefficients set to 1. See section 3.4 for pseudo-code of a finite impulse response filter. To mimic response time of MX-COM's serial MSK modems the length of the window should be eight symbols so L=N x 8 where N is the number of samples per symbol.

3.2.2.3 Carrier Detect Comparator

The carrier detect comparator monitors the output of the sliding window filter to determine if the zero crossing spacings are consistent enough to look like MSK. It has hysterisis to prevent chattering in noisy conditions. The comparator's upper threshold is set to five while its lower threshold is set to one. Thus, it trips to the detect state when there are no bad zero crossings in the last L samples and trips to the non-detect state when there are more than five. Section 3.4 shows pseudo-code for a comparator with hysterisis. That models output should be inverted to have an active high MSK carrier detect.

3.2.3 Bit Synchronization

The Bit Synchronization section re-times the data from the demodulation section. There are two blocks in this section, the Phase Lock Loop block (PLL) and the re-timing block. The PLL creates the clock that is used to re-time the data.

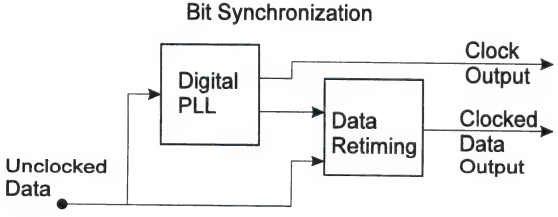


Figure 28: Bit Synchronization Block Diagram.

All trademarks and service marks are held by their respective companies.

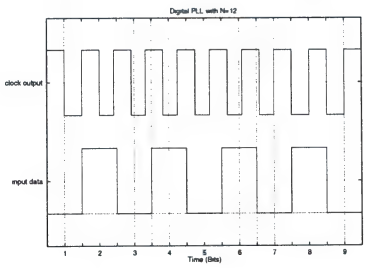


Figure 29: Bit Synchronization Plot.

3.2.3.1 Digital Phase Lock Loop

The PLL aligns the output clock rising edge to the middle of the input NRZ data bit. When the PLL is not aligned with the incoming data a correction factor is applied to the PLL clock period until it becomes synchronized with the incoming data. As seen in Figure 29 the output clock starts out of phase with the data and it becomes synchronized by the end of the plot. In Figure 29 the correction factor used is one 12^{th} of a bit period to more clearly show the locking process

Pseudo-Code Listing 6 Digital PLL

I/O, Variables and Constants

```
input[i]    // current input sample; input is NRZ data
output[i]   // current output sample; output is clock which locks to NRZ data changes
X           // the correction factor  (Note: for MX-COM MSK modems X = 5% bit time)
N           // number of samples per symbol
early       // flag set TRUE if data transition is early
late        // flag set TRUE is data transition is late
counter     // a general counter
reset       // flag set TRUE when algorithm determines it is time to reset counter
```

Pseudo Code for First Order Digital PLL

```
reset = 0;
if  counter<N/2-(0.5X) and input[0] not equal to input[1]        // set early flag
    then    early = 1;
if counter>N/2+(0.5X ) and input[0] not equal to input[1]        // set late flag
    then    late = 1;
if counter is equal to N - 1 - X and early and NOT late          // apply correction factor
    then    reset = 1;                                           //      by resetting early
if counter is N-1 and NOT early and NOT late                     // apply no correction
    then    reset = 1;                                           //      by resetting on time
if counter is N-1 and early and late                             // reset on time since flags conflict
    then    reset = 1;
if counter is equal to N - 1+ X                                  // apply correction factor
    then    reset = 1;                                           //      by resetting late
if counter > N/2                    // set output clock phase based on counter state
    then    output = 0;
```

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

```
    else      output = 1;
if reset is equal to 1  then {          // reset flag is true then reset counter and early and late flags
    counter = 0;
    late = 0;
    early = 0;
    }
    else  increment counter;
```

3.2.3.2 Data Re-timing

The date re-timing block aligns the data to the clock recovered by the PLL. The most common solution is a D flip-flop. The data is applied to the D input of the flip-flop and the PLL output clocks the data through the flip-flop. A model of a D flip-flop is shown in section 3.4.

3.3 System Simulations

Figure 30 shows an MSK system consisting of a transmitter, noisy channel, and a receiver. By simulating a complete system with the models defined above, various signals are plotted in Figure 31. The transmit data bits have a 16 bit preamble for bit synchronization. The receive filter output shows how noise degrades the band limited MSK signal. This degradation is more clearly seen in the receive filter eye diagrams, Figure 32 and Figure 33. The discriminator output clearly shows the need for the post discriminator low pass filter. The unclocked output exhibits jitter (i.e. variable length bit duration) and shows the need for sampling it in the middle of the bit to reliably recover it. The clocked data output shows relatively little jitter in the re-timed data. Additionally the carrier detect output and internal signals are shown to help the reader understand their function. While the transmitter is not enabled many bad zero crossings are indicated. These keep the sliding window filter output from going below the carrier detect threshold. After the start of transmission few bad zero crossings are seen and the carrier detect output trips high when the sliding window filter output goes below the threshold.

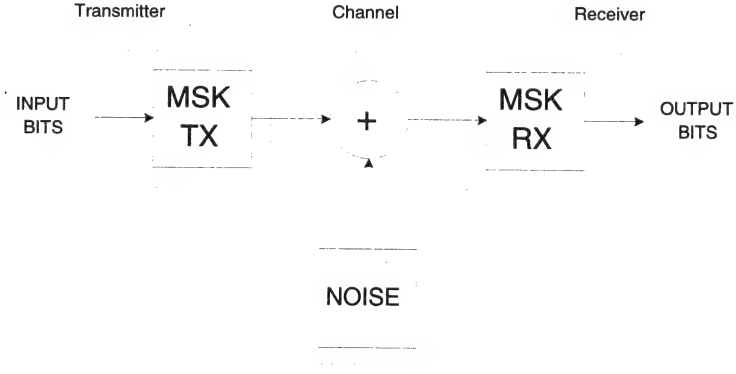


Figure 30: MSK Communications System with Noisy Channel.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

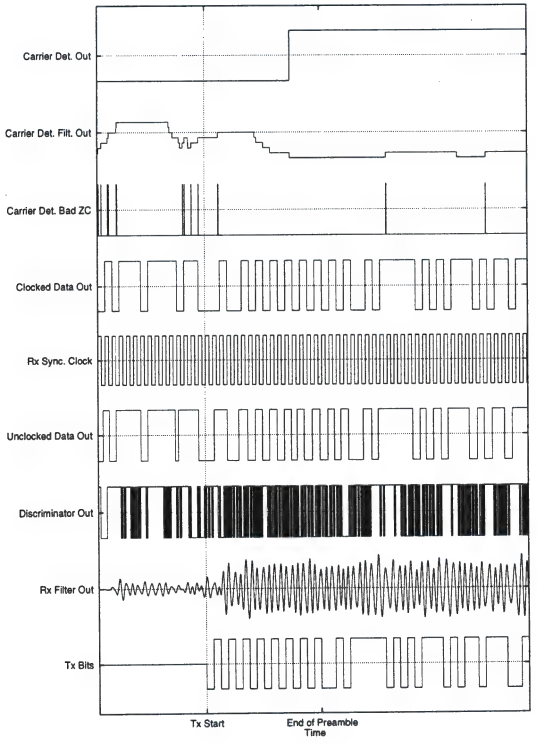


Figure 31: System Simulation Signals for 1200 baud at 12dB SNR

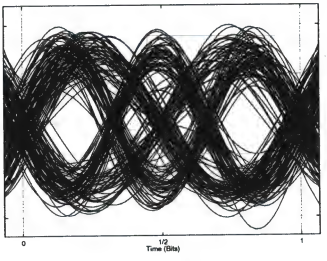


Figure 32: RX Eye Diagram for 1200 Baud at 12dB SNR.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

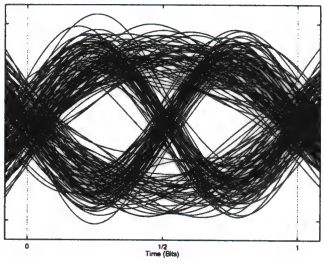


Figure 33: RX Eye Diagram for 2400 Baud at 12dB SNR.MSK Simulations with various SNR

Figure 34 shows the simulated bit error rate performance of the system depicted in Figure 30. The channel is assumed to be additive white gaussian noise (AWGN). In the simulations the noise source produces white noise from DC to half the sampling rate. Thus the total noise power is much higher than the noise in the bit rate bandwidth. Equation (29) computes an effective SNR from a measured SNR assuming white noise over the measurement bandwidth.

$$SNR_{Eff} = SNR_{Meas} + 10\log\frac{BW_{Meas}}{BW_{BitRate}} \tag{29}$$

which can be rearranged as:

$$SNR_{Meas} = SNR_{Eff} - 10\log\frac{BW_{Meas}}{BW_{BitRate}} \tag{30}$$

To adjust the effective SNR to 12dB assuming:

AWGN source is a random variable with zero mean and variance = $\sigma^2 = 1$ i.e. dB power = 0dB.

MSK peak signal level = 1 i.e. signal power = 20log(RMS voltage level) = $20\log\left(\frac{1}{\sqrt{2}}\right)$ = -3dB

and a sampling rate 60 times the baud rate i.e. BW_{Meas} = 30 times the baud rate

$$\text{Correction Factor} = 10\log\frac{BW_{Meas}}{BW_{BitRate}} = 10\log\frac{30}{1} = 14.77\text{dB}$$

thus SNR_{Meas} = 12dB - 14.77dB = -2.77dB

The SNR without adjusting noise power level is:

$$SNR_{Meas} = 10\log\frac{\text{Signal Power}}{\text{Noise Power}} = -3\text{dB}$$

so it is necessary to decrease the noise power by 0.23 dB so:

$$\text{noise variance} = 10^{\frac{-0.23}{10}} = 0.9484$$

to arrive at other effective SNR we can simply adjust the noise variance by a scale factor:

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

$$\text{scale factor} = 10^{\frac{12-SNR}{10}}$$

The table below shows the required noise variance for SNR near 12dB with the system sampling rate equal to 60 x baud rate.

Effective SNR (dB)	Noise Variance	Scale factor from reference
13	0.753	0.794 = 1/1.259
12	0.948	1 i.e. 12dB is reference
11	1.194	1.259
10	1.503	1.585 = $(1.259)^2$

Table 3: Noise variance for various effective SNR.

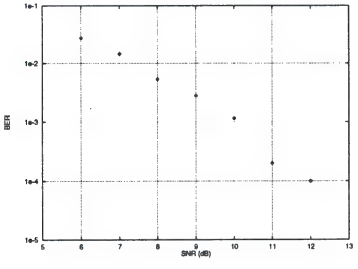


Figure 34: Simulated Bit Error Rate Performance.

3.3.2 FM System

Because of the relatively narrow bandwidth required by MSK, it can often be transmitted over existing analog radio links with little or no modification. Figure 35 is a block diagram of FM transmission of MSK. Pseudo-code models for the key blocks of this system are shown below.

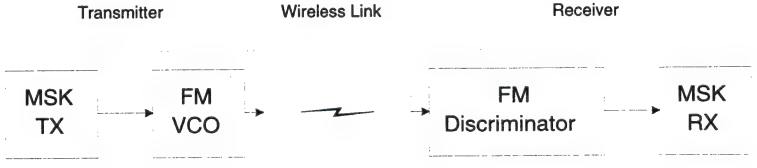


Figure 35: FM Block Diagram.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.3.2.1 FM modulation model

Pseudo-Code Listing 7 VCO based FM modulator model

I/O, Variables and Constants

input[ ] // input sequence

output[ ] // output sequence

IntIn = 0 // variable used to store integral of input[] sequence up to current time.

step // difference between consecutive input samples normalized to interpolation rate M.

carrier // FM carrier frequency normalized to interpolation rate M

deviation // FM deviation frequency normalized to carrier frequency.

$\omega_c = \frac{2\pi \cdot \text{carrier}}{M}$ // carrier frequency constant

$\omega_d = \frac{2\pi \cdot \text{carrier} \cdot \text{deviation}}{M}$ // deviation frequency constant

PSEUDO-CODE // run for each sample, output sample rate is
// M times input sample rate
// use linear interpolation between input samples

$\text{step} = \frac{\text{input[i]} - \text{input[i - 1]}}{M}$;

for j=0 to M-1 {

IntIn = IntIn + input[i-1] + step · j; // simple integrator

output[M · i + j] = $\sin(\omega_c \cdot (i \cdot M + j) + \omega_d \cdot \text{IntIn})$;

}

3.3.2.2 FM Discriminator Model

A simple heterodyne discriminator model based on Figure 35 can be built with multipliers, delays and filters. Pseudo-code is shown for the mixer and the discriminator.

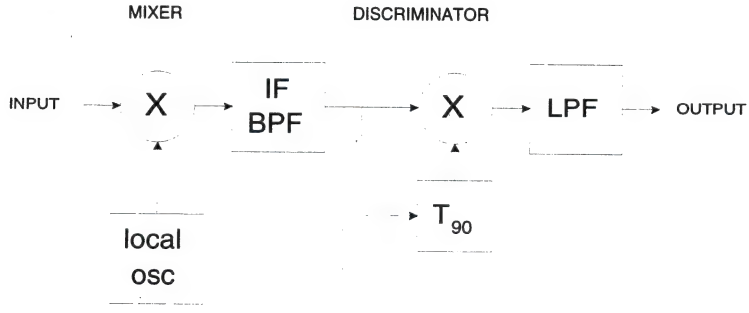


Figure 36: Heterodyne Discriminator Block Diagram.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Pseudo-Code Listing 8 Mixer

I/O, VARIABLES and CONSTANTS

RFinput[i] // RF input
IFoutput[i] // IF output
// local oscillator frequency normalized to sampling rate of block

$\omega_c = \frac{2\pi \cdot f_c}{f_s}$ // note f_c is offset from the RF carrier by the IF frequency.

PSEUDO-CODE for MIXER

IFoutput[i] = RFinput[i] $\times \sin(\omega_c \times i)$;

Pseudo-Code Listing 9 FM Discriminator

I/O, VARIABLES and CONSTANTS

IFinput[i] // input to discriminator
DSoutput[i] // discriminator output
T_{90} // Delay equal to one quarter of the IF center frequency

PSEUDO-CODE for DISCRIMINATOR

DSoutput[i] = IFinput[i] $\times$ IFinput[i - T_{90}];

3.4 General Purpose Models

This section list various general purpose models which the authors hope are self explanatory.

Pseudo-Code Listing 10 Finite Impulse Response Filter Model

I/O, VARIABLES and CONSTANTS

input[i] // current input sample
output[i] // current output sample
L // FIR filter order
j // index to previous samples
sum // used to accumulate tap x weight products
weights[0..L-1] // array of filter coefficients

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

PSEUDO-CODE // run for each sample, input and output sample rates are equal

```
sum = 0
j = 0
while j<L {
    sum = sum + (input[i-j] x weights[j]);
    increment j;
    }
output[i] = sum;
```

Pseudo-Code Listing 11 Comparator with Hysterisis

I/O, VARIABLES and CONSTANTS

```
input[i]    // current input sample
output[i]   // current output sample
Hth         // upper threshold
Lth         // lower threshold
```

PSEUDO-CODE // run for each sample, input and output sample rates are equal

```
if (input[i] > Hth)                    // output trips high
    then output[i] = 1
    else if (input[i] < Lth)           // output trips low
            then output[i] = 0
            else output[i] = output[i-1] // output stays same as last output
```

Pseudo-Code Listing 12 D type flip-flop

I/O, Variables, and Constants

```
D[i]    // current input sample
C[i]    //  clock input
Q[i]    // current output sample
state   // used to store sampled
```

Pseudo-Code

```
if (C[i] = 1) & (C[i-1] = 0)    // rising edge of clock input
    then state = D[i];          // sample input
```

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

```
Q[i] = state;                    // output state
```

3.5 References

[1] J.B. Anderson, T. Aulin and Carl-Erik Sundberg, *Digital Phase Modulation*, Plenum Press, New York, NY, 1986.

[2] R. E. Crochiere and L. R. Rabiner, *Multirate Digital Signal Processing*, Prentice Hall, Inc., Englewood Cliffs, NJ, 1983.

[3] M.L. Doelz and E.H. Heald, "Minimum Shift Data Communications," US Patent No. 2,977,417, March 28, 1961. Assigned to the Collins Radio Company.

[4] W. D. Greeg, *Analog and Digital Communication*, John Wiley and Sons, Inc. New York, NY, 1977.

[5] R. A. Haddad and T. W. Parsons, *Digital Signal Processing - Theory, Applications, and Hardware,* W. H. Freeman and Company, 41 Madison Avenue, New York, NY, 1991.

[6] Kostedt, F. and Kemerling, J., "Practical GMSK Data Transmission," Wireless Design and Development, vol. 3, No. 1, pp. 21-25, January 1995.

[7] E. A. Lee and D.G. Messerschmitt, *Digital Communications*, Kluwer Academic Publishers, Boston, MA, 1988.

[8] A. V. Oppenheim and R. W. Schafer, *Digital Signal Processing*, Prentice Hall, Inc., Englewood Cliffs, NJ, 1975.

[9] J.G. Proakis, *Digital Communications*, 3rd Ed., McGraw-Hill, Inc., New York, NY 1995.

[10] T. S. Rappaport, *Wireless Communications - Principles and Practice*, ISBN 0-13-375536-3, Prentice Hall PTR, Upper Saddle River, NJ, 1996

[11] Sklar, B., *Digital Communications: Fundametals and Applications*, Prentice-Hall, Englewood Cliffs, NJ, 1988.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830084.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Using an MX469 MSK Synchronous Modem with an Asynchronous Data I/O

Asynchronous Modem Circuitry

This application note, used with current MX469 product information, outlines the construction of a low-cost asynchronous modem for the transmission of RS-232 data in the form of Minimum Shift Keying (MSK), between terminals by a radio or line medium (see page 157-170 for MX469 information).

The modem circuitry shown in Figure 1 accepts asynchronous data while transmitting synchronous data using the MX469 series modem. The MX469 may be used to transmit data at either 1200 or 2400 bps, depending on the setting of Switch 1 shown in Figure 1. The chart below details the devices used in this application.

Performance Requirement	Associated Circuitry
RS-232 Driver/Receiver Level Translator	Maxim MAX-232
Async to Sync,	Sipex MAS7838
Sync to Async Conversion	
Data Carrier Detection	MX•COM MX469
Controlled RTS/CTS Delay	74HC04 Delay Element
Generation of MSK Signals	MX•COM MX469
Reception of MSK Signals	MX•COM MX469
Interface into Radio System	MX•COM MX469
RS-232 Handshake	Misc. Circuitry

The signals required for an RS-232 handshake for asynchronous data are as follows. A complete definition of each is given at the end of this application note.

DTR	Data Terminal Ready
DSR	Data Set Ready
RTS	Request to Send
CTS	Clear to Send
TXD	Transmit Data
RXD	Receive Data

The Maxim MAX-232 converts the TTL/CMOS input/output levels to ±10V RS-232 input/output levels. On power-up, the data set ready (DSR) signal is set by the MAX-232's DC to DC converter. The incoming data terminal ready (DTR) signal enables the transmitter keying signal.

The request to send (RTS) and clear to send (CTS) signals are level shifted from the RS-232 interface to TTL/CMOS signal levels. When the modem receives an RTS, the RF transmitter and the MSK tone are keyed immediately and a 30 ms to 100 ms timer is started. At the completion of the timing, a CTS signal is generated for the data terminal to allow serial data flow.

The transmit data (TXD) signal is level shifted to the TTL/CMOS levels, and applied to the Sipex MAS7838 sync to async converter circuit. The random timed asynchronous input from the data terminal is synchronized with the transmit clock pulses of the MX469. If a timing error builds up due to the difference of the external asynchronous clock and the synchronous internal timing on the modem, the Sipex MAS7838 will skip a stop pulse to allow an adjustment to occur. The receiving end Sipex MAS7838 will generate a stop pulse and add it into the data flow so that no information is lost.

From the sync to async convertor, synchronous information is then sent into the MX469, which converts the digital '1' into one cycle of 1200 Hz sinewave and a digital '0' into one and a half cycles of 1800 Hz sinewave for 1200 bps and 1200 and 2400 Hz for 2400 bps. This sinewave is then sent on the transmitter through a level adjustment. The signal

© 1997 MX-COM, Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20830068.001

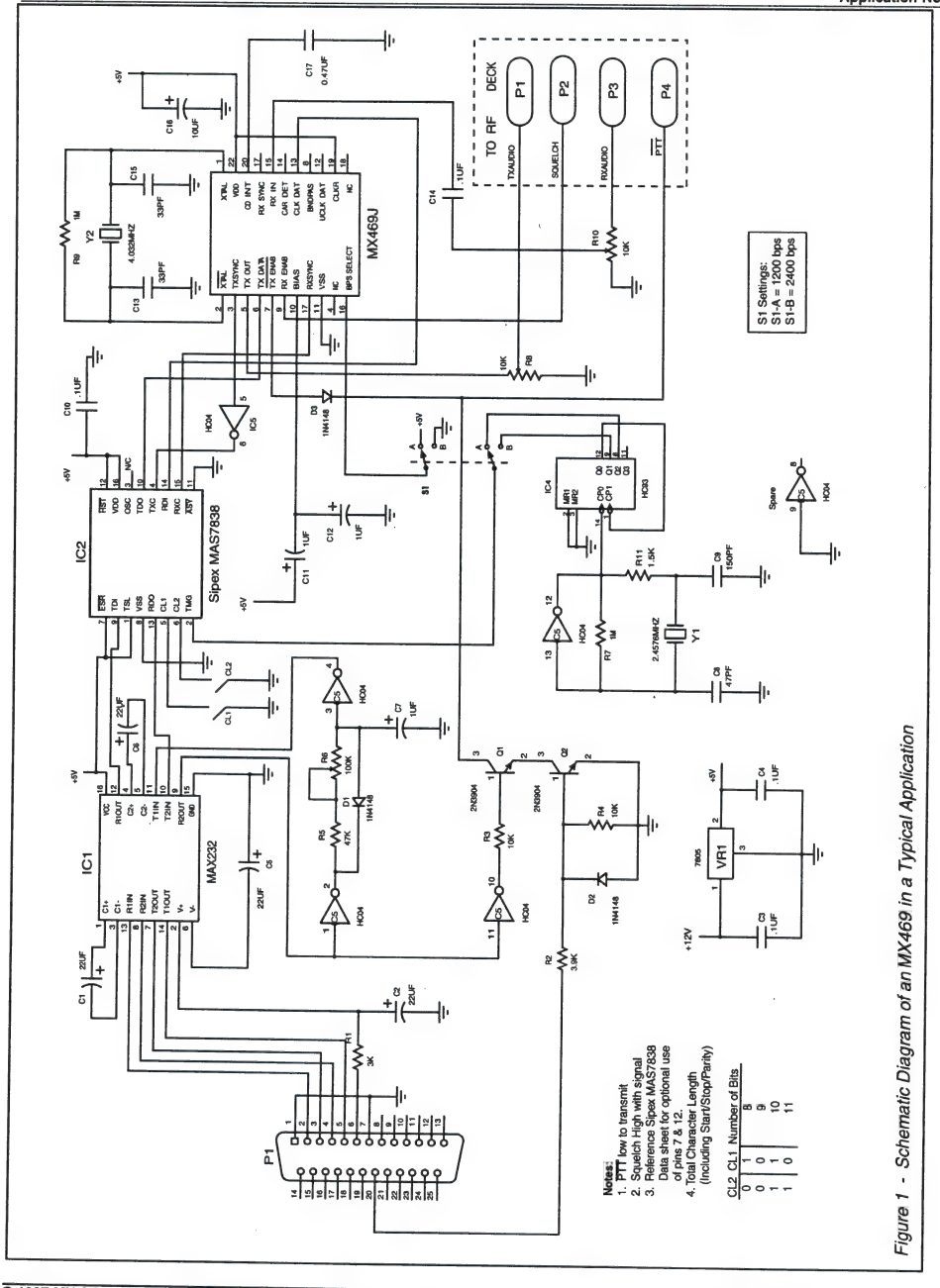


Figure 1 - Schematic Diagram of an MX469 in a Typical Application

© 1997 MX-COM, Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20830068.001

is sufficiently band limited and level controlled to pass FCC type acceptance testing without any additional in-band filtering.

The incoming receiver signal is fed into the MX469 which is held in a power down mode until an RF carrier is detected by the receiver squelch circuitry. This minimizes power drain and also prohibits false information from being sent to the data terminal. If the receiver does not have a noise squelch signal, the chip's carrier detect must be used. It will detect within 12 ms the presence of the data modulation tone. This event is output on the carrier detect pin which should be used to disable the data output to minimize random data at the terminal. The use of the Schmidt trigger circuitry would minimize the 'clatter' at the beginning of the detection signal.

The tones are translated into logic levels and a digital phase lock loop is locked onto the incoming data steam within 16 bit reversals. The detected synchronous data and the recovered receive clock are sent into the Sipex MAS7838 for conversion back into asynchronous data. This information is then sent out to the data terminal through the Maxim MAX-232.

Operation in either a synchronous or asynchronous mode is achieved with a jumper. If additional RS-232 level shifting is needed for transmit and receive clocks and TX and RX enable, pins on the Sipex MAS7838 are brought low. Bringing these pins low bypasses the conversion process and allows synchronous data to pass directly through the device.

Proper clock frequency for the MX469 device is provided by a 4.032 MHz crystal. Clock frequency for the Sipex MAS7838 must be provided at 256 times the bit rate. This is accomplished by using a 2.4576 MHz crystal and dividing down by eight to 301.2 kHz (1200 bps) or by four to 602.4 kHz (2400 bps). Power is derived from a single 7805 voltage regulator. DC current measured on the first model is 12.75 mA.

Software Considerations

As with many data systems, there are certain items that should be addressed within software for proper operation.

Bit sync pattern

The MX469 is a simple data pump that can be used with any protocol by adding the preamble to the start of the protocol. The ability of the MX469 to send and receive data, in a low signal to noise environment, lie in the ability of the receiving modem's phase lock loop to predictively determine the zero crossing of each successive data bit. A preamble must be sent prior to sending meaningful data (such as sync word or data) for the phase lock loop to acquire bit synchronization. A minimum of 16 successive alternating ones and zeros must be transmitted as a preamble to train the receiving MX469's phase lock loop.

This preamble pattern may be accomplished by appending two bytes of $55 or $AA onto the message. Make sure you take into account the stop, start, and parity bits to achieve a minimum of 16 one to zero transitions.

Stop, Start, and Length of Data

Once an RF signal ends, high level noise will be emitted from the receivers's discriminator. Even with data carrier detect or noise squelch circuits to gate the MX469's receiver off, there will be a period of noise (or false data out of the MX469) while muting circuits make a decision. This type of random data often creates problems down stream when applied to the logic controller or point of sale terminal. Having a message bracketed and only dealing with the information between start and stop characters is one method of prohibiting random data from entering the actual message. One should consider methods (or protocol) to distinguish start, stop, and length of data string to discern data burst from random noise.

Microprocessor Interface:

Although this application note depicts using the MX469 without the need of a microprocessor, interface to a microprocessor may also be considered by the circuit designer. Additional flexibility can be added so the microprocessor adds or strips off unnecessary RS-232 bits and adds the required preamble and bit timing to data sent to and from an asynchronous RS-232 port. The microprocessor interface is simple.

The MX469 internally generates a Rx and Rx SYNC clock for the microprocessor to use to synchronize each transmitted or received data bit. This allows the microprocessor to slave its timing to the zero crossings of the MSK modulation method used to conserve bandwidth. Each successive data bit sent from the microprocessor to the TX data input pin must be present and stable while the TX SYNC clock is transitioning from a low to a high. The next bit to be transmitted is sent, on the clock's falling edge. In a similar manner data is read from the Rx CLOCKED DATA output pin on the falling edge of the Rx SYNC clock output pin. Data on the CLOCKED DATA output pin should be ignored while the Rx SYNC clock output pin is transitioning from a logic low to a logic high.

The Carrier Detect output can be used as an additional logic level to indicate an RF carrier is or is not present during data reception.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830068.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Operation with CTCSS or DCS Sub-Carriers

Because the MX469 modems contain a bandpass filter on the input, CTCSS/DCS sub-carriers are filtered out without extra circuitry.

It is important that no energy from the tone section appears within the transmitted data signal passband of 900 to 2100 Hz for 1200 bps or 600 to 3000 Hz for 2400 bps. It is equally important that the tone and data signals are not summed together and sent into the limiter section of the transmitter. The limiter represents a nonlinearity and would generate intermodulation products within the data bandpass which when received generate errors in the decoding of the data. Tone is normally summed into an FM transmitter after the limiting.

Radios designed only for data do not require a speech limiter, allowing tone and data to be summed directly.

RS-232 Handshake

The RS-232 handshake for asynchronous data requires the following signals:

Data Terminal Ready is a signal from the terminal or computer that indicates to the modem that the unit is powered and active. An RF transmission should not be enabled if the Data Terminal is not active.

Data Set Ready is a signal from the modem that indicates to the terminal that the unit is powered and active. Many terminals or computers will not allow data to flow without this condition being true.

Request to Send emanates from the terminal or computer. The software or user has decided that transmission should begin and requests that the RF carrier be turned on.

Clear to Send is a signal that originates from the modem. It is sent in response to a RTS, the request to send signal from the terminal or computer after certain criteria have been met. It is not sent until sufficient time has expired after the transmitter keyed to allow adequate settling time for both the RF transmitter and receiver. It would not be sent if there is an RF carrier on the channel indicating another user. Finally, it would not be sent if a high VSWR were detected on the transmitter when it was keyed. (Not all transmitters are provided with a VSWR detector.)

Transmit Data and Receive Data is the actual asynchronous data flow. Transmit data is data coming from the terminal and Receive data is data flowing into the terminal.

Another term often heard is DTE and DCE ends of RS-232. This refers to what part of the handshake is expected and what the functions of the RS-232 connectors would be. Most often a computer would be programmed to be a DTE or data terminal end of the information flow. When one computer wishes to talk to another computer, it's like two people transmitting on their radios at the same time. Nobody hears the other! If one were to use a 'null' modem cable, the wires are interchanged such that one of the data terminals is now wired like a data communication device. The same is true of two modem devices. A modem device is a DCE (data communication device) which cannot be plugged into another DCE. However, if a few additional signals are available, one DCE could be used to daisy chain into another DCE as shown in Figure 2. As can be seen the data carrier detect lines are used to key the companion modem unit. The originating end must be programmed with sufficient delay to allow the RTS/CTS delay of the modems to occur prior to the beginning of any information transfer.

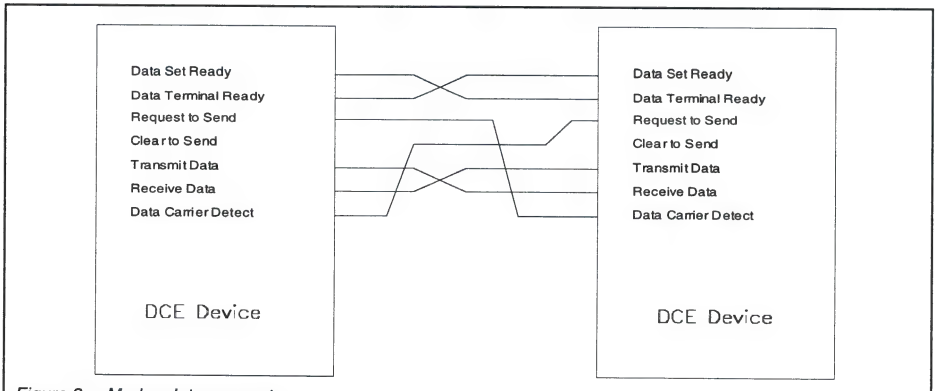


Figure 2 - Modem Interconnect

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830068.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Continuously Variable Slope Delta Modulation: A Tutorial

1. Introduction

Virtually all means of wireless and wireline speech communication are, or are becoming, digital. Digital coding of speech for transmission or storage clearly has advantages over traditional analog methods. In digital data communication or storage systems, information is transmitted or recorded as a series of binary digits—the receiver or player must only distinguish between a one or zero to exactly recover the original information. In digital voice systems the information is the human voice. Digital speech coding algorithms are judged by their ability to quantize (digitize) speech accurately for transmission and then perform the reverse at the decoder. In other words, the original analog speech signal must be accurately recovered at the receiver. Sounds simple, however, without compression quantized speech can require significantly more bandwidth than analog speech. For wireline or wireless telecom applications, the speech extends from 300 Hz to 3300 Hz. If an analog signal in this band is quantized using a linear Analog to Digital Converter (ADC) sampling just above the Nyquist rate, say 8 KHz, with 256 quantization levels (8 bits) the resulting data rate is 64 Kbits per second. Without exotic modulation/coding, the bandwidth (BW) for the digitally encoded signal is nearly twenty times the original analog signal. Such BW consumption is not practical, particularly for wireless applications.

Engineers working in the field of Speech Coding have been actively searching for methods to reduce the bandwidth consumed by quantized speech signals. Early algorithms attempted to take advantage of the human ear's adaptive dynamic range. The human ear has a built in ability to become more or less sensitive to audible signals—the ear can hear sound pressure levels (SPL) as low as 0 dB SPL (threshold of human hearing) to 120 dB SPL (on set of pain) yet at any one time the dynamic range of human hearing is generally considered to be about 40 dB. In other words, we have a difficult time hearing someone whispering at a rock concert. Some speech coding algorithms exploit this phenomena by using a greater number of progressively smaller quantization levels for low amplitude signals and fewer, more coarse quantization levels for large amplitude signals. This is known as non-uniform quantization. Non-uniform quantization is used in the Public Switched Telephone Network (PSTN) where it is called μ-law Pulse Code Modulation (PCM). A slightly more complex approach takes advantage of strong correlation between adjacent speech samples, quantizing the amplitude *difference* (delta) between two samples as opposed to the entire sample amplitude. This *difference* signal requires fewer quantization levels for the same signal quality and consequently, reduces the required bandwidth. Algorithms employing this technique are classified under the broad category of differential quantization or differential PCM (DPCM). Further bandwidth conservation is possible through more complex algorithms. For example, combining adaptive quantization with DPCM results in the commonly used coding algorithm, adaptive DPCM (ADPCM).

Delta modulation (DM) and Continuously Variable Slope Delta modulation (CVSD) are differential waveform quantization techniques. Both employ two level quantizers (one bit). CVSD is basically DM with an adaptive quantizer. Applying adaptive techniques to a DM quantizer allows for continuous step size adjustment. By adjusting the quantization step size, the coder is abled to represent low amplitude signals with greater accuracy (where it is neede) without sacraficing performance on large amplitude signals.

CVSD is used in tactical communications where "communication quality[1]" is required yet the option for security must be available. MIL-STD-188-113 (16 Kb/s and 32 Kb/s), and Federal Standard 1023 (12 Kb/s CVSD) are examples of a tactical communication systems using CVSD. With the tremendous worldwide growth in wireless technology, secure communication is becoming important to everyone. In addition to point-to-point communication, CVSD is commonly used in digital voice recording/messaging and audio delay lines.

This paper attempts to describe CVSD quantization, focusing on its application to coding of speech. Before discussing the details of CVSD, the basics of uniform and non-uniform quantization (non-adaptive) will be reviewed. Next, the subject of differential quantization will be explained, showing that DM and CVSD are equivalent to one bit DPCM and ADPCM, respectively. Finally, some application suggestions for MX•COM CVSD codecs will be presented.

[1] ***Communication quality*** is a qualitative expression widely considered synonymous with "acceptable speech communication." It is not intended to imply "high-fidelity," only that intelligible conversation can take place.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. Waveform Quantization [1, 3, 5, 9]

Waveform quantization is a process of assigning discrete levels to a sampled analog signal. In the context of this paper the signal of interest is speech, although the concepts are applicable to signals in different frequency bands. The term "quantization" implies a relationship between the amplitude of a discrete sample and its numeric value. This relationship may be linear, non-linear, or differential.

2.1 Sampling [5, 9]

Before a signal can be quantized it must first be sampled. Sampling is the act of instantaneously capturing the level of a continuous signal at some predetermined rate. This predetermined rate is called the sampling frequency. As the sampling rate increases, the sampled signal begins to approximate the original continuous signal. As the sampling frequency decreases, samples move further apart in time, eventually the original signal cannot be reconstructed from the sampled version. The limit on how far apart these samples can be, without losing information, is the basis for Shannon's sampling theorem.

Shannon's sampling theorem [5] was originally stated as follows: "If a function $f(t)$ contains no frequencies higher than f cycles per second it is completely determined by giving its ordinates at a series of points spaced $(1/2f)$ seconds apart." A mathematical version of this theorem can be obtained by convolving the Fourier transform of the signal to be sampled with the Fourier transform of an infinite sequence of impulse functions

$$F_S(\omega) = \frac{1}{2\pi}[F(\omega) * S(\omega)] \tag{1}$$

or,

$$F_S(\omega) = \frac{1}{2\pi}\int_{-\infty}^{\infty} S(\tau)F(\tau - \omega)d\omega \tag{2}$$

Where, $F_S(\omega)$ = sampled signal spectrum

$F(\omega)$ = original signal spectrum

$S(\omega)$ = spectrum for a sequence of impulses

$\omega = 2\pi f$ (radian frequency).

The result of the convolution in equation (2) is the original signal spectrum repeated at multiples of the sampling frequency, see Figure 1. Notice that if the sampling frequency is less than twice the bandwidth of the original signal the replicas centered at multiples of the sampling frequency will overlap and distort the original. This undesirable phenomenon is *aliasing*. To avoid aliasing,

$$f_S \geq 2B. \tag{3}$$

Where, f_S = sampling frequency in Hz

B = bandwidth of original signal in Hz.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

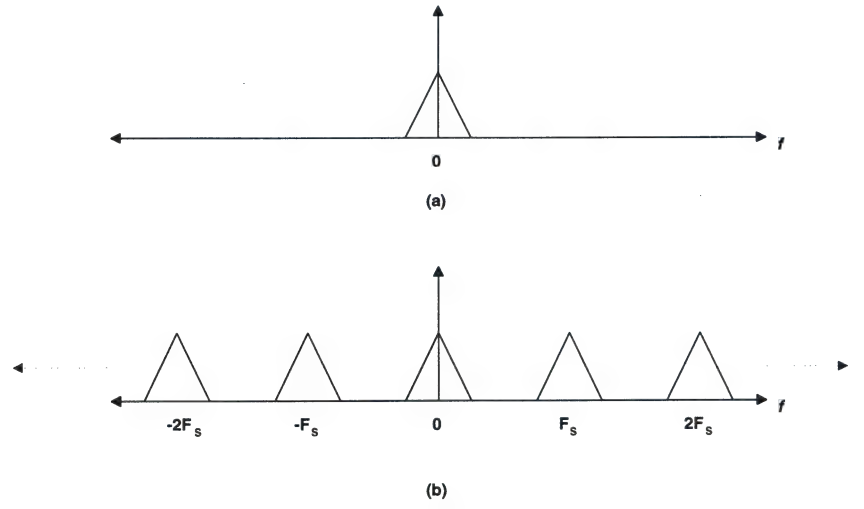


Figure 1: Fourier transform of (a) continuous time signal and (b) sampled signal.

Shannon's sampling theorem is mathematically accurate. Although, in most cases it is not practical to sample a signal at exactly twice it's highest frequency. Band-limiting is necessary to avoid aliasing. For $f_s=2B$ the band-limiting filter must have a so called "brick wall" roll-off at frequency B. A filter that matches this requirement is physically unrealizable. Several factors contribute to the actual sampling frequency used. Generally there is a compromise between the complexity of the band-limiting filter versus the cost of the analog to digital converter (ADC). As f_S becomes closer to $2B$, the band-limiting filter requires more stages to give the desired roll-off. As f_S increases, the required conversion time necessitates a faster ADC. Cost for ADCs is inversely proportional to conversion time, as conversion time decreases, cost rises.

2.2 Uniform Quantization [3, 4, 9]

Figure 2 illustrates the transfer characteristic of a seven level uniform quantizer. To represent the quantized output $q(n)$ as a binary number would require 3 bits. Once a signal has been sampled it is discrete in time. However, the amplitude remains continuous. The quantized version of a signal is obtained by applying the sampled signal to a binary encoder where the discrete voltage levels are assigned to the nearest binary numbers. The complete process, combining sampling and amplitude quantization, is known as PCM.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

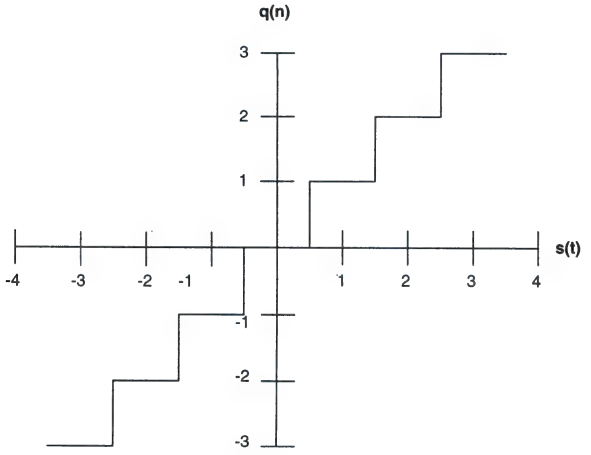


Figure 2: Uniform quantizer transfer characteristic.

The noise introduced by PCM is primarily due to the rounding to the "nearest" binary number. If a signal is quantized to eight levels (3 bits) using a quantizer transfer characteristic similar to the one shown in Figure 2, the finest resolution is the full scale magnitude divided by eight. In general,

$$\frac{A}{2^n} = \alpha . \tag{4}$$

Where, A = full scale amplitude

n = number of bits per sample

α = difference between quantization levels (i.e. finest resolution).

The uncertainty error due to rounding is based on the assumption that there is a continuous range of values within α, all of which are equally likely to have been the actual value of the original signal (uniform distribution). The error signal ε is the difference between the original signal amplitude and the quantized sample value. As a result, the mean square uncertainty error can be solved for by finding the expected value of error squared over the range of $-\alpha/2$ to $\alpha/2$

$$E(\varepsilon^2) = \frac{1}{\alpha}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \varepsilon^2 d\varepsilon . \tag{5}$$

Where, E = expected value operator

ε = difference between actual and quantized signal levels.

Performing the integration in equation (5) yields an expression which is equivalent to quantization noise power

$$N_{OUT}^2 = \frac{\alpha^2}{12}. \tag{6}.$$

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20830070.001

Taking the square root of both sides gives the root mean square (RMS) noise voltage

$$N_{OUT} = \frac{\alpha}{2\sqrt{3}}. \quad (7)$$

The maximum signal-to-noise ratio (SNR) for a uniformly quantized signal can be calculated by finding the ratio of the full scale quantization level to the noise voltage in equation (7). The full scale quantization level is simply the total number of quantization levels multiplied by the minimum quantization increment α

$$S_{OUT_{MAX}} = \frac{\alpha(2^n)}{2}. \quad (8)$$

Where, n = number of bits in quantizer.

The ratio of equations (7) and (8) yields the SNR

$$SNR = \frac{2^n}{\sqrt{3}}. \quad (9)$$

In dB,

$$SNR_{dB} = 4.77 + 6.02n. \quad (10)$$

Equation (10) is an objective measure of quality in systems employing uniform quantization. It should be noted: the SNR calculated in equation (10) is a theoretical maximum. In practice other factors (e.g. power supply noise) tend to reduce the final SNR. Also, the human voice is considered to have about 40 dB of dynamic range, however, during most conversations it is typically about 20 dB down from maximum. In other words, we generally do not shout during normal conversation. Consequently, the average signal to noise ratio for uniformly quantized speech is about 20 dB less than what would be calculated using equation (10).

Another objective measure of quality which can be derived in a similar manner is dynamic range. Dynamic range pertains to the resolution of a quantization scheme. It is the ratio of the full scale amplitude to the smallest quantized amplitude change,

$$DR = \frac{1}{2}\left(\frac{\alpha 2^n}{\alpha}\right) = 2^{n-1}. \quad (11)$$

In dB,

$$DR_{dB} = 6.02(n-1). \quad (12)$$

2.3 Non-uniform Quantization [1, 7, 9]

To this point the discussion has been based strictly on uniform quantization (linear speech coding). That is, waveforms are quantized such that all signal levels have the same resolution. An alternative to linear quantization is to make α fine for low level signals and coarse for high level signals, introducing a non-uniform quantizer characteristic. This type of quantization can result in improved dynamic range for a given number of bits and effectively raise the SNR for lower level signals. The drawback is lower maximum SNR—equations 9 and 10 are not valid for non-uniform quantization. Figure 3 shows a transfer characteristic for a seven level non-uniform quantizer. Notice, when compared to the uniform quantizer transfer characteristic shown in Figure 2, there are three quantization levels for the input $s(t)$ between zero and one, where there is only one with the uniform quantizer.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

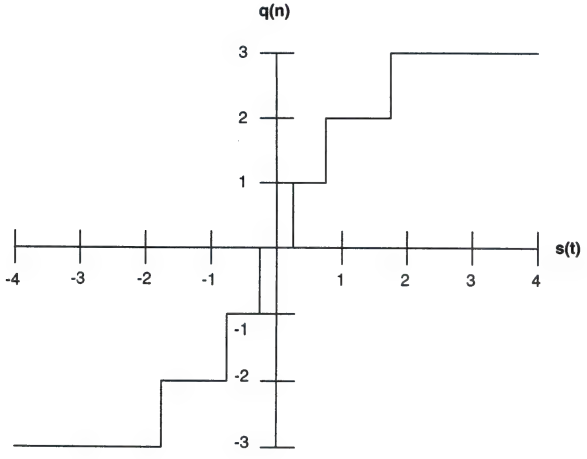


Figure 3: Non-uniform quantizer transfer characteristic.

A complete digital communication system, incorporating non-uniform speech coding, compresses the quantized signal at the transmitter then expands the signal back to linear form at the receiver. The compressed signal requires fewer bits and therefore consumes less BW. Ideally, the expander transfer function is the exact inverse of the compressor and is able to reproduce the original uncoded analog signal. In literature pertaining to telecommunications, the words *compressor* and *expander* are generally combined in to a single word; *compandor.*

Companding is on of the most popular forms of non-uniform quantization. When compared to uniform quantization, it allows for bandwidth compression without degradation in dynamic range, at the expense of peak signal to noise ratio. For example, a signal uniformly quantized to 14 bits, using equations (10) and (12), would have a peak SNR and DR of approximately 89 dB and 78 dB respectively. If the same signal is non-uniformly quantized (compressed) using only 8 bits (256 levels), the minimum quantization level can be set such that DR of 78 dB can be retained, although the peak SNR will be degraded. Degradation in the peak SNR is due to the course quantization levels used for the large amplitude signals (where fine quantization is not necessary). Low amplitude signals are quantized at finer resolution (more steps, where it is necessary). Consequently, the SNR at low signal levels is improved when compared to uniform quantization with the same number of levels. Essentially, companding strives to make SNR constant over the dynamic range of the quantizer.

2.3.1 μ-Law Companding [1, 9]

Most forms of non-uniform quantization are derived from a logarithmic transfer function. That is, the output signal is proportional to the log of the input signal. In North America and Japan, digital telecommunications networks employ μ-law companding as the standard for PCM encoding (μ=255 for North America). The general form of the transfer characteristic is

$$y(x) = sign(x)\frac{\ln(1+\mu|x|)}{\ln(1+\mu)}. \qquad (13)$$

Where, $-1 \le x \le 1$

x = input signal

$y(x)$ = compressed output signal

$sign(x)$ = polarity of input signal.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2.3.2 Uniform versus Non-uniform Quantization [7]

An accepted method of objectively measuring quality in signal processing systems is SNR. In the context of digital coding this would more accurately be called: signal to quantization noise ratio (SQR). Equation (10) was derived to calculate the SNR for uniform quantization assuming maximum input signal. To find SNR for input signal amplitudes less than maximum equation (10) must be rewritten

$$SNR_{dB} = 4.77 + 6.02n + 20\log\left(\frac{S_i}{S_{MAX}}\right). \tag{14}$$

Where, S_i = input signal level

S_{MAX} = maximum signal level.

When the quantization characteristic is not uniform (14) is no longer valid. To clarify the performance of companded quantization, the SNR must be calculated for a full range of input signal levels. For μ-law companding the signal to noise ratio is given by the following equation [9],

$$SNR_{\mu(dB)} = 10\log\left[\frac{3(2^{2n})}{[\ln(1+\mu)]^2\left[1+\frac{1.732}{\mu S_i}+\frac{1}{\mu^2 S_i^2}\right]}\right]. \tag{15}$$

It should be noted that as $\mu \rightarrow 0$, equation (15) is equivalent to equation (14), thus $\mu = 0$ implies uniform quantization. Figure 4 compares SNR versus relative input signal power for 256 level non-uniform quantization (μ = 255) and 256 level uniform quantization.

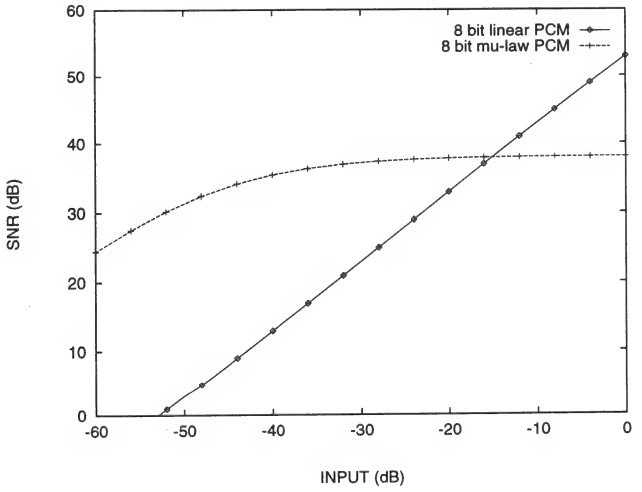


Figure 4: SNR versus input level for 8 bit μ-law and 8 bit uniform quantization.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2.4 Differential Quantization [4, 8]

Differential quantization is a coding technique where the difference between the present sample and the predicted value for the next sample is quantized. This type of quantization is advantageous because the difference signal dynamic range (variance) is less than the unprocessed input signal. Consequently, fewer quantization levels are required to retain the same Signal-to-Noise Ratio (SNR). Alternatively, the number of quantization levels can remain the same allowing the difference signal to be encoded using all the available bandwidth resulting in greater resolution and improved signal quality.

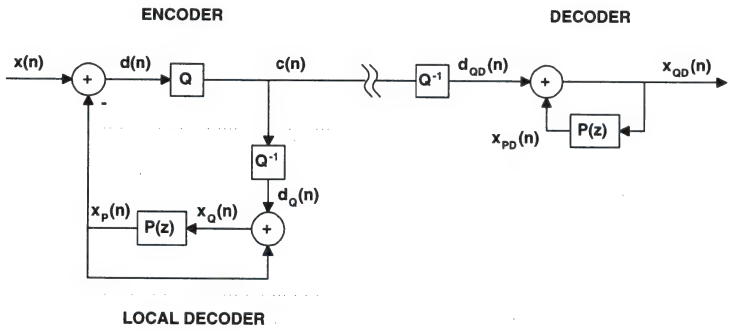


Figure 5: Differential quantization block diagram.

Figure 5 is a block diagram displaying a differential quantization system. All signals are represented in discrete time notation implying that $x(n)$ is the discrete time version of $x(t)$. Notice the decoder is in the feedback path of the encoder. Thus, the decoder is performing the inverse of the encoder. The block labeled **Q** converts the difference signal $d(n)$ in to a binary representation suitable for transmission and the block labeled $\mathbf{Q}^{-1}$ does the inverse. In reality, the process of converting $d(n)$ to $c(n)$ and back to $d_{QD}(n)$ is a significant factor in the non-ideal behavior of differential quantization. Nevertheless, fundamental analysis of the system is simplified by assuming blocks **Q** and $\mathbf{Q}^{-1}$ cancel. Employing this assumption, the transfer function of the encoder in z-domain terms

$$H_{ENC}(z) = \frac{C(z)}{X(z)} = Q(z)[1 - P(z)]\,. \tag{16}$$

And the decoder transfer function is

$$H_{DEC}(z) = \frac{X_{QD}(z)}{C(z)} = \frac{1}{Q(z)[1 - P(z)]}\,. \tag{17}$$

If $D_{QD}(z) \equiv D(z)$, then $X_{QD}(z) \equiv X(z)$ and the entire system transfer function can be written as,

$$H(z) = H_{ENC}(z)H_{DEC}(z) = 1\,. \tag{18}$$

Although equation (18) is based on several assumptions, it shows a differential quantization system patterned after the topology displayed in Figure 5 can be made to produce an output signal which approximates the original input signal. The quality of the approximation is what distinguishes various differential quantization schemes. Generally, high quality approximation does not come without a price.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

A crucial element in differential quantization is the predictor $P(z)$. The output $x_P(n)$ of $P(z)$ is a weighted sum of past input samples. The general form is equivalent to a finite impulse response (FIR) filter

$$x_P(n) = \sum_{k=1}^{P} a_k x_Q(n-k). \tag{19}$$

Where, P = order of predictor

a_k = weighting factor (coefficient)

$x_P(n)$ = output of predictor

$x_Q(n) = d_Q(n) + x_P(n)$ (input to predictor).

Applying the z-transform to equation (19) yields the transfer function for the predictor

$$P(z) = \frac{X_P(z)}{X_Q(z)} = \sum_{k=0}^{P} a_k z^{-k}. \tag{20}$$

Equations (19) and (20) show that the predictor output is a linear combination of past inputs giving rise to the term "linear prediction." Non-linear predictors (non-linear combination of past input samples) have been studied, however, due to complexity and stability issues, their popularity is limited.

The coefficients a_k are calculated such that $P(z)$ will provide a reasonably accurate model for the behavior of human speech. In 1966 a paper was published by McDonald [6] suggesting coefficients, based on normalized autocorrelation of human speech samples, for predictors of order one to ten. Later, in 1972, Noll [4] published similar data. These two papers are generally referenced in determination of predictor coefficients. Assuming that $P(z)$ does provide a reasonably accurate model for human speech, $x_Q(n) \cong x(n)$ and $d(n) \rightarrow 0$. In other words, a good predictor should minimize the difference signal $d(n)$. This is the basis for differential quantization. In most DM algorithms the predictor order P is set to one.

The potential for instability in differential quantizers exists in the encoder. As mentioned early, equation (20) is the transfer function of an FIR filter. One of the significant characteristics of FIR filters is, by definition, they are stable (the transfer function has only zeros). However, when an FIR is placed in a feedback path, as is the case with the encoder, the zeros become poles—if one of these poles finds its way outside the unit circle the differential quantizer will be unstable.

3. Delta Modulation [1, 4, 6, 8, 10]

DM is a differential quantization scheme that uses two level quantization (i.e. one bit quantizer). By using a single bit to represent each sample, the sample rate and the bit rate are equivalent. Consequently, sample rate is directly related to signal quality (SNR). Also, BW of the input signal and band-limiting of the output are significant factors in determining signal quality.

The first DM algorithm was conceived in 1946. During the last 50 years, two algorithms; Linear DM (LDM) and CVSD, received a significant amount of attention from those interested in efficient methods to digitize speech. LDM is the most fundamental, least complex form of DM. Hence, this tutorial will attempt to provide an understanding of LDM as a foundation for understanding more complex DM algorithms. The CVSD algorithm, an accepted standard in the tactical community and finding a growing number of applications in "point-to-point" wireless applications, will also be covered.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.1 Linear DM [1, 4, 6, 8]

The predictor $P(z)$ in LDM is first order and the quantizer **Q** is two level. Figure 6 is a flow diagram describing the LDM encoder and decoder algorithms.

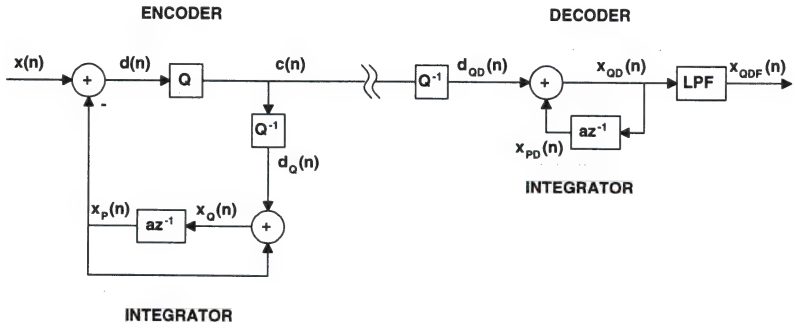


Figure 6: LDM block diagram.

The predictor is shown as a single tap FIR filter with transfer function $P(z) = az^{-1}$. In the encoder, the transfer function between $d_Q(n)$ and $x_P(n)$ can be expressed in the z-domain terms as

$$\frac{X_P(z)}{D_Q(z)} = \frac{az^{-1}}{1 - az^{-1}} \tag{21}$$

In the decoder, the transfer function between $d_{QD}(n)$ and $x_{QD}(n)$ is

$$\frac{X_{QD}(z)}{D_{QD}(z)} = \frac{1}{1 - az^{-1}} \tag{22}$$

Equations (21) and (22) represent discrete time integrators (if $a = 1$). If $a < 1$ they become damped or lossy integrators. McDonald [6] and Noll [4] both suggest $a = 1$ for optimum prediction gain. A pure integrator ($a = 1$) will cause bit errors to propagate longer than if $a < 1$. In practice, a value of $a < 1$ is preferred.

The quantizer **Q** in figure 6 functions like a comparator. When the input $d(n)$ exceeds zero it outputs a logic one, when the input is less then zero the output is a logic zero. Hence, the output of **Q** is a single bit indicating the sign of the magnitude of $d(n)$. The inverse quantizer $\mathbf{Q}^{-1}$ converts logic levels to delta $d_Q(n)$ as shown in the table below.

sign of $d(n)$	$c(n)$	$d_Q(n)$
-	0	$-\Delta$
+	1	Δ

Table 1: Sign of $d(n)$ with corresponding logic levels and deltas.

The value of Δ plays an important role in the performance of LDM. If Δ is relatively small, tracking of slowly changing, low amplitude signals is quite good at the expense of poor tracking for fast, abruptly changing signals. When DM is not able to keep up with the input signal a phenomena called *slope overload* is exhibited, as shown in Figure 7.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

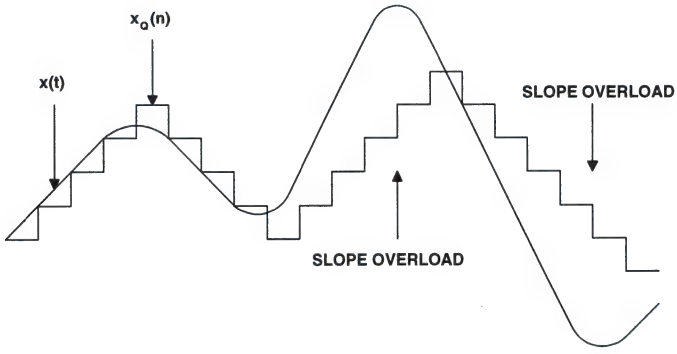


Figure 7: Slope overload in LDM.

Increasing the value of Δ can lessen the effects of slope overload but creates a new problem; *granular noise*. With Δ to large, low amplitude signals will not be quantized at fine enough levels and they appear as *idle channel noise* , see Figure 8. The idle channel pattern is simply an alternating one-zero sequence indicating the input signal amplitude is not changing. Since an alternating one-zero bit pattern has a mean value of zero, the signal out of the decoder will integrate to zero.

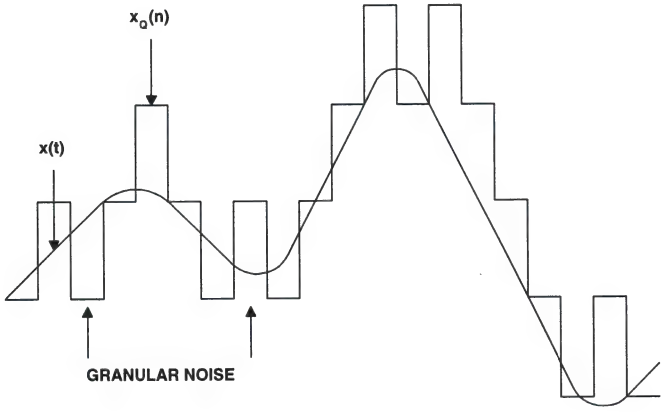


Figure 8: Granular noise in LDM.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.2 CVSD [2, 4, 10]

Issues with granularity and slope overload can be drastically reduced by making dynamic adjustments to the quantizer step size Δ. Adaptive DM (ADM) algorithms attempt to do this by making Δ small for slowly changing signals and large for rapidly changing signals. The most publicized ADM algorithm is known as CVSD. It was first proposed by Greefkes and Riemens in 1970 [2]. In their CVSD algorithm, adaptive changes in Δ are based on the past three or four sample outputs (i.e. $c(n)$, $c(n-1)$, $c(n-2)$, $c(n-3)$). Figure 9 and Figure 10 show flow diagrams of the algorithms for the encoder and decoder respectively. Notice only the last three samples of $c(n)$ are used here.

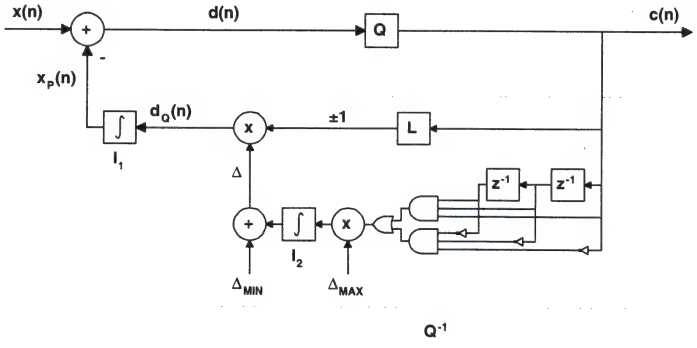


Figure 9: CVSD encoder block diagram.

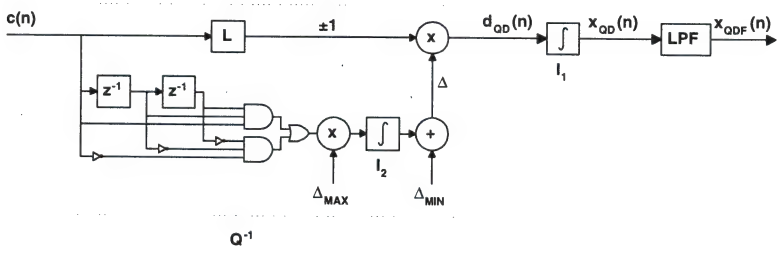


Figure 10: CVSD decoder block diagram.

The block labeled $\mathbf{Q^{-1}}$, previously shown in Figure 6, has been replaced by two cascaded one sample delays (z^{-1}) and logic to determine when three consecutive ones or zeros have occurred. The minimum and maximum step height is set by Δ_{MIN} and Δ_{MAX}, respectively. When strings of three consecutive zeros or ones have not occurred for a period of time long enough for the output of the integrator $\mathbf{I_2}$ to decay to near zero, the algorithm is equivalent to LDM (section 3.1). The time constants for the integrator $\mathbf{I_2}$ and integrator $\mathbf{I_1}$ are typically 4 ms and 1 ms respectively. In CVSD literature integrator $\mathbf{I_1}$ is referred to as the *principle integrator* and integrator $\mathbf{I_2}$ as the *syllabic integrator*. The so called *syllabic integrator* derives its name from the length of syllable. Actually a syllable is about 100 ms in duration, however, pitch changes are on the order of 10 ms. Consequently, 4 ms seems to work best for the CVSD *syllabic* (*pitch*) time constant. The block labeled **L** performs simple level conversion (i.e. $c(n) = 1$, **L** outputs 1; $c(n) = 0$, **L** outputs -1). This CVSD algorithm is also known as "Digitally Controlled DM" [10].

Figure 11 displays the output of the integrator $\mathbf{I_1}$ ($x_P(n)$ in the encoder and $x_{PD}(n)$ in the decoder). When compared to Figure 7 and Figure 8 slope overload and granular noise are reduced.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

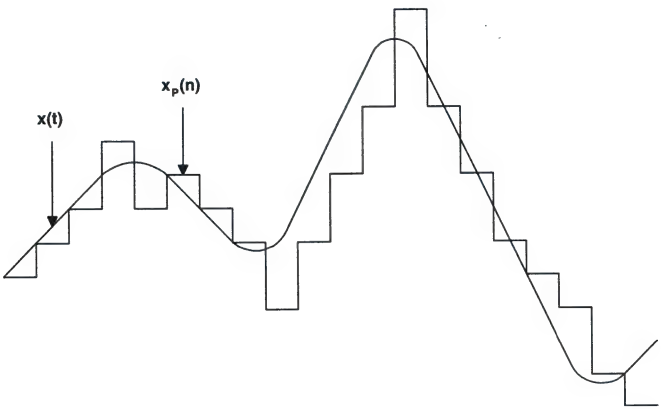


Figure 11: CVSD quantization noise.

3.3 Performance Measurement of DM [1,4]

The maximum SNR for DM speech coders is [1]

$$SNR_{dB} = 10\log\left(\frac{f_S^3}{f_{BW} f^2}\right) - 14.0\,. \tag{23}$$

Where, f_S = data rate (sample rate)

f_{BW} = signal BW (cutoff frequency of LPF)

f = signal frequency.

Most literature on DM coding agrees on the terms involving f_S, f_{BW}, and f in equation (23) but most do not agree on -14 dB. This term varies from -17.0 dB to -11.7 dB depending on a variety of different input signals and assumptions about environment. Nevertheless, equation (23) is considered a maximum because it assumes no slope overload and minimum granular noise, i.e. optimum step size.

The adaptive behavior of CVSD results in a SNR versus input level characteristic similar to non-uniform quantization (mentioned in section 2.3). This non-linear SNR characteristic is due to *companding*, where the quantization level (slope) is adjusted to a larger or smaller value according to past pitch changes of the input signal. The number of past samples (bits) used to make a prediction is normally three or four. Four bit *companding* has proven to be most effective for data rates greater than 32 Kb/s, three bit *companding* seems to work better for data rates less than 32 Kb/s.

Figure 12 shows a typical SNR versus input level characteristic for 32 Kb/s CVSD (four bit *companding* algorithm, input signal = 820 Hz sinewave). Equation (23) predicts a maximum SNR of 27.6 dB which is nearly met in Figure 12 for and input signal level of -15 dbm0 (0 dBm0 = 489 mVrms). Above and below the -15 dBm0 input level granular and slope overload noise start cause distortion. Finally, It should be noted that CVSD does not perform well with continuous tone or data input signals, particularly at data rates below 32 Kb/s.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

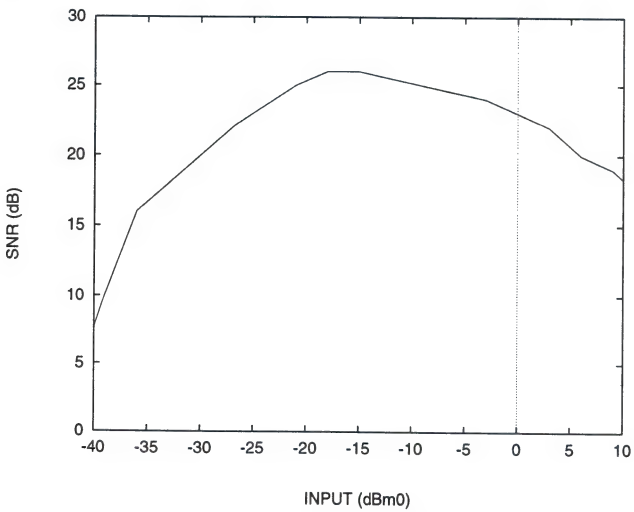


Figure 12: Measured SNR versus input level for 32 Kb/s CVSD (input = 820 Hz sinewave).

SNR is the most used method to objectively quantify performance of speech coding algorithms. However, it does not always correspond with perceived quality, particularly for differential and adaptive algorithms using actual voice as the input. In addition, it is difficult to make reliable SNR measurements in the presence of random bit errors. In an effort to quantify the perceived quality of a speech coding algorithm, *Mean Opinion Score* (MOS) testing was developed [4]. Table 2 summarizes the five point scale used to judge quality and impairment.

Number	Quality	Impairment
5	excellent	imperceptible
4	good	perceptible but not annoying
3	fair	slightly annoying
2	poor	annoying
1	bad	very annoying

Table 2: Mean Opinion Score testing guidelines.

An MOS rating of 4 to 4.5 is considered *Toll Quality* (equivalent to commercial telephony). Where as *Communication Quality* MOS ratings are 3 to 4 (barely perceptible distortion, but no degradation in intelligibility).

Figure 13 compares MOS ratings for μ-law PCM (the standard for *Toll Quality*), CVSD and ADPCM. Notice CVSD performs as well or better than both μ-law PCM and ADPCM in the presence of bit errors. Specifically, CVSD retains quite good MOS ratings at bit error rates exceeding 1%, and at 10% has an MOS rating of 3 (*Communication Quality*). It is this robustness to bit errors (channel noise) that makes CVSD an ideal solution for many wireless speech communication applications.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

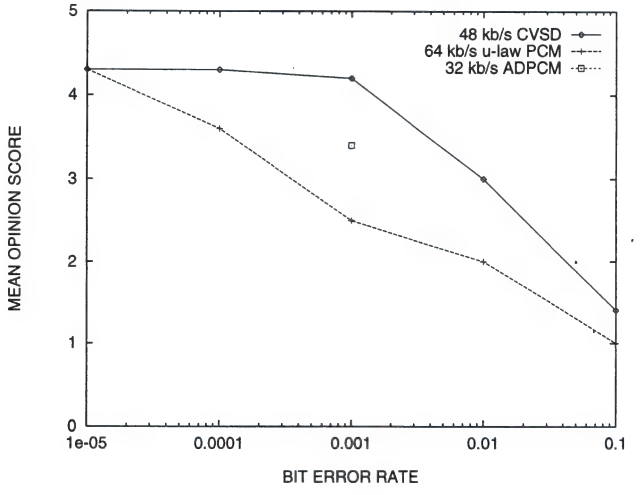


Figure 13: MOS versus bit error rate for ADPCM, μ-law PCM, and CVSD from [4].

4. Summary

CVSD has several attributes that make it well suited for digital coding of speech. One bit words eliminate the need for complex framing schemes. Robust performance in the presence of bit errors make error detection and correction hardware unecessary. Other speech coding schemes may require a digital signal processing engine and external analog to digital/digital to analog converters to convert the analog signal in to a form that can be processed digitally—the entire CVSD codec algorithm, including input and output filters, can be integrated on a single silicon substrate. Despite this simplicity, CVSD has enough flexibility to allow digital encryption for secure applications. Finally, CVSD can operate over a wide range of data rates—it has been successfully used from 9.6 kB/s to 64Kb/s. At 9.6Kb/s audio quality is not particularly good, however, it is intelligible. At data rates of 24 Kb/s to 48 Kb/s it is judged as quite acceptable. And above 48 Kb/s it is comparable to *toll quality*. All of these attributes make CVSD attractive to wireless telecommunication systems (e.g. digital cordless telephones, digital Land Mobile Radio). The defence industry has been using CVSD for decades in wireline and wireless systems as specified in Mil-Std-188-113. More recently, Federal Standard 1023 proposed CVSD for 25 Khz channel radios operating above 30 Mhz. Figure 14 is a block diagram showing a CVSD Codec (MX109) in a digital mobile radio system.

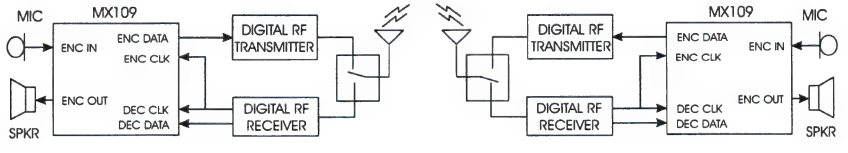


Figure 14: Digital wireless system incorporating MX•COM MX109 CVSD Codec.

This tutorial has attempted to shed some light on the fundamental aspects of CVSD. It has shown that CVSD is a differential adaptive quantization algorithm with one bit coding and first order prediction (one bit ADPCM). In addition, objective and subjective methods of measuring signal quality showing that CVSD performs quite well in the presence of bit errors (noisy channel) have been presented.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

5. References

[1]J. C. Bellamy, Digital Telephony, Wiley and Sons, New York, 1982.

[2] J. A. Greefkes and K. Riemens, "Code Modulation with Digitally Controlled Companding for Speech Transmission," Philips Tech. Rev., pp. 335-353, 1970.

[3] A. Gersho, "Principals of Quantization," IEEE Transactions on Circuits and Systems, pp. 427-436, July 1978.

[4] N. S. Jayant and P. Noll, Digital Coding of Waveforms: Principles and Applications to Speech and Video, Prentice-Hall, Englewood Cliffs, N. J., 1984.

[5] A. B. Jerri, "The Shannon Sampling Theorem—Its Various Extensions and applications: A Tutorial Review,"Proceedings of the IEEE, pp. 1565-1596, November 1977.

[6] R. A. McDonald, "Signal-to-Noise and Idle Channel Performance of Differential Pulse Code Modulation Systems-Particular Applications to Voice Signals," Bell System Technical Journal, pp. 1123-1155, Sept. 1966.

[7] P. Noll, "A Comparative Study of Various Quantization Schemes for Speech Encoding," Bell System Technical Journal, pp. 1597-1614, November 1975.

[8] L. R. Rabiner and R. W. Schafer, Digital Processing of Speech Signals, Prentice-Hall, Englewood Cliffs, N. J., 1978.

[9] M. Schwartz, Information, Transmission, Modulation, and Noise, McGraw Hill, New York, 1980.

[10] R. Steele, Delta Modulation Systems, Pentech Press, London, England, 1975.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830070.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

DATA BULLETIN

MX609

An Audio Delay circuit based on the MX609 CVSD Codec

1. Introduction

The schematic diagram shown on the following page is an audio delay circuit based on the MX609 CVSD Codec. In addition to the MX609, the circuit uses a Motorola MCM6287 64K x 1 bit RAM, two 4520 counter ICs, and a 4069 inverter chip. It provides up to two seconds of delay. This circuit provides a starting point for a designer who wishes to implement an audio delay circuit. MX-COM makes no guarantee of its performance and assumes no responsibility for its use in any product.

2. Circuit Operation

In the following operational description, a bar over a signal name is used to indicate an active low signal. For example, W is an active low write enable signal. On the MX609P, Clock Mode 1, pin 22, is tied to VDD and Clock Mode 2, pin 21, is tied to ground to set the encode and decoder clocks for a sampling rate of 32 kb/s. The Encoder Force Idle, Powersave, and Decoder Force Idle inputs, pins 6, 15, and 16, respectively, are tied to VDD to set them inactive. The Data Enable input, pin 7, is tied to VDD to make the encoded data available at the Encoder Output, pin 5. Pin 19, the Algorithm select input, is tied to ground to select a four-bit companding algorithm. The other inputs are the same as recommended for "External Component Connections" shown in the MX-COM data book.

The audio signal to be delayed is input to pin 10 of the MX609, the Encoder Input, and is converted to a serial stream of digital data. The serial data are output on pin 5, the Encoder Output, and connected to pin 13, the D input, of the MCM6287 memory chip. The Decoder Data Clock output from pin 18 of the MX609 is connected to pin 1 of the 4069 inverter. The output of the inverter, pin 2, is connected to pin 10 of the MCM6287, the W input, and to pin 3 of the 4069, the input to second inverter. Pin 4, the inverter output, is connected to the enable input of the first 4520 counter.

The enable input is taken from the second inverter to ensure that the 4520 counters increment after the W signal into the 81C71 transitions from low to high. The clock inputs of each of the 4520s, pins 1 and 9, are tied to ground so that only the enable inputs control when the counters increment. The reset inputs, pins 7 and 15, are also tied to ground so that they never reset the counters. The individual four bit counters in the 4520s are cascaded to produce a 16 bit counter. The counter outputs, Q15 - Q0, are connected to the address inputs, A15 - A0, of the MCM6287.

There are switches between Q15 and A15 and between Q14 and A14. The switches allow the number of bits of the counter, and therefore the length of the delay, to be adjusted. When the Decoder Data Clock falls from high to low, the counter, and therefore the address, increments. Since the W input to the memory, pin 17, is the complement of the clock, it rises from low to high, latching the encoded data bit at the D input. The E input to the MCM6287, pin 12, is tied to ground so that the memory is always selected. When W is high and the address is stable, a valid data bit appears at the Q output, pin 17, of the MCM6287. The address of the data bit appearing at Q is one greater than the address of the bit that was just written, so the counter must cycle through its entire range before a data bit that has been written into the memory can be read. Therefore, a data bit output from the MX609 at the Encoder Output pin is delayed by the number of clock periods of the range of the counter. The delay is given by:

$$\text{Delay} = (\text{T sec/cycle}) * (2\text{N cycles})$$

Where: T = period of Decoder Data Clock
N = number of bits used in counter

If all 16 bits of the counter are used, and the decoder clock frequency is 32 kHz, then the delay would be:

Delay: = (1/32000) sec/cycle * (216) cycles
= 2.048 seconds

In this example, all locations of the memory are used. If a shorter delay is desired, the switches connecting the counter outputs and address inputs can be opened. If only 14 bits of the counter are used, then the delay is reduced by a factor of four, to 0.512 seconds. The range of delays could be increased even more by adding more switches and by making the sampling clock frequency adjustable. The Q output, pin 9, of the MCM6287 is connected to the Decoder Input, pin 17, of the MX609. The decoder clocks in the serial digital data stream from the memory and converts it to an analog signal which is output at pin 13, the Decoder Output. The Decoder Output is the delayed audio signal.

© 1997 MX•COM, Inc.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20830064.001

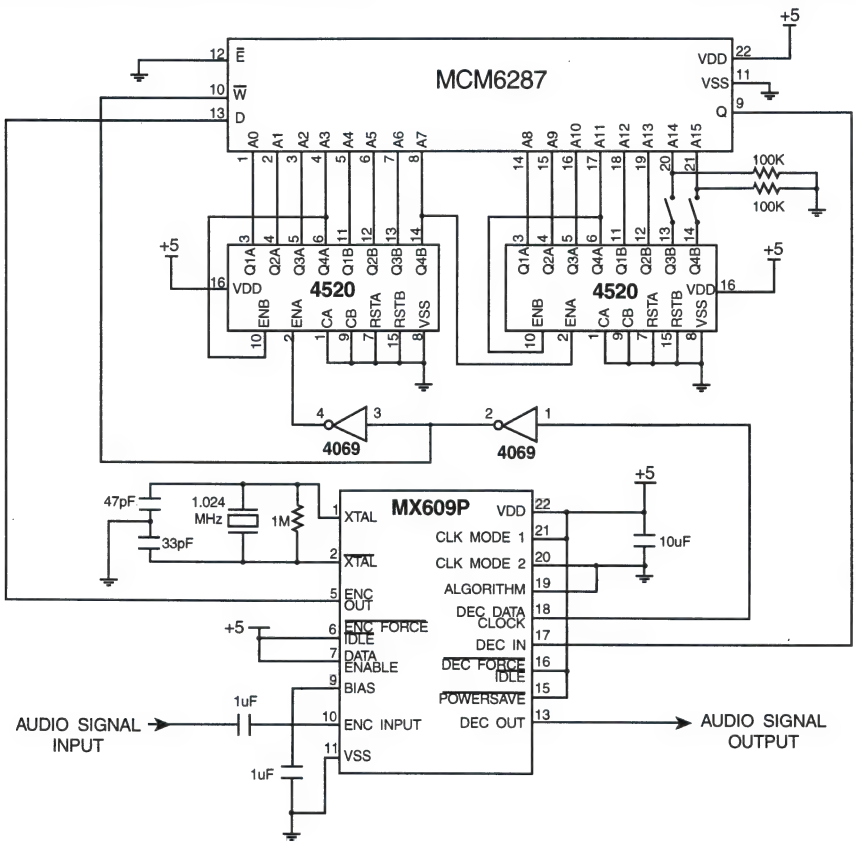


Figure 1: Audio Delay Circuit

© 1997 MX•COM, Inc.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20830064.001

Crystal Oscillator Circuit Design

In this application note we shall discuss our recommended crystal oscillator circuit, explain each component in the circuit and provide some guidelines on selecting values for these components. Finally, we shall give a few precautions to take in order to avoid in-stability and start-up problems.

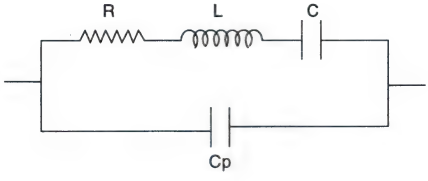


Figure 1. Crystal equivalent Circuit.

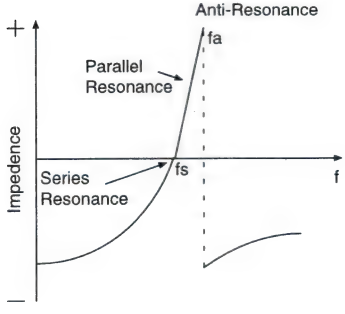


Figure 2. Reactance Vs Frequency plot of a crystal.

Figure 1. shows the crystal equivalent circuit. R is the effective series resistance, L and C are the motional inductance and capacitance of the crystal. C_P is the shunt capacitance due to the crystal electrodes. Figure 2. shows the reactance-frequency plot of the crystal. When a crystal is operating at series resonance it looks purely resistive and the reactances of the inductor and the capacitor are equal (XL = XC). The series resonance frequency is given by the equation

$$fs = \frac{1}{2\pi\sqrt{LC}}$$

When the crystal is operating in parallel resonant mode it looks inductive. The frequency of operation in this mode is defined by the load on the crystal. The crystal manufacturer should specify the load capacitance C_L for parallel resonant crystals. In this mode the frequency of oscillation is given by the equation.

$$f_a = \frac{1}{2\pi\sqrt{L\dfrac{C_L C_P}{C_L + C_P}}}$$

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830065.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

In parallel resonance mode the crystal can be made to oscillate anywhere on the f_s - f_a slope of the reactance plot, shown in Figure 2, by varying the load of the crystal. All of MX-COM's crystal oscillator circuits recommend using parallel resonant mode crystals.

Figure 3. shows the recommended Crystal oscillator circuit diagram. In this type of setup the crystal is expected to oscillate in parallel resonant mode. The inverter which is internal to the chip acts as class AB amplifier and provides approximately 180° phase shift from input to the output and the π network formed by the crystal, R_1, C_1 and C_2 provides additional 180° phase shift. So the total phase shift around the loop is 360°. This satisfies one of the conditions required to sustain oscillation. The other condition, for proper startup and sustaining oscillation is the closed loop gain should be ≥1.

The resistor R_f around the inverter provides negative feedback and sets the bias point of the inverter near mid-supply operating the inverter in the high gain linear region. The value of this resistor is high, usually in the range of a 500KΩ ~ 2MΩ. Some of MXCOM's ICs have this resistor internal, refer to the external component specifications in the data sheet of a particular chip.

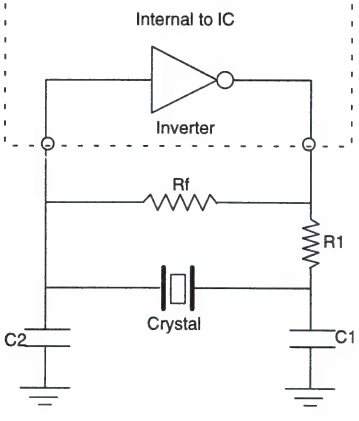


Figure 3. Crystal oscillator circuit.

The capacitors C_1 and C_2 form the load capacitance for the crystal. The optimum load capacitance (C_L) for a given crystal is specified by the crystal manufacturer. The equation to calculate the values of C1 and C2 is

$$C_L = \frac{C_1 * C_2}{C_1 + C_2} + C_S$$

Where C_S is the stray capacitance on the printed circuit board, typically a value of 5pf can be used for calculation purposes. Now C_1 and C_2 can be selected to satisfy the above equation. Usually C_1 and C_2 are selected such that they are approximately equal. Large values of C_1 and/or C_2 increases frequency stability but decreases loop gain and may cause start-up problems.

R_1 is the drive limiting resistor, the primary function of this resistor is to limit the output of the inverter so that the crystal is not over driven. R_1 and C_1 form a voltage dividing circuit, the values of these components are chosen in such a way that the output of the inverter goes close to rail-to-rail and the input to the crystal is 60% of rail-to-rail, usual practice is to make resistance of R_1 and reactance of C_1 equal at the operating frequency, i.e. $R_1 \approx XC_1$. This makes the input to the crystal half that of the inverter output. Always make sure that the power dissipated by the crystal is with-in the crystal manufacturer's specifications. Over-driving the crystal may damage the crystal. Please refer to the crystal manufacturer's recommendations.

Ideally the inverter provides 180° phase shift, but the inherent delay of the inverter provides additional phase shift proportional to the delay. In order to ensure the total phase shift of n360° around the loop, the π network should provide 180° less the phase shift due to the inverter delay. R1 can be varied to accomplish this. With fixed C_1 and C_2, the closed

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830065.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

loop gain and phase can be altered by varying R_1. In some applications R_1 can be ignored if the above two conditions are met.

Some ICs have all the external components (R_f, R_1, C_1, and C_2) internal to the chip, thus eliminating worries to the circuit designer. In this case simply connect the crystal across the XTAL and XTAL pins.

Hints:

Select a crystal with low effective series resistance (ESR), which helps with crystal start-up problems. Lower ESR increases the loop gain.

Reduce the stray capacitance on the board layout by shortening the traces. This would help with startup problem and as well as the frequency of oscillation.

Always test the circuit in applicable temperature and voltage ranges to ensure the crystal starts and sustains oscillations and tweak the component values if necessary.

For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of Vdd, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain further crystal oscillator design assistance, consult your crystal manufacturer.

The recommended way to optimize R_1 is first calculate C_1 and C_2 as explained earlier and connect a potentiometer in place of R_1, set its initial setting at approximately equal to XC_1, then vary the potentiometer setting if required until the crystal starts under all conditions and sustains oscillation under steady state condition.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830065.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

Tone Generation - An Application of the MX105A

This Application Note describes how to configure an MX105A as a tone generator. It may be helpful to refer to the current MX105A data sheet before reading this document. The MX105A was primarily designed as a tone detector with user configurable center frequency, detection band width and response/de-response time (refer to the MX105A data sheet for this use). However, it can also be configured as a low distortion sinusoidal tone generator with minimal filtering. Figure 1 depicts a recommended circuit configuration for tone generation. Figure 2 details the circuit of Figure 1 by showing a block diagram of the active circuits in the MX105A used for tone generation.

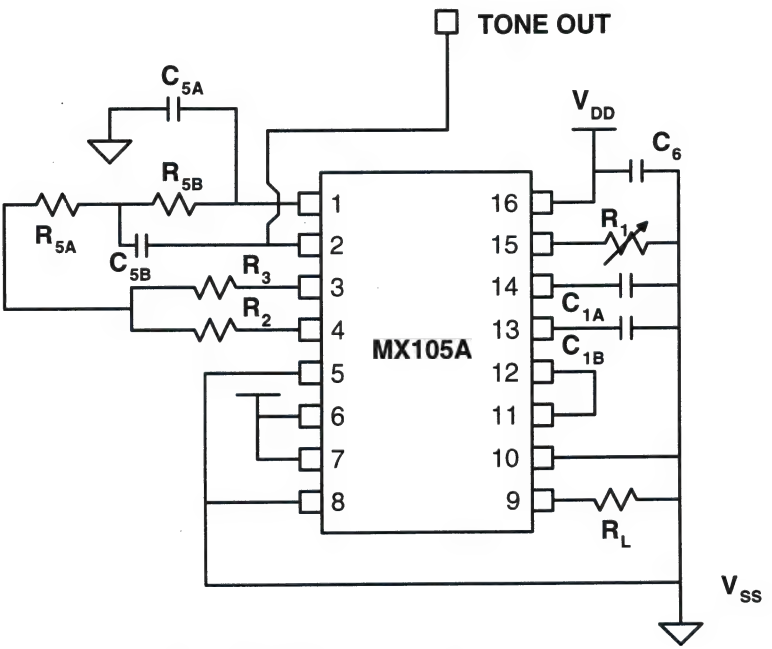


Figure 1. Simple Tone Generation Circuit using MX105A.

© 1997 MX•COM Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. #20830069.001
All trademarks and service marks are held by their respective companies.

1. Circuit Description for Tone Generation.

An RC oscillator (pins 13-15) generates an internal clock at six times the center frequency. This clock is internally decoded to sequentially enable four analog switches configured between pins 3 and 5 (SW3A), pins 3 and 6 (SW3B), pins 4 and 7 (SW2A), and pins 4 and 8 (SW2B). The control signals for these switches are shown in Figure 3. The switch connections to R2 and R3 form a simple Digital to Analog converter to produce a three level approximation of a sine wave (1 1 0 -1 -1 0 . . .) as shown in Figure 3. This waveform is well suited for tone generation as described below. Finally, a simple low pass filter formed with the on chip buffer amplifier smoothes the three level sine wave to produce a low distortion sine wave.

Note: a large value DC blocking capacitor should be used at pin 2 if pins 6 and 7 are driven for tone level control or amplitude modulation as shown in Figure 2.

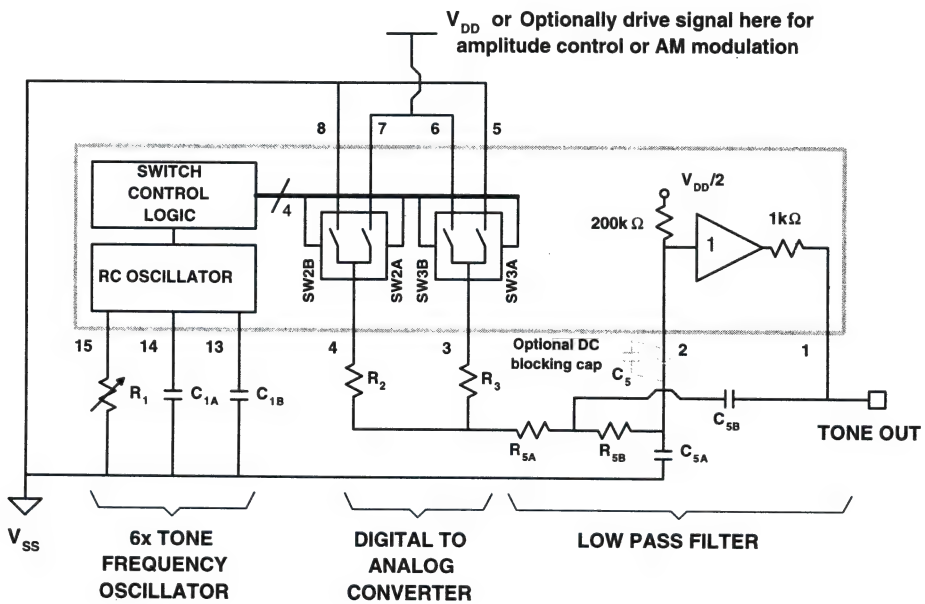


Figure 2. Block Diagram of Tone Generation Circuit.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830069.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

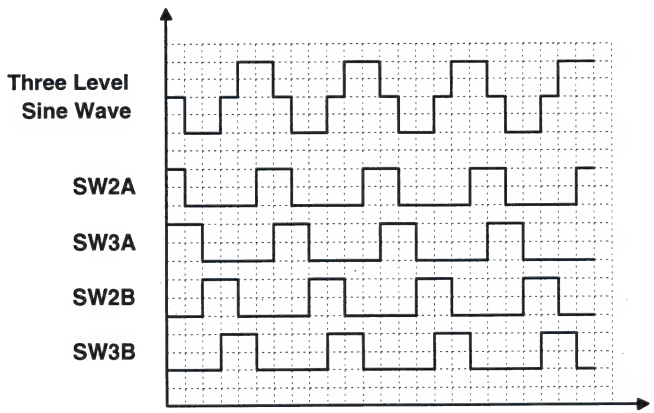


Figure 3. Internal Switch Control Signals and Resulting Three Level Waveform.

1.1 Fourier Series Analysis of the Three Level Waveform.

The periodic three level approximation of a sine wave can be represented by the following formula:

$$f(t) = \begin{cases} A & \text{for } |t| < \frac{T}{6} \\ 0 & \frac{T}{6} < |t| < \frac{T}{3} \\ -A & \text{for } \frac{T}{3} < |t| < \frac{T}{2} \end{cases} \qquad \text{where T is the period}$$

Fourier Series Expansion of f(t) yields the following coefficient formulas after some calculus:

$$a_n = \frac{2}{T}\int_0^T f(t)\cdot\cos\left(n\cdot\frac{2\pi}{T}\cdot t\right)dt$$

$$= \frac{2A}{n\cdot\pi}\sin\left(\frac{1}{3}\cdot n\cdot\pi\right)\cdot\left[1+2\cdot\cos\left(\frac{1}{3}\cdot n\cdot\pi\right)\right] \qquad \text{for positive integer n}$$

$$= \frac{2\cdot A\cdot\sqrt{3}}{\pi}\left[\frac{1}{1},0,0,0,-\frac{1}{5},0,\frac{1}{7},0,0,0,-\frac{1}{11},0,\frac{1}{13},\ldots\right]$$

$$b_n = \frac{2}{T}\int_0^T f(t)\cdot\sin\left(n\cdot\frac{2\pi}{T}\cdot t\right)dt = 0 \qquad \text{for positive integer n}$$

These coefficients result in the following fourier series representation:

$$f(t) = \frac{2\cdot A\cdot\sqrt{3}}{\pi}\left[\cos\left(\frac{2\pi}{T}t\right)-\frac{1}{5}\cos\left(5\frac{2\pi}{T}t\right)+\frac{1}{7}\cos\left(7\frac{2\pi}{T}t\right)-\frac{1}{11}\cos\left(11\frac{2\pi}{T}t\right)+\frac{1}{13}\cos\left(13\frac{2\pi}{T}t\right)+\ldots\right]$$

This function is plotted in the time domain in Figure 4 and in the frequency domain in Figure 5. It is clear from the frequency domain plot that the first harmonic spur above the fundamental, the fifth, is already about 14 dB down. Thus the required filtering to pass the fundamental while suppressing the harmonics is simplified compared to a square wave.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830069.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

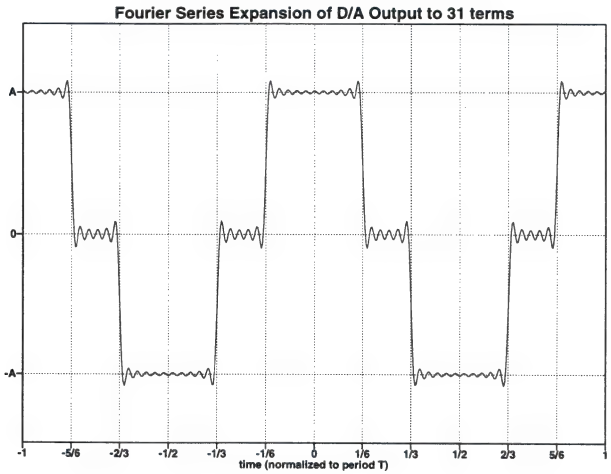


Figure 4. Time Domain Plot

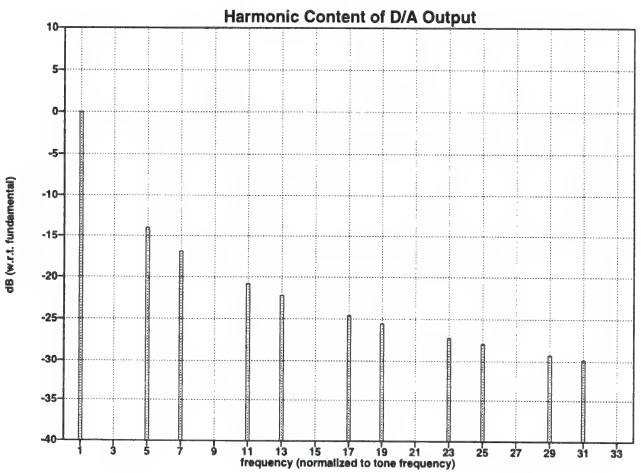


Figure 5. Frequency Domain Plot

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830069.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1.2 Analysis of the Low Pass Smoothing Filter

A simple second order filter can provide 12 dB per octave roll-off in the filter's stop band. Thus we can expect as much as 27 dB (i.e. $27dB \approx 12 \cdot \log_2(5)$) attenuation of the fifth harmonic and above with such a filter. This should produce a sine wave with distortion of about 1% (i.e. harmonics more than 40 dB down). More complex filtering can be used if lower distortion is required.

A simple second order low pass filter (formed with R5A, R5B, C5A, C5B, and the internal buffer amplifier between pins 1 and 2) suppresses the harmonics of the three level waveform to produce a low distortion (<1%) sine wave at pin 2. The transfer function of this low pass filter including effects of the input impedance of the MX105A buffer amplifier is:

$$H(j\omega) = \frac{\left[\frac{Ri}{R5A+R5B+Ri}\right]\cdot\left[\frac{R5A+R5B+Ri}{C5A\cdot C5B\cdot R5A\cdot R5B\cdot Ri}\right]}{\left[\frac{R5A+R5B+Ri}{C5A\cdot C5B\cdot R5A\cdot R5B\cdot Ri}-\omega^2\right]+\left[\frac{1}{C5A\cdot R5A}+\frac{1}{C5A\cdot R5B}+\frac{1}{C5B\cdot Ri}\right]j\omega}$$

choosing to let R = R5A = R5B and C5A = 2 C5B and substituting C = C5B results in

$$H(j\omega) = \frac{\left[\frac{Ri}{2R+Ri}\right]\cdot\left[\frac{2R+Ri}{2C^2\cdot R^2\cdot Ri}\right]}{\left[\frac{2R+Ri}{2C^2\cdot R^2\cdot Ri}-\omega^2\right]+\left[\frac{1}{C\cdot R}+\frac{1}{C\cdot Ri}\right]j\omega}$$

From this expression the equation for the pole frequency is: (f_p is plotted in Figure 6 to help in component choices).

$$\omega_p{}^2 = \left[\frac{2R+Ri}{2C^2\cdot R^2\cdot Ri}\right] \Rightarrow f_p = \frac{\sqrt{\frac{2R+Ri}{2C^2\cdot R^2\cdot Ri}}}{2\pi}$$

The equation for the Pass Band DC Gain is: (plotted in Figure 7 to help in component choices).

$$\text{DC Gain} = \frac{Ri}{2R+Ri}$$

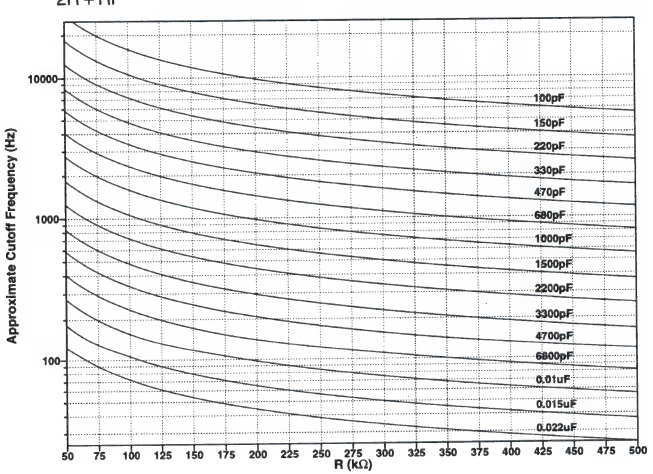


Figure 6. Approximate Cutoff Frequency Design Chart

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830069.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

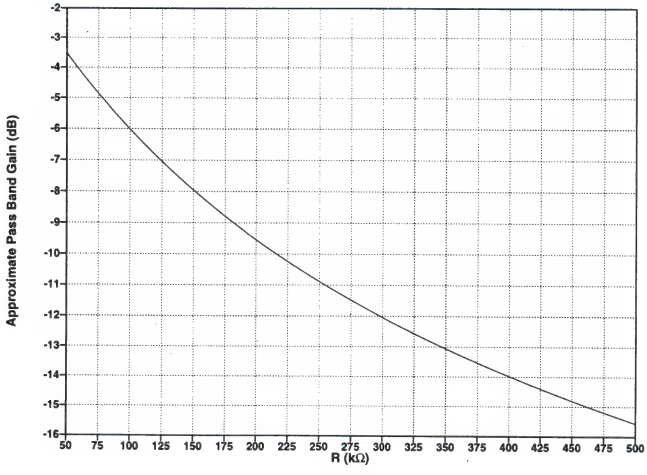


Figure 7. Approximate Filter Gain vs. R

Note that this filter provides attenuation in the pass band due to the input impedance of the buffer amplifier. The filtered tone level will be:

$$\text{Approximate Tone Level (in } V_{p\text{-}p}) = \frac{2 \cdot A \cdot \sqrt{3}}{\pi} \frac{Ri}{2R + Ri} \approx 1.1 \cdot A \cdot 10^{\left(\frac{\text{dB Gain}}{20}\right)}$$

where A is V_{DD} or optionally the level driven into pins 6 and 7 and dB Gain is read from Figure 7.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830069.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

2. A Worked Design Example - 1700 Hz Tone Generator

The tone frequency is set according to the standard formula in the MX105A data sheet:

$$F_0 = \frac{1}{6 \cdot R1 \cdot C1A \cdot \ln(2)} \qquad \text{with C1A = C1B}$$

To generate a 1700 Hz tone while choosing C1A = C1B = 680pF

$$R1 = \frac{1}{6 \cdot F_0 \cdot C1A \cdot \ln(2)} = \frac{1}{6 \cdot 1800 \cdot 680 \cdot 10^{-12} \cdot \ln(2)} = 208\ k\Omega$$

Choosing R1 = 150kΩ in series with a 100kΩ potentiometer will allow frequency tuning if required.

Referring to Figure 6 to pick R after choosing C = 680pF for the low pass filter results in:

R = R5A = R5B = 130kΩ

C = C5B = 680pF and C5A = 2 x C5B ≈ 1500pF

Calculating the approximate pole frequency to check design choices:

$$f = \frac{\sqrt{\frac{2R + Ri}{C5A \cdot C5B \cdot R^2 \cdot Ri}}}{2\pi} = 1838\ Hz \quad \text{(seems reasonable)}$$

Calculating the approximate tone level for V_{DD} = 5V results in:

$$\text{Tone Level} = 1.1 \cdot A \cdot 10^{\left(\frac{-7}{20}\right)} = 2.46\ V_{p-p} = 870\ mV_{RMS}$$

If tone amplidude control is required, drive a DC level (A) into pins 6 and 7 and use DC blocking capacitor C5 as shown in Figure 2.

Finally, choose R3 and R2 sufficiently low compared to R so as not to significantly affect the filter's frequency response and gain. For example, choose R3 = R2 = 10kΩ.

The filter graphs and design example are based on the typical buffer input impedance of 200kΩ. This parameter varies from device to device and with supply voltage. The input impedance is approximately proportional to $\frac{4}{V_{DD} - 1}$ and may vary from 160kΩ to 360kΩ at VDD = 5V. These figures are given to help the designer analyze for device variation; they are not guaranteed specifications! Refer to the MX105A for all specifications. A smoothing filter built with an external amplifier may eliminate these issues.

Note: In this design example the filter cut off may vary from 1720 Hz to 2120 Hz and the filter gain may vary from -8.2 dB to -4.6 dB due to the buffer 's input impedance. Even with these variations the second order filter should provide good attenuation of the 1700 Hz tone's 5th harmonic and above.

© 1997 MX•COM Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830069.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX029

Dual Digitally Controlled Amplifier

1. Introduction

The MX029 is a single-chip LSI circuit comprised of two individual, digitally controlled gain sections. Control of each gain section is accomplished through the serial interface. Each section has 48 distinct gain steps (+/-48dB of range in 2dB steps) plus MUTE. As shown in Figure 1 both gain stages have switchable inputs. This switching allows for selection of three different input signals on one channel and two on the other channel. One of the channels also has output switching. These features make it very easy to use the MX029 as a summing amplifier.

The MX029 can also be used as a digital to analog converter(DAC). For this application we take advantage of the 48 distinct gain settings. With a single DC input voltage the variable gain of the amplifier can be used to generate an analog output signal. This application note describes both applications, the MX029 as a summing amplifier and DAC.

Whenever the MX029 is used in any application the input signal should be as noise free as possible. Cutting off the serial clock when it is not being used will reduce noise. With high gain settings a very small amount of noise is amplified and becomes a problem.

When serial loading the MX029 make sure that the serial clock, serial data and LOAD/LATCH timing is correct. This seems to be a common problem for users, especially the timing of the LOAD/LATCH line. Use a storage scope to check your timing.

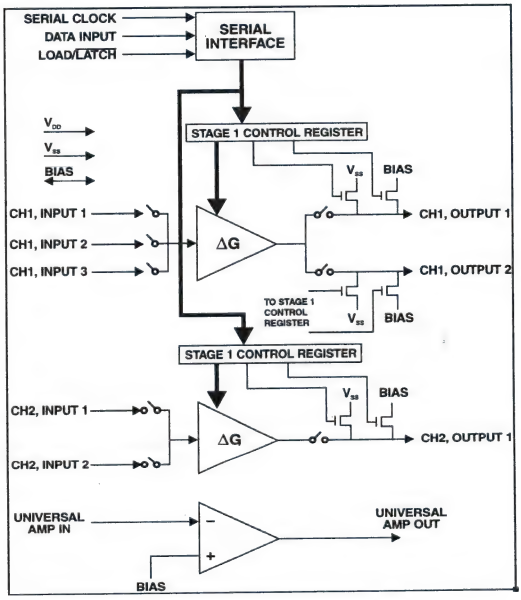


Figure 1: Device Block Diagram.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA.
All trademarks and service marks are held by their respective companies.
Doc. # 20830071.001

2. The MX029 as a Summing Amplifier

The MX029 can be used as a summing amplifier. Using channel one you can sum up to three different signals. With channel two you can sum two signals. As seen in Figure 2 very few external components are needed for the MX029 to be used as a summing amplifier.

The MX029 has an internal resistor that creates a voltage divider with R_{IN}. The configuration and value of this internal resistor is different in gain and attenuation mode, see Figure 2 and Figure 3. In gain mode the internal resistor is approximately 200KΩ and in attenuation mode the internal resistance is approximately 100KΩ. With a larger value of R_{IN} there will be more of a drop across R_{IN}. On the other hand, if the value of R_{IN} is too small the input source may not be able to drive R_{IN} due to source loading. Recommended values for R_{IN} are 10kΩ to 20kΩ. The equation used to calculate the signal level at the input of the MX029 for a two input summing amplifier is:

$$V_{IN\,029} = \frac{V_{IN1}(R_{IN2}R_L)}{R_{IN1}(R_{IN2}+R_L)+R_{IN2}R_L} + \frac{V_{IN2}(R_{IN1}R_L)}{R_{IN2}(R_{IN1}+R_L)+R_{IN1}R_L}$$

Where R_L is approximately 200KΩ in gain mode and 100KΩ in attenuation mode.

For a three input summing amplifier use the following equation :

$$V_{IN\,029} = \frac{V_{IN1}(R'//R_L)}{R_{IN1}+(R'//R_L)} + \frac{V_{IN2}(R''//R_L)}{R_{IN2}+(R''//R_L)} + \frac{V_{IN3}(R'''//R_L)}{R_{IN3}+(R'''//R_L)}$$

Where R' is the parallel combination of R_{IN2} and R_{IN3} (R_{IN2}// R_{IN3}) and R'' = R_{IN1}//R_{IN3} and R''' = R_{IN1}//R_{IN2} and R_L is approximately 200KΩ in gain mode and 100KΩ in attenuation mode.

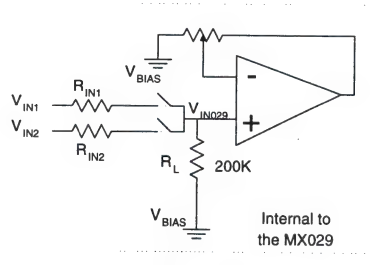


Figure 2: Gain Mode Configuration.

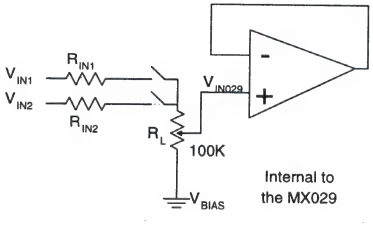


Figure 3: Attenuation Mode Configuration.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830071.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

3. The MX029 as a digital to analog converter

The MX029 can be used as a digital to analog converter. The input should be DC coupled not AC coupled. If the part is AC coupled it will not function as a DAC.

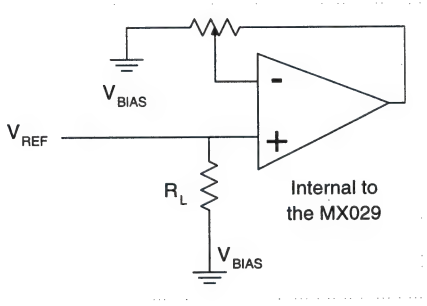


Figure 4: Using the MX029 as a DAC.

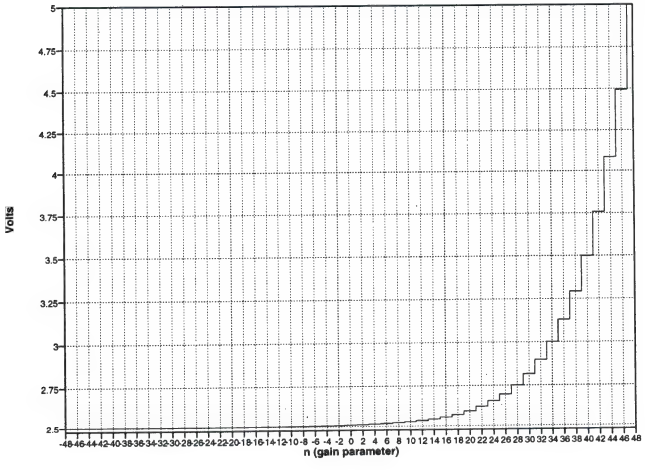


Figure 5: Volts vs. Gain Setting with V_{REF} at 2.51V.

When using the MX029 as a DAC there will be one input voltage(V_{REF}). To generate the output signal this input voltage is stepped up or down using the gain settings of the MX029. Each gain setting corresponds to a step on the output signal, see Figure 5. The minimum duration of each step(sample time) is approximately 8µs (giving a maximum sample rate of 125KHz). This is the time required to load and latch the 14 bits of serial data. This 125kHz sample rate can only be realized with negative gain settings. With gain settings 0dB to +30dB the amplifier's bandwidth will be the limiting factor and the maximum sample rate is approximately 20kHz. With gain settings above +30dB the maximum sample rate will be considerably less.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830071.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

The analog GND of the MX029 is at $V_{DD}/2$ (V_{BIAS}). With a 5 volt power supply this voltage is 2.5 volts. With V_{BIAS} at $V_{DD}/2$ a sign bit is needed to get output levels above and below V_{BIAS}, see Figure 6. When in gain (attenuation) mode the difference of V_{BIAS} and the reference voltage(V_{REF}) will be amplified (attenuated).

$$V_{OUT} = (V_{REF} - V_{BIAS})10^{\frac{n}{20}} + V_{BIAS}$$

Where n is the gain setting -48 to +48. For n = 0, $V_{OUT} = V_{REF}$, for n < 0, V_{OUT} is between V_{REF} and V_{BIAS}, and for n > 1, V_{OUT} is between V_{REF} and a supply rail.

For example if V_{REF} is 2.4 volts and V_{BIAS} is 2.5 volts, with a gain setting of +24dB the output signal will $(2.4 - 2.5)10^{1.2} + 2.5V = 0.915$ volts.

To calculate the gain of each 2dB step use the following formula:

$$Gain = 10^{\frac{n}{20}}$$

Where n is the gain setting -48 to +48.

Figure 7 is an example of an output signal generated by changing the gain settings where the full dynamic range of the MX029 is used. To generate the output signal above V_{BIAS}, V_{REF} needs to be approximately 10 millivolts above V_{BIAS}. And to generate the output signal below V_{BIAS}, V_{REF} needs to be approximately 10 millivolts below V_{BIAS}. When using input levels 10 millivolts above or below V_{BIAS}, the input referred offset voltage of the amplifier must be compensated for by adjusting V_{REF} accordingly. An input referred offset voltage of 10 millivolts is not uncommon for an MX029. For this reason it is not very practical to use values of V_{REF} that are so close to V_{BIAS}. In this application the higher and lower gain settings will typically not be used. It is important to recognize that above V_{BIAS} the range is approximately 2.5 volts to 4.7 volts and below V_{BIAS} it is approximately 0.3 volts to 2.5 volts. With a sign bit the range is approximately 4.4 volts.

$$n_{MAX} = 20\log\frac{2.2V}{|V_{REF} - V_{BIAS}|}$$

Where n_{MAX} is the maximum gain setting with a particular V_{REF}.

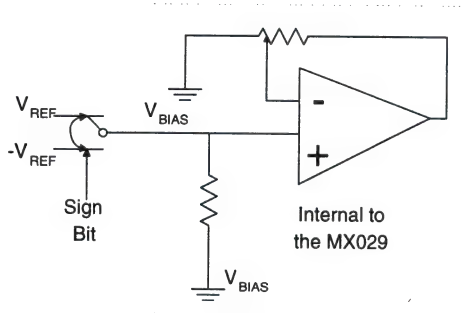


Figure 6: Using two V_{REF}s to generate an output that goes above and below V_{BIAS}.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830071.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

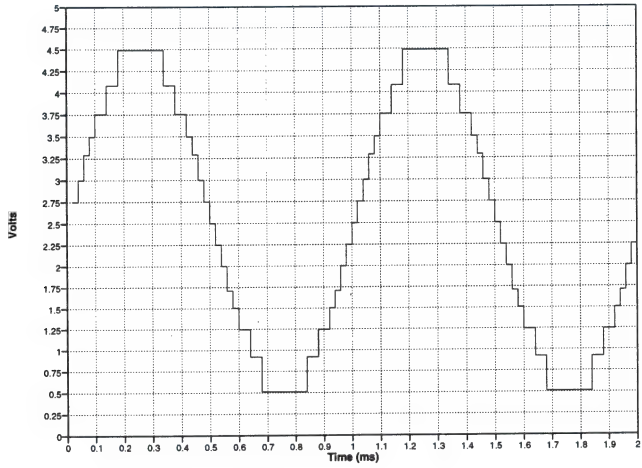


Figure 7: Example Output Signal.

Figure 7 is just one example of an output signal. There are many different output signals that can be generated. Before you start programming the MX029 take some time to think about what input signal level is necessary above or below V_{BIAS} to obtain the output signal that you desire.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830071.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

MX009 and MX019 Amplifier Array

The MX009 and MX019 offer 8 and 4 digitally controlled gain/attenuation amplifiers respectively.

MX009	MX019	
7 Amplifiers	3 Amplifiers	+3dB to -3dB adjustment range in 0.43dB steps
1 Amplifier	1 Amplifier	+15dB to -15dB adjustment range in 2dB steps

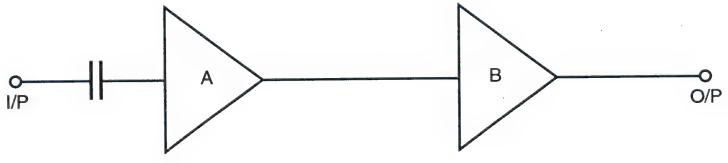
In certain applications it may be necessary to trim over a wider dynamic range or use smaller step sizes. This can be achieved by grouping the amplifier stages together either in series or parallel.

The 2 following examples show a typical application of:

1. Series connection of 2 amplifiers to achieve trimming over a 30dB dynamic range in 0.43dB steps.
2. Parallel connection of 2 amplifiers to achieve approximately 0.21dB steps over a 6dB dynamic range.

Example 1: 0.43dB steps over a 30dB dynamic range

This is achieved by connecting the volume amplifier stage in series with 1 of the other amplifier stages as shown in the diagram below.



Note:

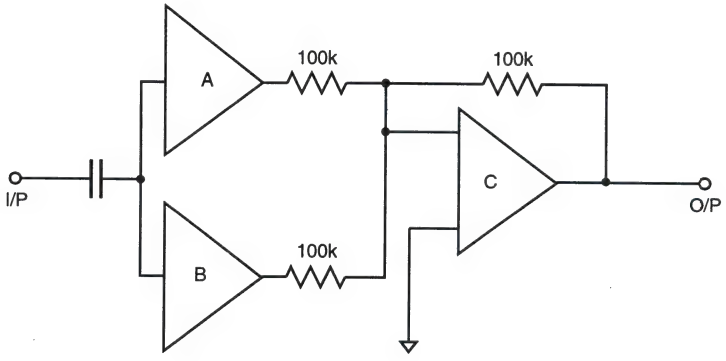
1. A - MX009 Amplifier no. 8 (MX009 Amplifier no.4) (Volume).
2. B - Any of the MX009 Amplifiers 1 through 7 (MX019 Amplifiers 1 through 3)

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

Doc. # 20830073.001

Example 2: 0.21dB steps over a 6dB dynamic range

A very fine step size of approximately 0.21dB can be obtained over a 6dB dynamic range by the connection of 2 amplifiers in parallel.



Note:

1. A & B - Any MX009 Amplifiers 1 through 7 (MX019 Amplifiers 1 through 3)
2. C - Standard CMOS Amplifier.

The table shows all possible combinations of gain on each of the 2 amplifiers, many of which are duplicated. The highlighted section shows 1 of the possible combinations to achieve an output dynamic of 6dB with approximately 0.21dB steps.

	3.00	2.57	2.14	1.71	1.29	0.86	0.43	0.00	-0.43	-0.86	-1.29	-1.71	-2.14	-2.57	-3.00
3.00	3.00	2.79	2.58	2.38	2.19	1.99	1.81	1.83	1.45	1.28	1.12	0.96	0.80	0.65	0.51
2.57	2.79	2.57	2.36	2.15	1.95	1.76	1.57	1.38	1.20	1.03	0.86	0.69	0.53	0.38	.022
2.14	2.58	2.36	2.14	1.93	1.72	1.52	1.33	1.14	0.95	0.77	0.60	0.43	0.26	0.10	-0.05
1.71	2.38	2.15	1.93	1.71	1.50	1.30	1.10	0.90	0.71	0.52	0.34	0.17	0.00	-0.17	-0.33
1.29	2.19	1.95	1.72	1.50	1.29	1.07	0.87	0.67	0.47	0.28	0.09	-0.09	-0.26	-0.43	-0.60
0.88	1.99	1.76	1.52	1.30	1.07	0.86	0.65	0.44	0.24	0.04	-0.15	-.033	-0.51	-0.69	-0.86
0.43	1.81	1.57	1.33	1.10	0.87	0.65	0.43	0.22	0.01	-0.19	-0.39	-0.58	-0.76	-0.94	-1.12
0.00	1.83	1.38	1.14	0.90	0.67	0.44	0.22	0.00	-.021	-0.42	-0.62	-0.81	-1.01	-1.19	-1.37
-0.43	1.45	1.20	0.95	0.71	0.47	0.24	0.01	-0.21	-0.43	-0.64	-0.85	-1.05	-1.24	-1.43	-1.62
-0.86	1.28	1.03	0.77	0.52	0.28	0.04	-0.19	-0.42	-0.84	-0.86	-1.07	-1.28	-1.48	-1.67	-1.86
-1.29	1.12	0.86	0.60	0.34	0.09	-0.15	-0.39	-0.62	-0.85	-1.07	-1.29	-1.50	-1.70	-1.90	-2.10
-1.71	0.96	0.69	0.43	0.17	-0.09	-0.33	-0.58	-0.81	-1.05	-1.28	-1.50	-1.71	-1.93	-2.13	-2.33
-2.14	0.80	0.53	0.26	0.00	-0.26	-0.51	-0.76	-1.01	-1.24	-1.48	-1.70	-1.93	-2.14	-2.35	-2.56
-2.57	0.65	0.38	0.10	-0.17	-0.43	-0.69	-0.94	-1.19	-1.43	-1.67	-1.90	-2.13	-2.35	-2.57	-2.78
-3.00	0.51	0.22	-0.05	-0.33	-0.60	-0.86	-1.12	-1.37	-1.62	-1.88	-2.10	-2.33	-2.56	-2.78	-3.00

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830017.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

APPLICATION NOTE

MX633/643 Noise Immunity Circuit for the MX633/643 Call Progress Detectors

Introduction

The telephone's central office sends call progress signals during the origination of a telephone call. Successful completion of each step of the connection process changes the call process signal. Call Progress Detectors, in computerized telephony equipment, provide quick progress detection for call automation applications.

Overview

The MX633 and MX643 are low power, low cost, call progress solutions. Both devices detect Dial Tone, Ring and Busy. The MX643 also detects international Special Information Tones (SIT). Both devices are capable of detecting tones levels down to -40dBm. Some applications are sensitive to noise. This application note provides an evaluation circuit for bread boarding purposes and discusses an approach for limiting the call progress detector's sensitivity to noise in poor signal to noise situations. Refer to the MX633 and MX643 data sheets for full details for device operation.

Noise Rejection Circuit

The schematic in Figure 2 page 3, depicts the MX643DW used in conjunction with a LM311 comparator. (The same circuit applies to MX633 use as well.) The comparator circuit (with hysteresis) provides audio signal conditioning for the call progress detector. Noise signals below a set threshold voltage are rejected. The comparator circuit is designed for single supply, +5.0VDC operation.

Circuit Description

Resistors R16, R3 and C5 form a 2.5 VDC reference bias applied to both inputs of the comparator through 100K Ω resistors, R2 and R4. Resistor R5 provides hysteresis (positive feedback) adjusting the threshold level above or below the 2.5V reference. When R5's value is 10 MΩ the signal level's threshold is approximately 18mVrms. Signals below 18mVrms do not trigger an output from the comparator. A power level of 0dBm represents 775 mVrms across 600 Ωs. Signal amplitudes below -32.7dBm (18mVrms referenced to 0dBm equal to 775mrms) are not presented to the input of the call progress detector.

The noise rejection circuit depicted in Figure 2 page 3, may require some adjustment depending on the application. Component tolerances of 5% for resistors and 10% for capacitors are used but should be set to reflect the requirements of the application.

Noise Rejection Threshold Adjustment

R5's value can vary to match noise rejection threshold requirements. Changing R5 from 10 MΩs to 20 MΩs results in a 9mVrms threshold. Changing R5 from 10 MΩs to 1 MΩs results in a 170mVrms threshold.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA.
Doc. # 20830017.002
All trademarks and service marks are held by their respective companies.

Circuit Layout Hints

LM311

The comparator circuit is sensitive to noise therefore the printed-circuit layout should be engineered with care to avoid sources of noise.

- Keep leads and traces short.
- Use a ground foil around the LM311 between inputs and outputs.
- Guard against capacitive coupling from high-level signals to the input pins.
- Route the LM311's output signal away from its input pins and pins 5 and 6.
- Place a bypass capacitor as close as practical across the power and ground pins.
- The device providing audio to the LM311 should have a low source impedance (1KΩ or less).

MX633 / MX643

The Call Progress Detector circuit is sensitive to noise therefore the printed-circuit layout should be engineered with care to avoid sources of noise.

- Keep leads and traces short.
- Use a ground foil around the MX633/643 between inputs and outputs.
- Guard against capacitive coupling from high-level signals to the input pins.
- Place a bypass capacitor as close as practical across the power and ground pins.
- If the supply source also powers digital logic additional filtering on the supply trace going to the MX633/643 should be considered.
- The device providing audio to the MX633/643 should have a low source impedance 10KΩ or less).
- Avoid stray capacitive coupling to crystal pins.

Audio Filtering

It is a good design practice to add an anti-aliasing filter prior to the LM311's input. The call progress detectors sample input signals at a 9.3 Khz rate. Care should be taken to avoid high frequency signals above 8.4khz as they will alias in the call detector's decoder. An anti-aliasing filter set at 5Khz is recommended in noisy environments where stray coupling of digital noise into the audio path is likely. Refer to Figure 1: Anti-aliasing Filter. If the input audio signal is buffered by an opamp in a previous stage, designers task of adding an anti-aliasing filter is simplified. Adding a capacitor across the opamp's feed back resistor, will form the desired anti-aliasing low pass filter. C2s value is calculated using the following.

$$f_{o\ @\text{-}3dB} = \frac{1}{(2\pi C_2 R_2)} \qquad C2 = \frac{1}{(2\pi\ 5KHz\ 100K\Omega)}$$

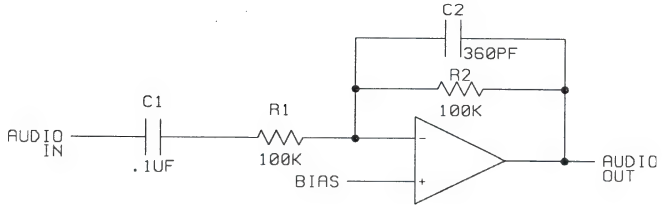


Figure 1: Anti-aliasing Filter

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830017.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

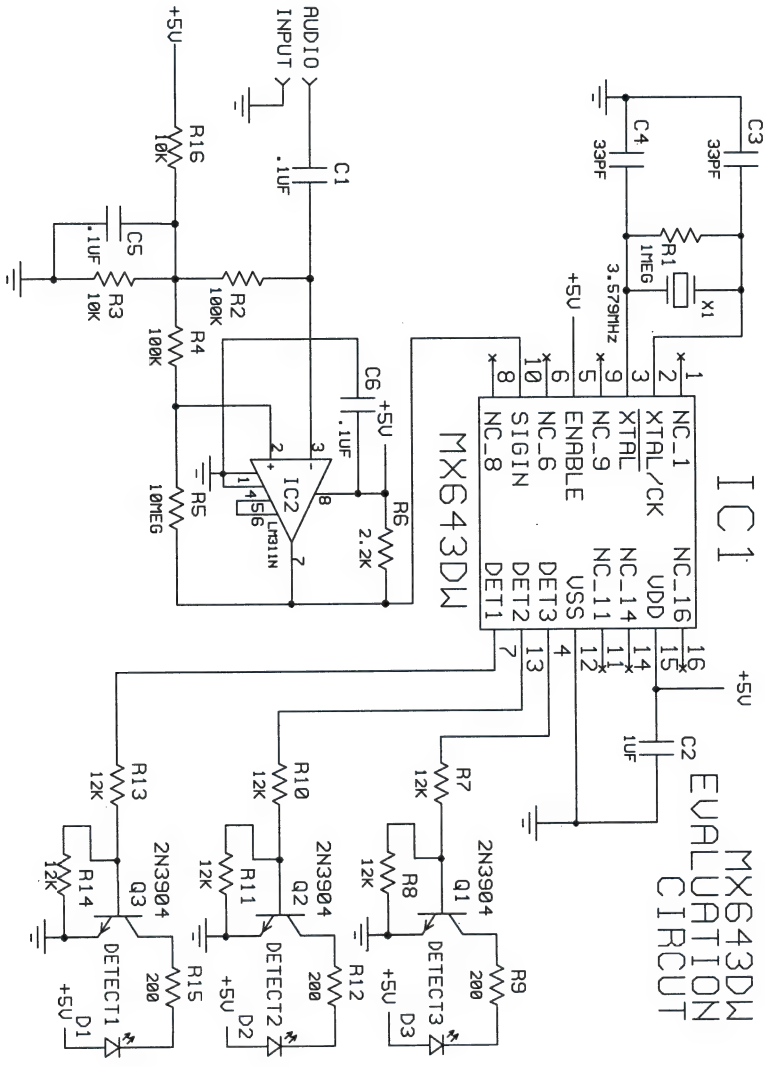


Figure 2: MX633DW Noise rejection circuit

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830017.002
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

SPM (Subscriber Pulse Metering) for PCMCIA, Data, and Fax Modems

Telephone Line Activity

All Fax machines, PC, and laptop Fax and data cards have a facility to report the "duration" of a Fax transmission in seconds and minutes.

The system relies on simple timing but gives no information as to the actual cost of each data transmission

A Call-Charge Report

By including an SPM detector (MX631) in the relevant equipment, a report can now be generated which actually reports the real cost of the 'call' in local currency.

This allows the machine to cost the differences between local and international calls and the use of peak- and cheap-rate dialing periods.

The Principals of Data and Fax Call-Charging

The MX631 SPM Detector monitors and detects 12kHz or 16kHz (SPM) call-charge pulses placed on the telephone line by the local telephone exchange. Each SPM pulse represents "one unit" of charge.

The number of pulses sent per second determines how expensive a particular telephone or Fax call is! In this respect, long-distance calls would have more pulses per second than a local call.

By using the detected output of the MX631 the host PC, Laptop or PDA can convert this received SPM information into actual cost. The conversion is achieved by multiplying the number of received SPM pulses for a given data transmission by the country's relevant "unit charge" [cost per pulse]. This unit-charge is a fixed rate in each country.

Transmission Cost = Number of received SPM pulses x Relevant unit charge for the country concerned

The "unit charge" would be programmed locally at installation of the modem or, multiple countries' charge rates would be held in memory. Increases in call charges could be taken care of automatically by the local telecomms authority increasing the rate of SPM pulses and not their unit value

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA.
All trademarks and service marks are held by their respective companies.
Doc. # 20830072.001

Error Detection & Correction of MPT1327 Formatted Messages

using MX429A or MX809 devices

1.1 Background

MPT1327 messages are transmitted as 64-bit 'codewords', where each codeword contains 48 information bits followed by 16 check bits:

Bit No:	1	48	49	64
	information field		check bits	

(Bit number 1 is transmitted first.)

These check bits allow the receive terminal to *detect* all odd numbers of errors, any 2 or 4 errors, and any error-burst up to length 16 in a codeword, and also to *correct* errors in the received codeword, although it should be noted that the higher the degree of error correction applied, the more likely is false decoding.

This document gives algorithms for:

Generation of the check bits of a transmitted codeword.
Received codeword *error detection*.
Limited *error correction* of a received codeword.

These algorithms may be used with any bit or byte oriented modem, such as the **MX429A** or **MX809**, although the **MX429A** and **MX809** devices can perform *check bit generation* and *error detection* automatically and the **MX429A** also provides a 16-bit 'Syndrome' output which may be used to aid *error correction*.

1.2 Generation of Transmit Codeword Check Bits

1.2.1 Theory

The first 15 check bits are derived from a (63,48) cyclic code by using codeword bits 1 to 48 as the coefficients X^{62} to X^{15} (in that order) of a 63 bit polynomial, which is then divided modulo-2 by the generating polynomial;

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + X^0 \qquad (11101000\ 00010101 \text{ binary})$$

On completion of the division, the 15 coefficients X^{14} to X^0 of the remainder are used as the first 15 check bits (codeword bits 49 to 63), with the X^0 coefficient (bit 63 of the complete codeword) inverted.
Finally, bit 64 of the codeword is added to provide an even parity check of the whole 64-bit codeword.

© 1997 MX-COM, Inc.
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
All trademarks and service marks are held by their respective companies.
Doc. # 20830066.001

1.2.2 Example of Transmit Codeword Generation

Information field; 6 data bytes

```
        89       AB       CD       EF       12       34     Hex
10001001 10101011 11001101 11101111 00010010 00110100  Binary
```

Polynomial division

```
      x62 ..................................................................... x0
10001001 10101011 11001101 11101111 00010010 00110100 00000000 0000000
11101000 00010101
 1100001 10111110 1
 1110100 00001010 1
   10101 10110100 010
   11101 00000010 101
    1000 10110110 1110
    1110 10000001 0101
     110 00110111 10111
     111 01000000 10101
       1 01110111 0001010
       1 11010000 0010101
         10100111 00111111
         11101000 00010101
          1001111 00101010 1
          1110100 00001010 1
           111011 00100000 01
           111010 00000101 01
                1 00100101 0010111
                1 11010000 0010101
                  11110101 00000101
                  11101000 00010101
                     11101 00010000 000
                     11101 00000010 101
                             10010 10110010 001
                             11101 00000010 101
                              1111 10110000 1001
                              1110 10000001 0101
                                 1 00110001 1100010
                                 1 11010000 0010101
                                   11100001 11101110
                                   11101000 00010101
                                      1001 11111011 0000
                                      1110 10000001 0101
                                       111 01111010 01010
                                       111 01000000 10101
                                             111010 11111000 00
                                             111010 00000101 01
                                                    11111101 0100000
```

Remainder with last bit inverted:

```
                                                    11111101 0100001
```

Complete codeword, including parity bit:

```
Bit; 1                                                                  64
10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000010
   89       AB       CD       EF       12       34       FD       42
```

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830066.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1.2.3 'C' Language Algorithm

```
/*************************************************************************/
/*    Function gen_ckbits() returns the first 15 check bits of a transmit  */
/*    codeword (codeword bits 49 to 63). Bit 15 of the returned value will */
/*    be codeword bit 49, bit 1 of the returned value will be codeword bit */
/*    63, and the lsb (bit 0) should be ignored.                           */
/*    The last bit (64) of the codeword must be derived separately, to     */
/*    give even parity of the whole 64-bit codeword.                       */

gen_ckbits()
    {
    int n,bit;
    unsigned int ckbits = 0;                    /* Clear check bits         */
    for(n=1;n <= 48;n++)                        /* 48 information bits......*/
        {                                       /*                          */
        bit = getbit_tx(n);                     /* Get each bit in turn ... */
        if( 1 & (bit ^ (ckbits >> 15)))         /*     XOR tx bit with MSB  */
                                                /*     of checkbits and if  */
                                                /*     the result == 1      */
            ckbits ^= 0x6815;                   /*     then XOR checkbits   */
                                                /*     with 6815 Hex        */
        ckbits <<= 1;                           /* ... Shift check bit word */
                                                /*        one bit left,     */
        }
    return(ckbits ^ 0x0002);                    /* Return checkbits with    */
                                                /* codeword bit 63 inverted */
    }

/*    Function getbit_tx(n) should return bit 'n' (1 to 48) of the transmit*/
/*    codeword information field.                                          */

getbit_tx(n)
    {
    return(/* 1 or 0 */);
    }
```

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830066.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1.3 Receive Codeword Checking & Error Correction

1.3.1 Theory

The parity of the received 64-bit codeword is checked, then bit 63 of the codeword is inverted. The first 63 bits of the resulting codeword are then used as the coefficients X77 to X15 of a 77 bit polynomial, which is then divided modulo-2 by the 'generating polynomial'. If the remainder is zero, and the parity check is met, then no errors have been detected.

The 15-bit remainder of this division is used as the least significant 15 bits of the 16-bit 'Syndrome' word generated by the MX429 (and by the algorithm of section 3.4), while the msb of the Syndrome word is set to '1' if the parity of the received codeword is incorrect. The resulting Syndrome word value can give an indication of which bit(s) of the codeword have been received incorrectly; see section 3.4.

1.3.2 Example of Receive Codeword Checking: No Errors

Received codeword: 6 bytes:

```
        89       AB       CD       EF       12       34       FD       42
     10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000010
  Bit;1                                                                    64
```

Step 1: even parity checked OK

Step 2: invert bit 63 then divide first 63 bits (shifted left 15 places) by generating polynomial:

```
x77 ..........................................................................x0
10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000000 00000000 000000
11101000 00010101
 1100001 10111110 1
 1110100 00001010 1
   10101 10110100 010
   11101 00000010 101
    1000 10110110 1110
    1110 10000001 0101
     110 00110111 10111
     111 01000000 10101
       1 01110111 0001010
       1 11010000 0010101
         10100111 00111111
         11101000 00010101
          1001111 00101010 1
          1110100 00001010 1
           111011 00100000 01
           111010 00000101 01
                1 00100101 0010111
                1 11010000 0010101
                  11110101 00000101
                  11101000 00010101
                     11101 00010000 000
                     11101 00000010 101
                              10010 10110010 001
                              11101 00000010 101
                               1111 10110000 1001
                               1110 10000001 0101
                                  1 00110001 1100010
                                  1 11010000 0010101
                                    11100001 11101110
                                    11101000 00010101
                                        1001 11111011 1111
                                        1110 10000001 0101
                                         111 01111010 10101
                                         111 01000000 10101
                                               111010 00000101 01
                                               111010 00000101 01
                                               000000 00000000 00000000 00000000 000000
```

Remainder = zero
MX429 'Syndrome' word: 00000000 00000000
No errors detected

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830066.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1.3.3 Example of Receive Codeword Checking: 2 Errors

Received codeword: 6 bytes: bits 9 & 10 in error

```
         89       6B       CD       EF       12       34       FD       42
      10001001 01101011 11001101 11101111 00010010 00110100 11111101 01000010
       errors; xx
  Bit;1                                                                    64
```

Step 1: even parity checked OK

Step 2: invert bit 63 then divide first 63 bits (shifted left 15 places) by generating polynomial:

```
x77 ..........................................................................x0
10001001 01101011 11001101 11101111 00010010 00110100 11111101 01000000 00000000 000000
11101000 00010101
 1100001 01111110 1
 1110100 00001010 1
   10101 01110100 010
   11101 00000010 101
    1000 01110110 1110
    1110 10000001 0101
     110 11110111 10111
     111 01000000 10101
       1 10110111 0001010
       1 11010000 0010101
          1100111 00111111 1
          1110100 00001010 1
            10011 00110101 011
            11101 00000010 101
             1110 00110111 1100
             1110 10000001 0101
                  10110110 10011111
                  11101000 00010101
                   1011110 10001010 0
                   1110100 00001010 1
                    101010 10000000 10
                    111010 00000101 01
                     10000 10000101 110
                     11101 00000010 101
                      1101 10000111 0111
                      1110 10000001 0101
                        11 00000110 001000
                        11 10100000 010101
                           10100110 01110110
                           11101000 00010101
                            1001110 01100011 0
                            1110100 00001010 1
                             111010 01101001 10
                             111010 00000101 01
                                    1101100 11110100 1
                                    1110100 00001010 1
                                      11000 11111110 011
                                      11101 00000010 101
                                        101 11111100 11011
                                        111 01000000 10101
                                         10 10111100 011101
                                         11 10100000 010101
                                          1 00011100 0010000
                                          1 11010000 0010101
                                            11001100 00001011
                                            11101000 00010101
                                              100100 00011110 01
                                              111010 00000101 01
                                               11110 00011011 000
                                               11101 00000010 101
                                                  11 00011001 101000
                                                  11 10100000 010101
```

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830066.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

```
                                    10111001 11110100
                                    11101000 00010101
                                     1010001 11100001 0
                                     1110100 00001010 1
                                      100101 11101011 10
                                      111010 00000101 01
                                       11111 11101110 110
                                       11101 00000010 101
                                          10 11101100 011000
                                          11 10100000 010101
                                           1 01001100 0011010
                                           1 11010000 0010101
                                             10011100 00011110
                                             11101000 00010101
                                              1110100 00001011 0
                                              1110100 00001010 1
```

Remainder; non zero

```
                                                        1 100000
```

MX429 'Syndrome' word: `00000000 01100000`

Therefore, from the table in section 3.4, codeword bits 9 & 10 of the received codeword are incorrect.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830066.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1.3.4 'C' Language Algorithm

The following algorithm produces a 16-bit 'Syndrome'similar to that generated by the MX429, which will have a value of zero only if no errors have been detected in the received codeword.

```
/*************************************************************************/
/*    Function calc_syndrome() returns the 16-bit 'Syndrome' of a received */
/*    MPT1327 64-bit codeword.                                             */

calc_syndrome()
    {
    int n,bit;
    int parity=0;                                  /* Clear parity register    */
    int syndrome=0;                                /* Clear 16-bit syndrome    */
    for(n = 1;n <= 64;n++)                         /* 64-bit codeword...       */
        {                                          /*                          */
         bit = getbit_rx(n);                       /* Get each bit in turn;..  */
         parity ^= bit;                            /* .. update parity         */
         if(n == 63) bit ^= 1;                     /* .. then invert bit 63    */
         if(n < 64)                                /* .. for bits 1 to 63;.... */
            {                                      /*    .. shift parity word  */
            syndrome <<= 1;                        /*          one bit left.   */
            if( 1 & (bit ^ (syndrome >> 15)))      /*    .. XOR rx bit with    */
                                                   /*       MSB of parity word,*/
                                                   /*       and if result == 1 */
                syndrome ^= 0x6815;                /*       then XOR syndrome  */
                                                   /*       with 6815 Hex.     */
            }                                      /*                          */
        }
    syndrome &= 0x7FFF;                            /* Finally, replace MSB of  */
    if(parity)                                     /*  syndrome word with the  */
        syndrome |= 0x8000;                        /*  calculated parity bit   */
    return(syndrome);
    }

/*    Function getbit_rx(n) should return the bit 'n' of the received      */
/*    codeword; Bit '1' is the first bit to be received, bit '64' the last.*/

getbit_rx(n)
    {
    return(/* 1 or 0 */);
    }
```

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830066.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

1.4 Error Correction

Single-bit and bit-pair errors in a received codeword may be corrected by comparing the 'Syndrome' word (generated by the MX429 or the algorithm of section 3.4) against the entries in the following table, and if a match is found inverting the corresponding bits.

Syndrome (Hex)	Error bits	Syndrome (Hex)	Error bits	Syndrome (Hex)	Error bits	Syndrome (Hex)	Error bits
0003	14, 15	468D	40, 41	8001	15	B456	25
0006	13, 14	4841	61, 62	8002	14	B484	19
000C	12, 13	4989	33, 34	8004	13	B83F	62
0018	11, 12	4B7B	45, 46	8008	12	B887	34
0030	10, 11	4BD7	22, 23	8010	11	B929	46
0060	9, 10	4E0F	16, 17	8020	10	B94D	23
00C0	8, 9	502A	62, 63	8040	9	BA05	17
0180	7, 8	50CE	34, 35	8080	8	C000	1
0300	6, 7	51B7	46, 47	8100	7	C02E	36
0600	5, 6	51E1	23, 24	8200	6	C31C	50
0C00	4, 5	530D	17, 18	8400	5	C60A	39
15D3	43, 44	574C	41, 42	8800	4	C748	57
1763	20, 21	5A62	48, 49	88E9	60	C885	28
1800	3, 4	5CD1	47, 48	8A09	32	CA3E	54
18CD	28, 29	5CFA	24, 25	8CB1	44	D048	29
193B	59, 60	5D8C	18, 19	8D21	21	E401	38
1E1B	31, 32	6000	1, 2	9000	3	E588	41
21CD	56, 57	6039	36, 37	90C7	52	E685	56
220B	38, 39	6292	50, 51	91D2	59	E815	63
2867	35, 36	6334	26, 27	9412	31	E849	35
2BA6	42, 43	64EC	57, 58	9962	43	E89E	47
2D31	49, 50	650F	39, 40	9A2B	26	E8AC	24
2E7D	25, 26	6815	63, 64	9A42	20	E908	18
2EC6	19, 20	6CAE	52, 53	A000	2	EE2D	49
3000	2, 3	6F21	54, 55	A017	37	F07E	61
3149	51, 52	740B	15, 16	A18E	51	F10E	33
319A	27, 28	786C	29, 30	A305	40	F252	45
3276	58, 59	7897	60, 61	A3A4	58	F29A	22
3657	53, 54	7B07	32, 33	A51F	55	F40A	16
3C36	30, 31	7EE3	44, 45	A824	30	F91F	27
439A	55, 56	7FBB	21, 22	B2C4	42	FC69	53
4416	37, 38	8000	64	B44F	48		

Example:
Transmitted codeword:

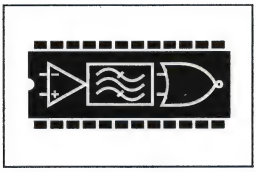
```
Bit; 1                                                                    64
     10001001 10101011 11001101 11101111 00010010 00110100 11111101 01000010
      errors; xx
```

Received codeword:

```
     10001001 01101011 11001101 11101111 00010010 00110100 11111101 01000010
```

For this received codeword, the 'Syndrome' will be 0060H, which appears in the table, indicating that the 9th & 10th bits received are incorrect and should be inverted.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830066.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.



MX•COM, INC. MiXed Signal ICs

APPLICATION NOTE

Generation of Non-Standard CTCSS Tones

MX•COM manufactures several integrated circuits which encode and decode CTCSS tones at the EIA RS-220 standard frequencies. In many instances, however, using tones of slightly different frequencies may be desirable. Because these MX•COM ICs use switched capacitor technology, tone frequencies may shifted simply by changing the crystal or clock input. The following five tables list alternative tones which can be encoded and decoded by the MX165C, MX365A, MX465, and the MX375, and encoded by the MX315A.

Each table lists the tone frequencies for three crystal values for each chip. The MX165C, MX315A and MX365A use a nominal crystal value of 1.0 MHz; the table lists tone frequencies for 1.008 MHz and 1.024 MHz crystals as well as for 1.0 MHz. The MX375 and MX465 uses a 4.0 MHz nominal crystal value; these tables lists frequencies for 4.0 MHz, 4.032 MHz, and 4.096 MHz crystals. The column labeled as "Divisor" for each table lists the quotient of the clock frequency divided by the tone frequency. This column can be used to calculate the clock frequency required to generate other tone frequencies. Each table also lists the (D5-D0 program code input associated with each divisor and tone frequency group. Each code is listed in both binary and hexadecimal formats. As an example, to encode a 70.0 Hz tone with the program code input D5-D0 = 011111 (1F Hex, the required clock would be calculated in the following manner:

D5	D4	D3	D2	D1	D0
0	1	1	1	1	1

Divisor = 13908
Tone frequency = 70.0 Hz
Required clock frequency = Divisor * Tone Frequency
= 13908 * 70.0 Hz
= 973560 Hz

When using these ICs in this manner, you must remember the following:

1. When the clock is changed, the audio pass band limits will change proportionately. These changes will be fairly small, however. For example, in the MX165C using a 1.024 MHz crystal, the lower limit will change to (1.024/1.0 * 300 = 307 Hz, and the upper limit will change to (1.024/1.0 * 3000 = 3072 Hz.
2. In the MX375, the frequency inversion carrier frequency will also change proportionately from its nominal value of 3333 Hz. For example, with a 4.096 MHz clock, the carrier frequency will change to (4.096/4.0 * 3333 Hz = 3413 Hz. For proper communication, the transmitter and receiver must use the same inversion carrier frequency.

© 1997 MX•COM, INC.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA.
Doc. # 20830061.001
All trademarks and service marks are held by their respective companies.

MX315A										
				Program Codes						
	Xtal Freq	Xtal Freq	Xtal Freq	Binary Codes						HEX
Divisor	1.0 MHz	1.008 MHz	1.024 MHz	D5	D4	D3	D2	D1	D0	
14912	67.06	67.60	68.67	1	1	1	1	1	1	3F
14415	69.37	69.93	71.04	1	1	1	0	0	1	39
13920	71.84	72.41	73.56	0	1	1	1	1	1	1F
13454	74.33	74.92	76.11	1	1	1	1	1	0	3E
12989	76.99	77.61	78.84	0	0	1	1	1	1	0F
12555	79.65	80.29	81.56	1	1	1	1	0	1	3D
12121	82.50	83.16	84.48	0	1	1	1	1	0	1E
11718	85.34	86.02	87.39	1	1	1	1	0	0	3C
11284	88.62	89.33	90.75	0	0	1	1	1	0	0E
10943	91.38	92.11	93.57	1	1	1	0	1	1	3B
10540	94.88	95.64	97.16	0	1	1	1	0	1	1D
10261	97.46	98.24	99.80	1	1	1	0	1	0	3A
10013	99.87	100.67	102.27	0	0	1	1	0	1	0D
9672	103.39	104.22	105.87	0	1	1	1	0	0	1C
9331	107.17	108.03	109.74	0	0	1	1	0	0	0C
9021	110.85	111.74	113.51	0	1	1	0	1	1	1B
8711	114.80	115.72	117.56	0	0	1	0	1	1	0B
8432	118.60	119.55	121.45	0	1	1	0	1	0	1A
8122	123.12	124.10	126.07	0	0	1	0	1	0	0A
7843	127.50	128.52	130.56	0	1	1	0	0	1	19
7595	131.67	132.72	134.83	0	0	1	0	0	1	09
7316	136.69	137.78	139.97	0	1	1	0	0	0	18
7068	141.48	142.61	144.88	0	0	1	0	0	0	08
6851	145.96	147.13	149.46	0	1	0	1	1	1	17
6603	151.45	152.66	155.08	0	0	0	1	1	1	07
6386	156.59	157.84	160.35	0	1	0	1	1	0	16
6169	162.10	163.40	165.99	0	0	0	1	1	0	06
5952	168.01	169.35	172.04	0	1	0	1	0	1	15
5766	173.43	174.82	177.59	0	0	0	1	0	1	05
5549	180.21	181.65	184.54	0	1	0	1	0	0	14
5363	186.46	187.95	190.94	0	0	0	1	0	0	04
5177	193.16	194.71	197.80	0	1	0	0	1	1	13
4929	202.88	204.50	207.75	0	0	0	0	1	1	03
4836	206.78	208.44	211.75	1	1	1	0	0	0	38
4743	210.84	212.53	215.90	0	1	0	0	1	0	12
4588	217.96	219.70	223.19	0	0	0	0	1	0	02
4433	225.58	227.38	230.99	0	1	0	0	0	1	11
4278	233.75	235.62	239.36	0	0	0	0	0	1	01
4123	242.54	244.48	248.36	0	1	0	0	0	0	10
3999	250.06	252.06	256.06	0	0	0	0	0	0	00

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830061.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

MX365A										
				Program Codes						
	Xtal Freq	Xtal Freq	Xtal Freq	Binary Codes						HEX
Divisor	1.0 MHz	1.008 MHz	1.024 MHz	D5	D4	D3	D2	D1	D0	
14914	67.05	67.59	68.66	1	1	1	1	1	1	3F
14426	69.32	69.87	70.98	1	1	1	0	0	1	39
13908	71.90	72.48	73.63	0	1	1	1	1	1	1F
13450	74.35	74.94	76.13	1	1	1	1	1	0	3E
12994	76.96	77.58	78.81	0	0	1	1	1	1	0F
12536	79.77	80.41	81.68	1	1	1	1	0	1	3D
12108	82.59	83.25	84.57	0	1	1	1	1	0	1E
11712	85.38	86.06	87.43	1	1	1	1	0	0	3C
11285	88.61	89.32	90.74	0	0	1	1	1	0	0E
10919	91.58	92.31	93.78	1	1	1	0	1	1	3B
10553	94.76	95.52	97.03	0	1	1	1	0	1	1D
10279	97.29	98.07	99.62	1	1	1	0	1	0	3A
10004	99.96	100.76	102.36	0	0	1	1	0	1	0D
9668	103.43	104.26	105.91	0	1	1	1	0	0	1C
9333	107.15	108.01	109.72	0	0	1	1	0	0	0C
9028	110.77	111.66	113.43	0	1	1	0	1	1	1B
8723	114.64	115.56	117.39	0	0	1	0	1	1	0B
8418	118.80	119.75	121.65	0	1	1	0	1	0	1A
8143	122.80	123.78	125.75	0	0	1	0	1	0	0A
7869	127.08	128.10	130.13	0	1	1	0	0	1	19
7595	131.67	132.72	134.83	0	0	1	0	0	1	09
7320	136.61	137.70	139.89	0	1	1	0	0	0	18
7076	141.32	142.45	144.71	0	0	1	0	0	0	08
6832	146.37	147.54	149.88	0	1	0	1	1	1	17
6619	151.09	152.30	154.72	0	0	0	1	1	1	07
6374	156.88	158.14	160.65	0	1	0	1	1	0	16
6161	162.31	163.61	166.21	0	0	0	1	1	0	06
5947	168.14	169.49	172.18	0	1	0	1	0	1	15
5764	173.48	174.87	177.64	0	0	0	1	0	1	05
5551	180.15	181.59	184.47	0	1	0	1	0	0	14
5368	186.29	187.78	190.76	0	0	0	1	0	0	04
5185	192.86	194.40	197.49	0	1	0	0	1	1	13
4910	203.65	205.28	208.54	0	0	0	0	1	1	03
4758	210.17	211.85	215.21	0	1	0	0	1	0	12
4575	218.58	220.33	223.83	0	0	0	0	1	0	02
4422	226.12	227.93	231.55	0	1	0	0	0	1	11
4270	234.19	236.06	239.81	0	0	0	0	0	1	01
4148	241.08	243.01	246.87	0	1	0	0	0	0	10
3996	250.28	252.28	256.29	0	0	0	0	0	0	00

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830061.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

MX375										
				Program codes						
	Xtal Freq	Xtal Freq	Xtal Freq	Binary codes						HEX
Divisor	4.0 MHz	4.032 MHz	4.096 MHz	D5	D4	D3	D2	D1	D0	
59657	67.05	67.59	68.66	1	1	1	1	1	1	3F
55633	71.90	72.48	73.63	0	1	1	1	1	1	1F
53800	74.35	74.94	76.13	1	1	1	1	1	0	3E
51975	76.96	77.58	78.81	0	0	1	1	1	1	0F
50144	79.77	80.41	81.68	1	1	1	1	0	1	3D
48432	82.59	83.25	84.57	0	1	1	1	1	0	1E
46849	85.38	86.06	87.43	1	1	1	1	0	0	3C
45142	88.61	89.32	90.74	0	0	1	1	1	0	0E
43678	91.58	92.31	93.78	1	1	1	0	1	1	3B
42212	94.76	95.52	97.03	0	1	1	1	0	1	1D
41114	97.29	98.07	99.62	1	1	1	0	1	0	3A
40016	99.96	100.76	102.36	0	0	1	1	0	1	0D
38673	103.43	104.26	105.91	0	1	1	1	0	0	1C
37331	107.15	108.01	109.72	0	0	1	1	0	0	0C
36111	110.77	111.66	113.43	0	1	1	0	1	1	1B
34892	114.64	115.56	117.39	0	0	1	0	1	1	0B
33670	118.80	119.75	121.65	0	1	1	0	1	0	1A
32573	122.80	123.78	125.75	0	0	1	0	1	0	0A
31476	127.08	128.10	130.13	0	1	1	0	0	1	19
30379	131.67	132.72	134.83	0	0	1	0	0	1	09
29280	136.61	137.70	139.89	0	1	1	0	0	0	18
28305	141.32	142.45	144.71	0	0	1	0	0	0	08
27328	146.37	147.54	149.88	0	1	0	1	1	1	17
26474	151.09	152.30	154.72	0	0	0	1	1	1	07
25497	156.88	158.14	160.65	0	1	0	1	1	0	16
24644	162.31	163.61	166.21	0	0	0	1	1	0	06
23790	168.14	169.49	172.18	0	1	0	1	0	1	15
23057	173.48	174.87	177.64	0	0	0	1	0	1	05
22204	180.15	181.59	184.47	0	1	0	1	0	0	14
21472	186.29	187.78	190.76	0	0	0	1	0	0	04
20740	192.86	194.40	197.49	0	1	0	0	1	1	13
19642	203.65	205.28	208.54	0	0	0	0	1	1	03
19032	210.17	211.85	215.21	0	1	0	0	1	0	12
18300	218.58	220.33	223.83	0	0	0	0	1	0	02
17690	226.12	227.93	231.55	0	1	0	0	0	1	11
17080	234.19	236.06	239.81	0	0	0	0	0	1	01
16592	241.08	243.01	246.87	0	1	0	0	0	0	10
15982	250.28	252.28	256.29	0	0	0	0	0	0	00

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830061.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

MX165C										
				Program Codes						
	Xtal Freq	Xtal Freq	Xtal Freq	Binary Codes						Hex
Divisor	1.0MHz	1.008MHz	1.024MHz	D5	D4	D3	D2	D1	D0	
14930	66.98	67.52	68.59	1	1	1	1	1	1	3F
14426	69.32	69.87	70.98	1	1	1	0	0	1	39
13908	71.901	72.48	73.63	0	1	1	1	1	1	1F
13435	74.431	75.03	76.22	1	1	1	1	1	0	3E
12993	76.965	77.58	78.81	0	0	1	1	1	1	0F
12551	79.677	80.31	81.59	1	1	1	1	0	1	3D
12124	82.483	83.14	84.46	0	1	1	1	1	0	1E
11712	85.383	86.07	87.43	1	1	1	1	0	0	3C
11300	88.494	89.20	90.62	0	0	1	1	1	0	0E
10934	91.456	92.19	93.65	1	1	1	0	1	1	3B
10553	94.76	95.52	97.03	0	1	1	1	0	1	1D
10263	97.435	98.21	99.77	1	1	1	0	1	0	3A
10004	99.96	100.76	102.36	0	0	1	1	0	1	0D
9668	103.429	104.26	105.91	0	1	1	1	0	0	1C
9333	107.147	108.00	109.72	0	0	1	1	0	0	0C
9013	110.954	111.84	113.62	0	1	1	0	1	1	1B
8708	114.84	115.76	117.60	0	0	1	0	1	1	0B
8418	118.793	119.74	121.64	0	1	1	0	1	0	1A
8128	123.028	124.01	125.98	0	0	1	0	1	0	0A
7854	127.328	128.35	130.38	0	1	1	0	0	1	19
7595	131.674	132.73	134.83	0	0	1	0	0	1	9
7320	136.612	137.70	139.89	0	1	1	0	0	0	18
7076	141.323	142.45	144.71	0	0	1	0	0	0	8
6847	146.044	147.21	149.55	0	1	0	1	1	1	17
6603	151.441	152.65	155.08	0	0	0	1	1	1	7
6375	156.875	158.13	160.64	0	1	0	1	1	0	16
6161	162.311	163.61	166.21	0	0	0	1	1	0	6
5963	167.708	169.05	171.73	0	1	0	1	0	1	15
5749	173.936	175.33	178.11	0	0	0	1	0	1	5
5566	179.654	181.09	183.97	0	1	0	1	0	0	14
5368	186.289	187.78	190.76	0	0	0	1	0	0	4
5185	192.864	194.41	197.49	0	1	0	0	1	1	13
4911	203.645	205.27	208.53	0	0	0	0	1	1	3
4743	210.848	212.53	215.91	0	1	0	0	1	0	12
4590	217.853	219.60	223.08	0	0	0	0	1	0	2
4438	225.339	227.14	230.75	0	1	0	0	0	1	11
4285	233.359	235.23	238.96	0	0	0	0	0	1	01
4133	241.97	243.91	247.78	0	1	0	0	0	0	10
3995	250.282	252.28	256.29	0	0	0	0	0	0	00

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830061.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

MX465										
				Program Codes						
	Xtal Freq	Xtal Freq	Xtal Freq	Binary Codes						Hex
Divisor	4.0MHz	4.032MHz	4.096MHz	D5	D4	D3	D2	D1	D0	
59719	66.98	67.52	68.59	1	1	1	1	1	1	3F
57703	69.32	69.87	70.98	1	1	1	0	0	1	39
55632	71.901	72.48	73.63	0	1	1	1	1	1	1F
53741	74.431	75.03	76.22	1	1	1	1	1	0	3E
51972	76.965	77.58	78.81	0	0	1	1	1	1	0F
50203	79.677	80.31	81.59	1	1	1	1	0	1	3D
48495	82.483	83.14	84.46	0	1	1	1	1	0	1E
46848	85.383	86.07	87.43	1	1	1	1	0	0	3C
45201	88.494	89.20	90.62	0	0	1	1	1	0	0E
43737	91.456	92.19	93.65	1	1	1	0	1	1	3B
42212	94.76	95.52	97.03	0	1	1	1	0	1	1D
41053	97.435	98.21	99.77	1	1	1	0	1	0	3A
40016	99.96	100.76	102.36	0	0	1	1	0	1	0D
38674	103.429	104.26	105.91	0	1	1	1	0	0	1C
37332	107.147	108.00	109.72	0	0	1	1	0	0	0C
36051	110.954	111.84	113.62	0	1	1	0	1	1	1B
34831	114.84	115.76	117.60	0	0	1	0	1	1	0B
33672	118.793	119.74	121.64	0	1	1	0	1	0	1A
32513	123.028	124.01	125.98	0	0	1	0	1	0	0A
31415	127.328	128.35	130.38	0	1	1	0	0	1	19
30378	131.674	132.73	134.83	0	0	1	0	0	1	9
29280	136.612	137.70	139.89	0	1	1	0	0	0	18
28304	141.323	142.45	144.71	0	0	1	0	0	0	8
27389	146.044	147.21	149.55	0	1	0	1	1	1	17
26413	151.441	152.65	155.08	0	0	0	1	1	1	7
25498	156.875	158.13	160.64	0	1	0	1	1	0	16
24644	162.311	163.61	166.21	0	0	0	1	1	0	6
23851	167.708	169.05	171.73	0	1	0	1	0	1	15
22997	173.936	175.33	178.11	0	0	0	1	0	1	5
22265	179.654	181.09	183.97	0	1	0	1	0	0	14
21472	186.289	187.78	190.76	0	0	0	1	0	0	4
20740	192.864	194.41	197.49	0	1	0	0	1	1	13
19642	203.645	205.27	208.53	0	0	0	0	1	1	3
18971	210.848	212.53	215.91	0	1	0	0	1	0	12
18361	217.853	219.60	223.08	0	0	0	0	1	0	2
17751	225.339	227.14	230.75	0	1	0	0	0	1	11
17141	233.359	235.23	238.96	0	0	0	0	0	1	01
16531	241.97	243.91	247.78	0	1	0	0	0	0	10
15982	250.282	252.28	256.29	0	0	0	0	0	0	00

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830061.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

The EIA RS-220 specification divides the standard frequencies into three groups. They are tabulated below with the program codes used in MX-COM ICs:

Group A	
Freq	Code
67.0	3F
77.0	0F
88.5	0E
100.0	0D
107.2	0C
114.8	0B
123.0	0A
131.8	09
141.3	08
151.4	07
162.2	06
173.8	05
186.2	04
203.5	03
218.1	02
233.6	01
250.3	00

Group B	
Freq	Code
71.9	1F
82.5	1E
94.8	1D
103.5	1C
110.9	1B
118.8	1A
127.3	19
136.5	18
146.2	17
156.7	16
167.9	15
179.9	14
192.8	13
210.7	12
225.7	11
241.8	10

Group C	
Freq	Code
74.4	3E
79.7	3D
85.4	3C
91.5	3B
97.4	3A
69.3	39
206.5	38

Note that with the exception of the 67.0 Hz tone in Group A, the programming codes are in reverse sequential order in relation to the tone frequencies for each group. Again, with the exception of 67.0 Hz, also note that the first hexadecimal digit for Group A is 0, the first digit for Group B is 1, and the first digit for group C is 3.

For more general information about these ICs, see the MX-COM Product Handbook and the MX-COM MX165C, MX315A, MX365A, MX375, and MX465 Data Bulletins.

MX-COM does not test its CTCSS ICs (MX165C, MX315A, MX365A, MX375, and MX465) at crystal or clock frequencies other than the nominal frequency specified in the Product Handbook or Data Bulletin, and as such, makes no guarantee of the performance of the device when used with a non-specified crystal or clock frequency. MX-COM does not assume responsibility for the use of its ICs in the manner described in this application note in any circuit or product.

© 1997 MX•COM, INC. www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054 Doc. # 20830061.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA. All trademarks and service marks are held by their respective companies.

SWITCHED CAPACITOR INTERFACING

Anti-Aliasing and Smoothing Filters

1.0 Introduction

Switched capacitor networks (SCNs) are sampled data systems and therefore are governed by the principles of discrete time signal processing. In this context, "discrete time" means the signal is sampled prior to processing. However, the amplitude is continuous – unlike digital signal processing (DSP) systems where both amplitude and time are discrete.

VLSI technology (generally CMOS) has facilitated complete integration of SCNs on a single monolithic chip. Filters utilizing switched capacitor techniques (SCFs) are composed of switches, capacitors and opamps. Notice resistors are not mentioned. The resistors normally present in active filters are approximated by switched capacitors. By taking advantage of matching properties of CMOS capacitors, SCFs can be fabricated with low tolerance levels (less than 0.1%) and virtually any order.

The wireless and wireline telecom industries have made extensive use of SCFs. Even with the move towards digital technology and the ensuing popularity of DSP in the communications industry, SCNs are frequently employed where cost and power consumption are critical. SCNs generally have relatively high sampling rates (typically greater than 20 times the bandwidth of the interest) due to their discrete time nature, so aliasing and output smoothing must be addressed. Often a simple single pole filter (R-C network) suffices, but the location of these poles must be carefully thought out in the design process. The world is still analog.

The purpose of this paper is to address the need for anti-aliasing and smoothing filters for SCFs. First, the basics of sampling will be reviewed. The fundamentals of SCNs will follow this, and finally the design of antialiasing and smoothing filters for SCFs is addressed.

2.0 Sampling [3]

Before a continuous signal is processed by a discrete time filter it must first be sampled. Referring to Figure 1a, sampling is the process of instantaneously capturing the level of a continuous signal at some predetermined rate. This predetermined rate is the sampling frequency. As the sampling rate increases (Figure 1b) the sampled signal begins to approximate the original continuous signal.

© 1997 MX-COM, Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20830063.001

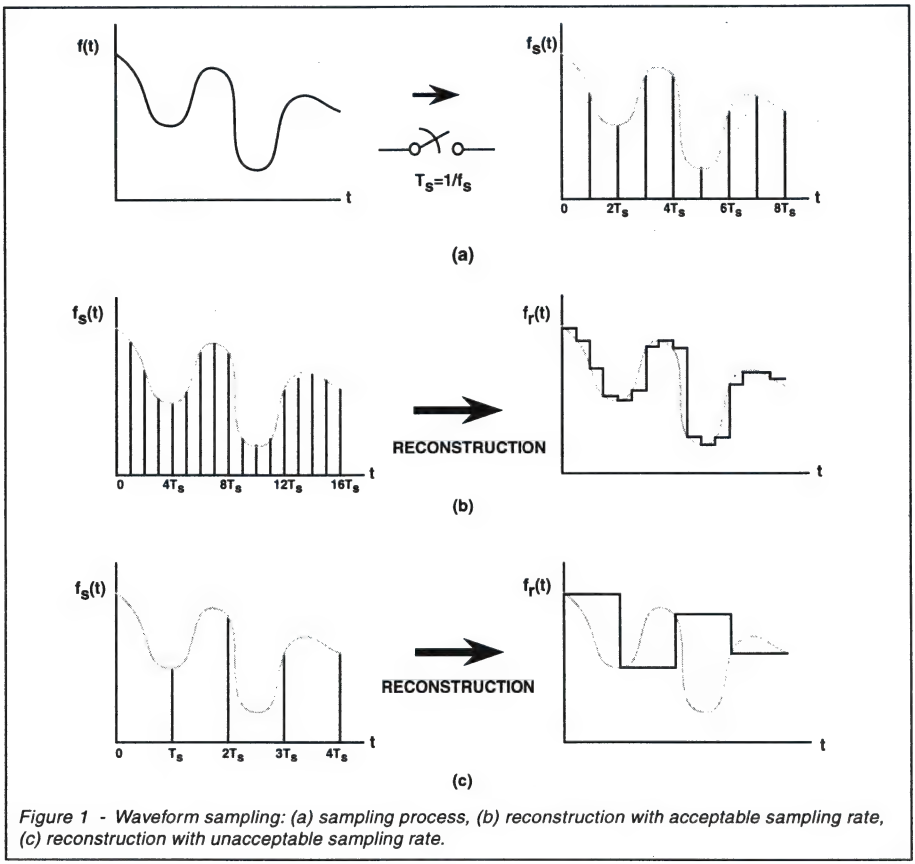


Figure 1 - Waveform sampling: (a) sampling process, (b) reconstruction with acceptable sampling rate, (c) reconstruction with unacceptable sampling rate.

On the other hand, as the sampling frequency decreases (Figure 1c) the samples move further apart in time, yielding a reconstructed signal that does not resemble the original. The limit on how far apart these samples can become without losing information is the basis for Shannon's sampling theorem.

Shannon's original work on sampling and information theory [3] stated the sampling theorem as:

> "If a function f(t) contains no frequencies higher than *f* cycles per second it is completely determined by giving its ordinates at a series of points spaced (1/2*f*) seconds apart."

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830063.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

A formal derivation is obtained by convolving the Fourier transform of the continuous signal with the Fourier transform of an infinite sequence of impulse functions.

$$F_S(\omega) = \frac{1}{2\pi}(F(\omega)*S(\omega)) \quad (1)$$

$$F_S(\omega) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F(x)S(\omega-x)dx \quad (2)$$

Where, $F_S(\omega)$ = sampled signal spectrum
$F(\omega)$ = original signal spectrum
$S(\omega)$ = spectrum for a sequence of impulses
ω = radian frequency ($2\pi f$).

The result of the convolution is the original signal spectrum repeated at multiples of the sampling frequency as shown in Figure 2. Notice that if the sampling frequency is less than twice the bandwidth of the original signal then the replica centered at the sampling frequency will overlap and distort the original. This undesirable phenomenon is aliasing. Aliasing will be avoided if,

$$f_S \geq 2B \quad (3)$$

Where, f_S= sampling frequency , Hz
B = bandwidth of original signal, Hz.

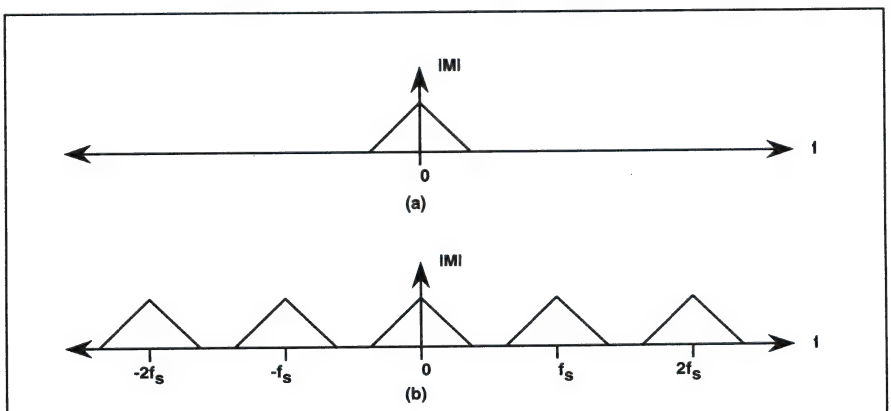


Figure 2 - Frequency Spectrum of (a) continuous time signal; (b) sampled signal

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830063.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

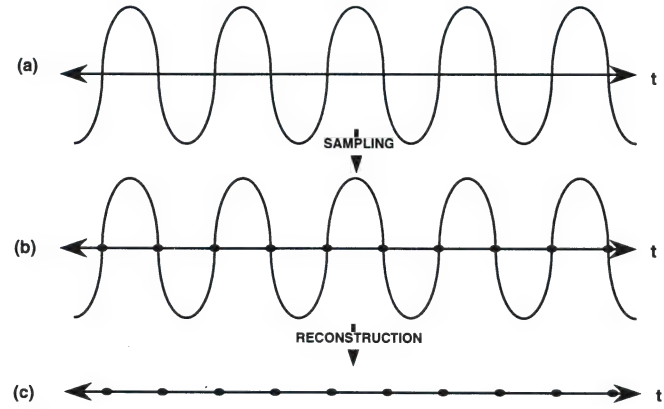


Figure 3 - Time domain representation of sampling at $f_S = 2B$; (a) continuous signal; (b) sampled signal; (c) reconstructed signal

Shannon's sampling theorem is mathematically sound although, in most cases, it is not practical to sample a signal at exactly twice its highest frequency component. Figure 3 shows a sinewave sampled at **2B** samples per second, where **B = 1/T** and **T** is the period of the sinewave. Notice the difference between the reconstructed wave shapes and the original unsampled signal. This type of error is not the result of aliasing, yet it could cause deceptive results. A mathematician might claim that there is no information in a continuous sinewave that never changes amplitude or frequency. This is a fact. However, if a signal is sampled at exactly **2B**, some of the original signal may be lost or distorted.

If the system designer is not concerned with the possibility of losing some of the original signal, and wanted to sample at **2B**, he or she would still be facing the problem of bandlimiting. Bandlimiting is necessary to avoid aliasing. Figure 4 shows the spectrum of a sampled signal. Notice that for f_S**=2B** the bandlimiting filter must have infinite attenuation at the frequency **B**. A filter that matches this requirement is physically unrealizable.

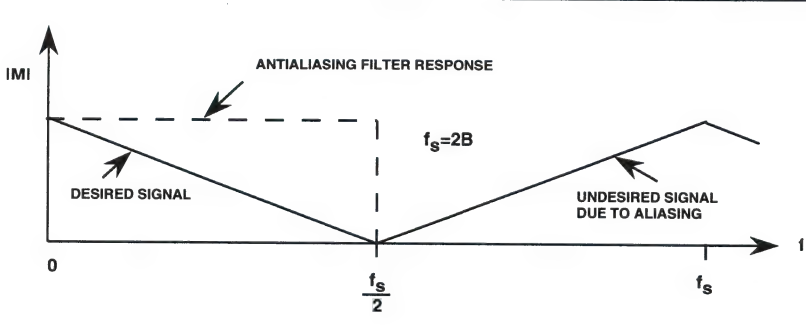


Figure 4 - Antialiasing filter required for sampling at exactly 2B

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830063.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

3.0 SCN Concepts [1]

A single pole active filter (inverting integrator) is shown in Figure 5. This circuit is the primary building block for most active filters.

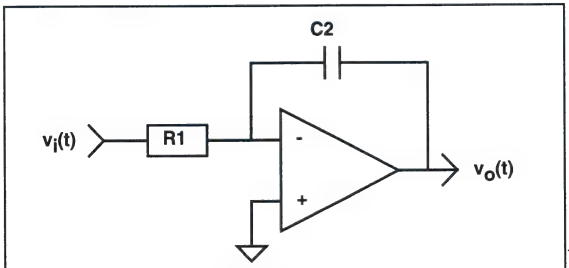


Figure 5 - Active R-C integrator.

The output is defined by

$$v_o(t) = -\frac{1}{RC}\int_0^t v_i(\tau)\,d\tau \qquad (4)$$

Hence, the output is an integrated version of the input, scaled by **-1/RC**. The pole frequency is determined by the value of **R** and **C**

$$f_p = \frac{1}{2\pi RC} \qquad (5)$$

For a pole frequency of 3000Hz, (5) implies RC=53.05μs. A possible implementation, selecting C=10pf (relatively large capacitor for CMOS technology), requires R=5.305MΩ. A monolithic resistor of this value would consume excessive amounts of silicon and is subject to significant variation with process and temperature. Integrated capacitors are also subject to variation with process and temperature. In addition, capacitor variations are independent of resistor variations.

A more practical realization is shown in Figure 6.

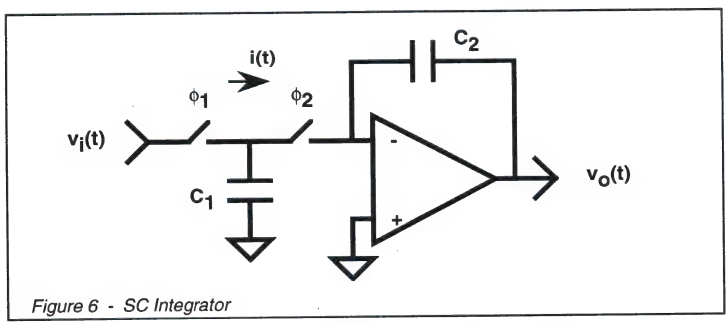


Figure 6 - SC Integrator

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830063.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Notice **R** is replaced by a capacitor and two switches. The function of the resistor is now approximated by transferring charge from vi(t) to the inverting input of the opamp at intervals determined by clocks $\phi 1$ and $\phi 2$. To ensure complete charge transfer $\phi 1$ and $\phi 2$ must not overlap as shown in Figure 7.

An approximate analysis of Figure 6 reveals the average current through the switches is

$$i = \frac{\Delta q}{T} = \frac{C_1}{T}(v_i - v_1) \quad (6)$$

or

$$i = \frac{1}{R}(v_i - v_1) \quad (7)$$

Where, $R = T/C_1$

Looking back at the previous example for a pole frequency of 3000Hz, using $T = 10\mu s$ (f_{clk}=100kHz), yields C_1=1.885 pf. Hence, the integrator can be realized with two capacitors that will track with process and temperature. No longer is the absolute value of the capacitors important, only their ratio.

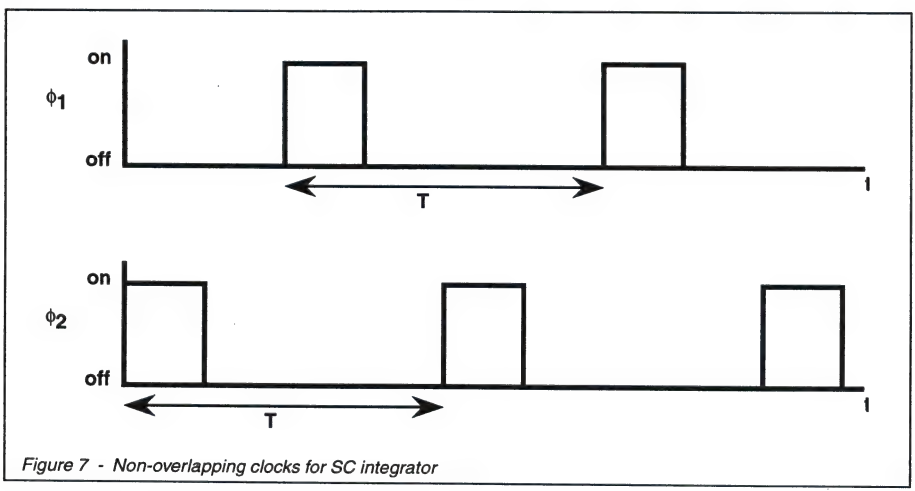


Figure 7 - Non-overlapping clocks for SC integrator

4.0 Anti-aliasing and Smoothing Filters for SCNs [2]

SCFs approximate active-RC filters by replacing resistors with switched capacitors. As the clock frequency (sampling rate) tends towards infinity the SCF becomes equivalent to the continuous time filter. In other words, higher clock frequency yields a better approximation of the desired response. Also, higher clock frequency lessens the requirements of the anti-aliasing filter (AAF) and smoothing filter (SMF). However, there are upper limits on clock frequency. Although SCFs have been implemented with clock frequencies greater than 1MHz, typical telecom filters (BW less than 10kHz) are clocked at or below 250kHz.

One factor which opposes higher clock frequencies is large capacitor ratios. Referring to the example in section 3.0,

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830063.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

using 1MHz in place of 100kHz, C_1 becomes 0.1885 pf. The ratio between C_1 and C_2 is now 53.05 where it was 5.305. Large capacitor ratios consume more silicon area and are more sensitive to process and temperature variations. Hence, the final sampling rate is a compromise between SCF implementation complexity and SMF/AAF requirements.

SMFs and AAFs can be integrated, but they are subject to the same problems associated with the continuous time RC integrator discussed in section 3.0 and are generally implemented externally. In some cases, where input and output signals are band limited externally, additional circuitry for AAFs and SMFs is not required. A block diagram of a typical SCF system, including AAF and SMF is shown in Figure 8.

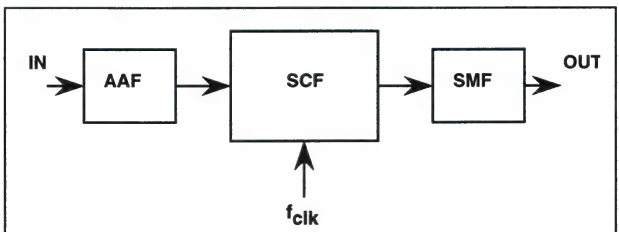


Figure 8 - SCF system with AAF and SMF

To determine AAF and SMF requirements the system designer must know the sampling frequency (f_{clk}) and the bandwidth (BW) or cutoff frequency (f_{co}) of the SCF. For discussion purposes, assume f_{clk}=100kHz and f_{co}=5kHz. Recall from section 2.0, if any signal energy is present at the input, with frequency f_s greater than $1/2f_{clk}$, it will be aliased to $f_{clk} - f_s$. Hence, an input with f_s=99kHz will be aliased to 1kHz. This aliased signal will appear as noise in the passband of the SCF. To eliminate or reduce the effect of this noise the AAF must band limit the input signal to $f_{clk} - f_{co}$ (see Figure 9).

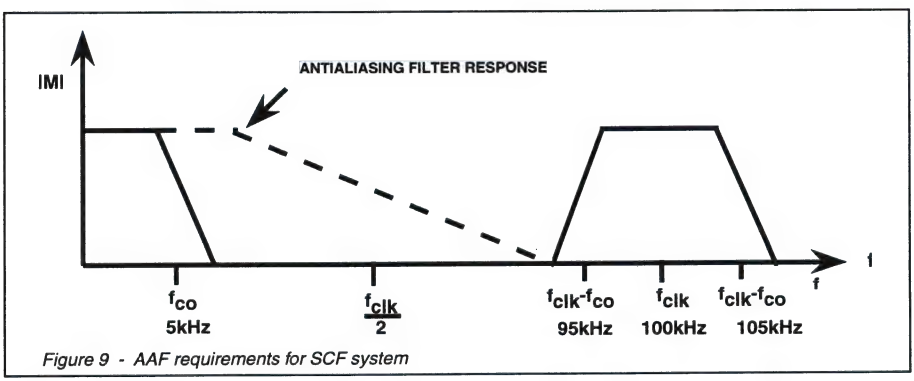


Figure 9 - AAF requirements for SCF system

To obtain 20 dB suppression of aliased noise the minimum requirement for the AAF is a first order section (single pole) with it's cutoff frequency set to 9.5kHz. (20 dB/decade/pole). Placing the pole at 9.5kHz minimizes the effect on the SCF passband response. To obtain further suppression more poles are necessary.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830063.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

The single pole AAF can be implemented with a simple RC at the input to the SCF. The values for can be arrived at by using

$$RC = \frac{1}{2\pi f_p} \quad (8)$$

where, f_p = pole frequency.

For the AAF response depicted in Figure 9, **RC** = 16.75ms. Setting **C** = 0.1µf yields **R** = 168Ω. The simple RC network should be used with caution–capacitive loading can cause stability problems. Also, the value of the resistor should be insignificant compared to the SCF input impedance.

A superior solution makes use of an additional opamp forming a damped integrator (see Figure 10). Often this opamp will be available on the SCF chip.

The complete network, including R1, C1, R2 and C2, forms a bandpass filter with a frequency response characteristic as shown in Figure 11.

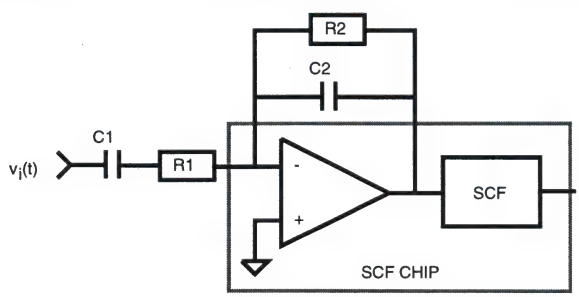


Figure 10 - Active RC AAF

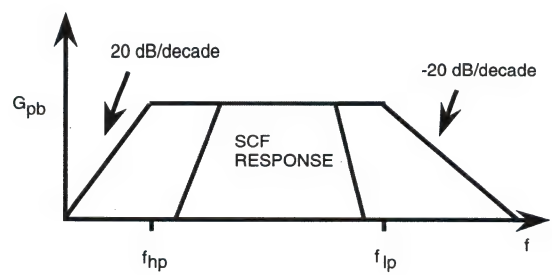


Figure 11 - AAF frequency response

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830063.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

The highpass cutoff (f_{hp}) and lowpass cutoff (f_{lp}) are determined by

$$f_{hp} = \frac{1}{2\pi R_1 C_1} \quad (9)$$

and

$$f_{lp} = \frac{1}{2\pi R_2 C_2} \quad (10)$$

The passband gain is set by

$$G_{pb} = R_2/R_1 \quad (11)$$

C_1 is not required if the input signal is biased properly (SCF internal bias = external bias).

To meet the AAF requirements shown in figure 9 (assuming unity passband gain, f_{lp} = 9.5kHz and f_{hp} = 100 Hz) R_1 = R_2 = 100KΩ, C_2 = 168pf and C_1 = 0.0159μf.

SMF requirements are similar to those of the AAF. The SCF output is a sampled signal and therefore contains replicas of the SCF response at multiples of the sampling frequency. If left unfiltered these replicas appear as high frequency (clock) noise. In some cases this is tolerable. However, in systems where minimum noise is critical the SMF is required.

5.0 Conclusion

Switched capacitor filters are sampled data systems and hence require anti-aliasing filters at their inputs and smoothing filters at their outputs. The simplest form (and often sufficient) of these filters is the single pole RC network. Other forms such as active RC networks and higher order filters can yield distinct benefits. In any case, application of switched capacitor filters must be viewed at the system level in order to realize optimum performance.

REFERENCES

[1] R. Gregorian, K. W. Martin, and G. C. Temes, "Switched-Capacitor Circuit Design," Proceedings of the IEEE, pp. 941-966, August 1983.

[2] L. P. Huelsman and P. E. Allen, Introduction to the Theory and Design of Active Filters, McGraw-Hill, New York, 1980.

[3] A. B. Jerri, "The Shannon Sampling Theorem - Its Various Extensions and Applications: A Tutorial Review," Proceedings of the IEEE, pp. 1565-1596, November 1977.

© 1997 MX-COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830063.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX-COM Inversion Security Devices

Split-Band Scrambling Furnishes Voice Security

Voice scrambling offers tactical security for radio dispatch communications. It takes so long, even for a dedicated eavesdropper, to unscramble your transmissions that the information would be worthless by then.

By Steve Kelley and Hank Wallace

Unwanted consequences of third-party radio communications eavesdropping include foiled drug busts, unsolved burglaries and pirated business opportunities. Some mobile radio users employ voice privacy and voice security devices to scramble their communications. Most users who need voice security continue to communicate in the clear, however, for several reasons:

(1) Cost --They cannot justify the captial expense.

(2) Technology -- The poor quality of recovered audio and the radio range reduction common to many voice security systems discourage their use.

(3) Availability -- Two principal scrambling alternatives, frequency inversion and digital encryption, are not suitable for many applications. Frequency inversion offers privacy but not security; digital encryption offers high security but with a high price tag.

Semiconductor technology advances have reduced costs and improved the quality of voice security products. Variable Split-Band (VSB) scrambling has become economical because of such advances.

How it works

Filters separate the voice band (400Hz to 2700Hz) into a pair of subbands (32 pairs are possible). (See Figures 1A, 1B and 1C.) A mixer fed with a carrier signal inverts the subbands; a summing amplifier recombines them. Ordinary radio transceivers transmit the resulting variable split-band-

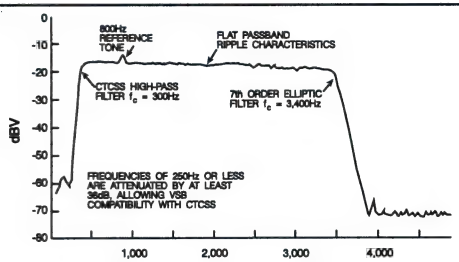


Figure 1A - Audio output of VSB filter array IC in clear mode

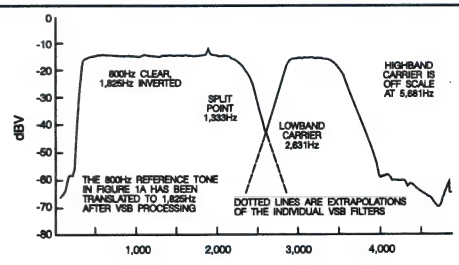


Figure 1B - Audio output of VSB filter array IC in "scramble" mode with split point at 2,333Hz.

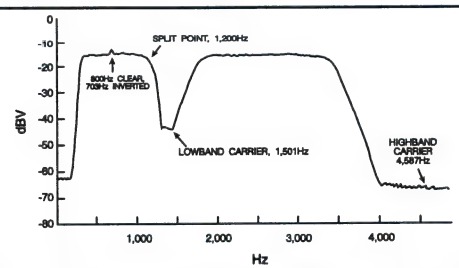


Figure 1C - Audio output of VSB filter array IC in "scramble" mode with split point at 1,200Hz.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830062.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

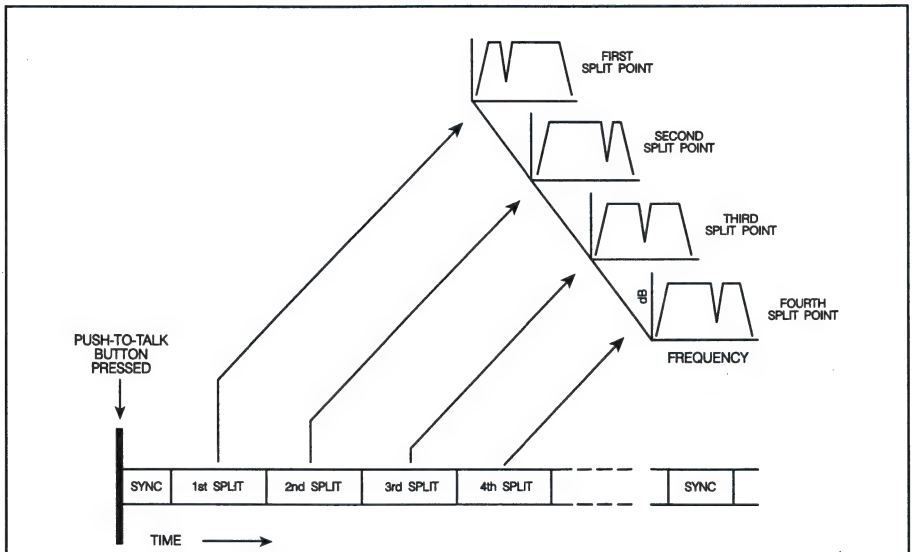


Figure 2 - The effect of rolling code split points on the transmitted radio spectrum

scrambled output via an ordinary radio communications channel.

Microprocessor outputs control the split point (the frequency at which the voice band is subdivided) and change it from 4 to 60 times per second. Figure 2 reveals the "rolling code" nature of VSB scrambling. One of more than 65,000 unique user-programmable code keys initializes the pseudorandom sequence of split points. User programming commands the split point's rate of change, or "hop rate," to vary pseudorandomly or in a fixed fashion.

Filtering Accuracy

Optimum recovered audio quality depends upon highly accurate voice filtering. Two pairs of 7th order, switched-capacitor, elliptic filters in the VSB filter array integrated circuit (IC, on-chip) accomplish all the filtering (See Figure 3).

The transceiver's mic. audio pre-amplifier or receiver audio demodulator output feeds the VSB filter array IC's highband and lowband inputs. Within the IC, audio from each subband passes through a lowpass filter, a frequency inverter and another lowpass filter. A summing amplifier recombines the subbands. The chip includes a highpass filter that permits VSB scrambling to be used with continuous-tone controlled squelch systems (CTCSS) and other sub-audible signaling schemes.

On-chip programmable dividers with a 5-bit logic address control the 32 split points and their highband and lowband carrier frequencies. The VSB microprocessor uses the 5-bit address to generate a rapidly changing sequence of split points. Table 1 shows the exact relationship between each split point and its associated carrier frequencies.

Microprocessor Control

The VSB microprocessor performs scramble system control functions, including:

- generation of split-point sequences
- control of system synchronization
- monitoring of the push-to-talk (PTT) line
- code key selection
- code key loading
- selection of the secure or clear mode.

The microprocessor generates pseudorandom strings of split points initialized by one of four user-programmable code keys. Non-volatile, electrically erasable, programmable read-only memory (EEPROM) stores the code keys and other user-programmable system information (see Figure 4).

To decode a rolling, VSB-scrambled message properly, the receiver(s) must "hop" in unison with the transmitter from one split point to the next. A continuous synchronization scheme accomplishes this task. The scheme transmits 1200-baud minimum-shift keyed (MSK) data bursts every three seconds. Authorized parties can descramble transmissions even if the beginning of the message is missed, preserving mobile radio's inherent "late joining" feature.

In the absence of valid synchronization bursts, receivers

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830062.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

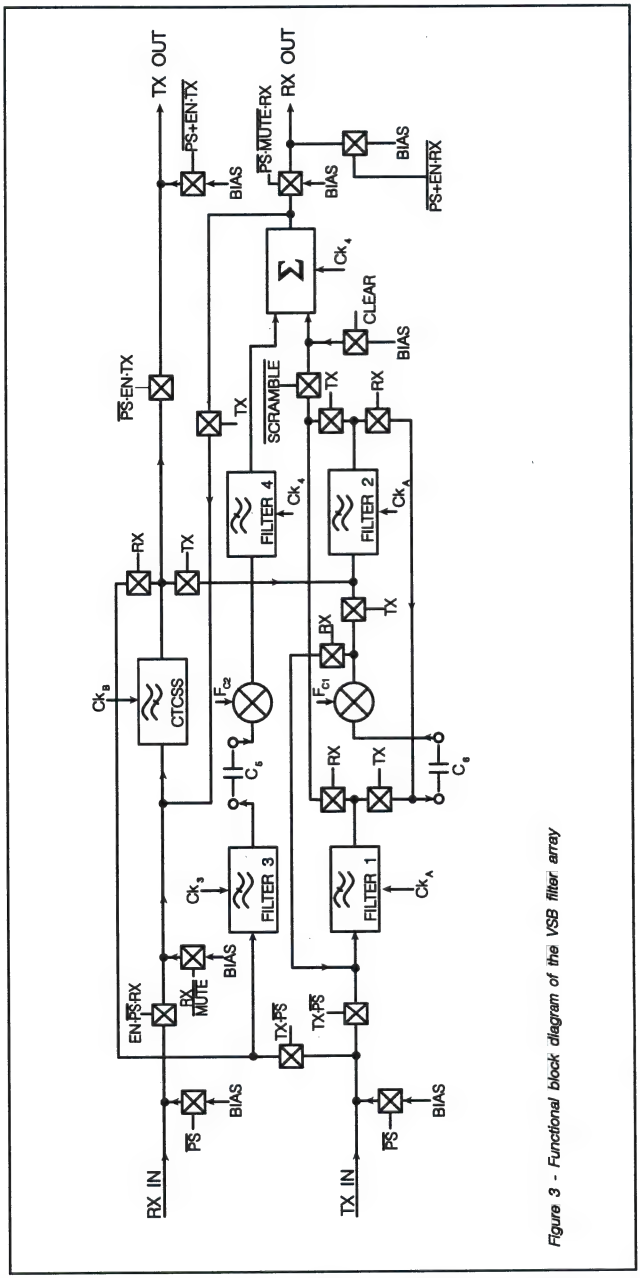


Figure 3 - Functional block diagram of the VSB filter array

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830062.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

ROM Address A_4-A_0	Split Point Hz	Low Band Carrier, Hz f_{c1}	High Band Carrier, Hz f_{c2}	ROM Address A_4-A_0	Split Point Hz	Low Band Carrier, Hz f_{c1}	High Band Carrier, Hz f_{c2}
00000	2800	3105	6172	10000	1135	1436	4504
00001	2625	2923	6024	10001	1050	1351	4424
00010	2470	2777	5813	10010	976	1278	4347
00011	2333	2631	5681	10011	913	1213	4310
00100	2210	2512	5555	10100	857	1157	4273
00101	2100	2403	5494	10101	792	1094	4166
00110	2000	2304	5376	10110	736	1037	4132
00111	1909	2212	5263	10111	688	988	4065
01000	1826	2127	5208	11000	636	936	4032
01001	1750	2049	5102	11001	591	891	3968
01010	1680	1984	5050	11010	552	853	3937
01011	1555	1858	4950	11011	512	813	3906
01100	1448	1748	4807	11100	471	772	3846
01101	1354	1655	4716	11101	428	728	3816
01110	1272	1572	4629	11110	388	688	3787
01111	1200	1501	4587	11111	350	650	3731

Table 1 - ROM Address Programming

revert to clear mode. The automatic reversion to clear mode ("clear voice override") makes scrambling easier to use in systems that include some radios not equipped for scrambling.

Only transmitting VSB units generate synchronizing data bursts, so the system resynchronizes at the transmitting station's command. Transceivers automatically transmit 80ms data bursts every three seconds after beginning a transmission. Each data burst includes:

Unit System Address-- Identifies the scrambler as part of a designated group.

Code Key File Number-- Identifies which of the four stored code keys to use.

Time Of Day -- When mixed with the secret code key, which never is transmitted, time of day tells the receiver on which part of the 50-hour long split-point sequence to begin "hopping."

Synchronization Cue -- Tells the receiver when to change split points.

In the standby mode, VSB scrambling units scan continuously for incoming synchronization bursts that have the proper system address and file number. After receiving one such data burst, a VSB unit uses the time-of-day signal and synchronization cue to descramble the incoming message properly. Unless the receiving unit receives the proper address and file combination, it processes incoming transmissions as though they were unscrambled.

A robust error-detection algorithm, based on the British MPT 1317 signaling protocol, minimizes synchronization errors. As a safeguard, VSB scramblers retain synchronization even if a single synchronization burst is missed. If the scrambler misses two synchronization bursts in a row, the system reverts to the standby mode and scans once again

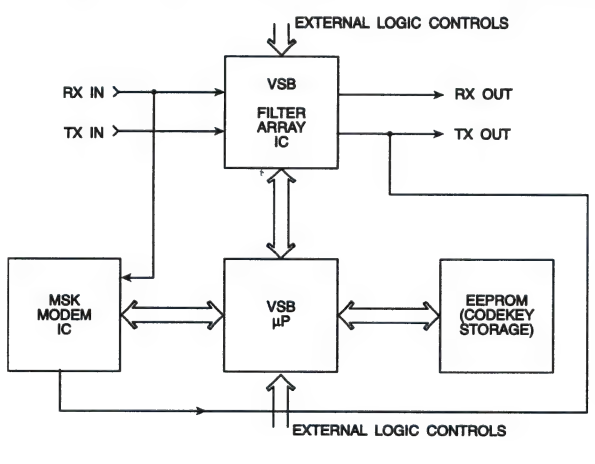


Figure 4 - Block diagram of VSB scrambler mode

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830062.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Voice Security Market

Potential markets for economical voice security products include:

- Taxi
- Towtruck
- Marine and other dispatch operations whose managers previously have been unsatisfied with the price or performance of voice security products.
- Municipal law enforcement agencies that lack voice security systems or that are committed to a digital encryption system that is too expensive to install into every radio in the organization.

for synchronization burst data.

Minimum-shift keyed modulation offers excellent narrowband transmission properties and superior noise performance. With MSK modulation, voice intelligibility and synchronization are lost more or less concurrently in fringe reception areas and without an appreciable loss in radio range.

An eavesdropper monitoring a VSB-scrambled transmission hears an unintelligible jumble, interrupted by bursts of digital "static" every three seconds. Consider VSB scrambling's security features:

(1) The split-point sequence permutation, which is based on a mixture of the secret code key and the time-of-day signal, changes automatically every three seconds. The code knowledge that may be obtained from one descrambled three-second sequence cannot be applied to descramble subsequent segments because they are based on different sets of pseudorandom permutations.

(2) The split-point "hop rate" may be varied pseudorandomly, further complicating the task.

(3) Each VSB-equipped radio can transmit and receive four programmed code keys, and VSB systems can accomodate as many as 16 unique code keys. Thus, a unit can transmit on one code key and receive on another.

(4) The code keys may be changed at any time. They never are transmitted. They cannot be deduced by visual or mechanical means.

Given these security features, how difficult is it to descramble such a garbled transmission? According to two

VSB Scrambling Multiple Codekey Capability

Within a VSB scrambling network, up to 16 codekeys can be allocated. Four of the sixteen codekeys can be installed per radio. As illustrated below, this capability can create interesting subgroup segregation possibilities:

Scenario: Public safety departments of medium-sized cities need interagency, as well as private, intradepartmental secure communications.

Solution: A VSB Scrambling codekey allocation scheme allocates seven codekeys (A-G), four to the police force, and two each to the fire department, ambulance service, and detective unit.

USER SUBGROUP	INSTALLED CODEKEYS	COMMUNICATIONS CAPABILITY
1) HQ/Supv.	All	Monitor all channels
2) Police	A	Intradepartment only
	B	Police and fire
	C	Police and detectives
	D	Police and ambulance
3) Fire	B	Police and fire
	E	Intradepartment only
4) Detectives	C	Police and detectives
	F	Detectives only
5) Ambulance	D	Police and ambulance
	G	Intrasquad, ambulance and hospital

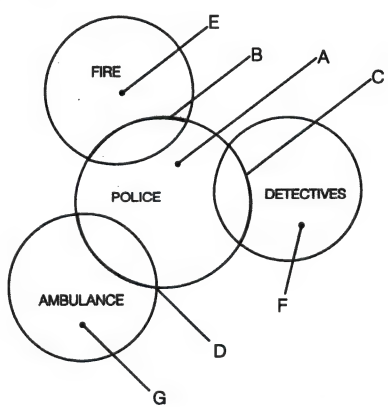


Figure 5 - Multiple codekeys extend subgroup segregation possibilities in a medium-sized city's public safety department

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830062.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

experts, it is not easy.

According to Michael Washvill, a voice and data security specialist with a federal agency, "VSB scrambling can be broken, but not in real time. The only practical attack is through trial and error. The scrambled speech must first be recorded, then divided into finite time segments according to the hop rate. Each segment is processed through a variety of split point combinations until clear speech results."

A TRW systems engineer and former U.S. Department of Defense employee, Jim Walker, concurs: "The 'brute force' method of trial and error is the only way to break VSB-scrambled speech. Assuming that the 'bad guys' have a stolen VSB unit and no prior knowledge of the code key or code keys, 50 to 100 minutes of dedicated effort are required to descramble one minute of VSB-scrambled speech. A rule of thumb is 60:1 'grunt time to clear speech time'."

Walker continued, "For most eavesdroppers, the potential rewards do not justify the time and effort. Two additional factors come into play. First, by the time the information is decrypted, will it still be of any use? Second, what percentage of the descrambled radio traffic will be of value?"

Given the time and perseverance required to break a VSB-scrambled transmission, two alternatives become much more attractive to those who want to eavesdrop: Steal a VSB-equipped radio or bribe someone who knows the codekey. Strict code key management procedures reduce system vulnerability to these attack methods.

To reduce the possibility of bribery, restrict code key knowledge to one person. To guard against stolen VSB units, change system code keys on a regular basis by using the VSB keyloader.

The keyfoader is a portable tool that reprograms VSB-equipped radios in the field. A technician connects the keyloader's data-loading cable to a VSB-equipped radio and presses the load button to install as many as four new codekeys into each radio. Only the person with codekey management authority can program the keyloader or read its contents.

Tactical vs. Strategic

Voice security requirements can be divided into two broad categories: tactical and strategic. Tactical applications are those in which the secrecy of the message is time-dependent, such as battlefield tactical communications, most municipal police communications and nearly all dispatch communications. The tactical message retains its value for one or two hours at most. VSB scrambling serves tactical security requirements.

James Bramford, in his book *The Puzzle Palace*, defines strategic communications as "the high-level diplomatic, commercial and military communications that might give away a nation's foreign policy venture, where and with whom it was doing business, or what new weapons were being developed over the next few years." Today's strategic applications demand some form of digital encryption.

In addition to the message security afforded by digital encryption or VSB scrambling, transmission security can be assured through spread-spectrum techniques, such as frequency hopping, which render the radio signal both undetectable and immune to jamming.

Most mobile radio users have tactical voice security requirements. For these applications, VSB scrambling offers a practical, economical alternative to digital encryption systems. VSB scrambling requires no modification of the installed communications network. It has little or no impact on radio range.

As dealers and users become more comfortable with VSB and other new scrambling technologies, foiled drug busts, unsolved burglaries and pirated business opportunities resulting from unauthorized eavesdropping will become things of the past.

MX•COM, INC.

Reprinted with permission from the May 1988 issue of Mobile Radio Technology. Copyright 1988, Intertec Publishing Corp., Overland Park, KS. All rights reserved.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830062.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

MX•COM, INC.

Digitally-integrated Baseband Subsystem

System Overview Including C-BUS Applications

C-BUS COMPATIBLE

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830060.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.

Digitally-integrated Baseband Sub-system (DBS800) System Overview

MX802 • MX803A • MX805A • MX806A • MX809

This family of audio processing and signaling devices is designed for use in two-way mobile or trunked radio. While supporting all internationally mandated or system-specific requirements for processing and signaling, DBS 800 also includes many high-level functions which offer a flexible, low-cost route to the "Added Value" opportunities in the LMR market.

DBS 800 was created with the mobile radio hardware and software development engineer in mind. All IC's were designed as peripherals to the radio's host microprocessor. They require a minimum amount of control software. A single address and data hardware bus (C-BUS) is used on all IC's for easy connections to the host microprocessor and minimum track layout.

To support the product's functions there is a development kit including all DBS 800 integrated circuits, a support microprocessor and software. It allows evaluation, demonstration and software development to be completed in a fraction of the time normally required.

Features

Complete audio processing (CEPT, EIA, etc.)

Universal Signaling:
- *SelCall (CCIR, ZVEI I, II, III, EEA, etc.)*
- *CTCSS (EIA, EEA)*
- *DPL™, Digital Coded Squelch (DCS)*
- *Digital Selcall, 1200 Baud MSK (MPT 1317/1327)*
- *DTMF encode*
- *LTR™, NRZ Data*
- *2-Tone, Special Tones*

Data Communications with data storage and buffering

Voice/Data Scrambling

Voice Management
- *Voice storage, Mailbox, delay, busy buffer, alarms and status -- Reduced airtime usage -- Increased spectrum efficiency -- VOX/Handsfree operation*

System Management
- *Over-air programming/re-configuration and cloning -- Call billing/monitoring/blocking -- TX time-out/ selective lockout -- Repeater access/control -- Direct control of all system radio units*

ANI (Automatic Number Identification)

Half-duplex repeater

Common Control and Data Bus ("C-BUS")

Hardware Development Kit

Software Support:
- *Evaluation - Demonstration - Development*

Electronic digital trimming and volume control

Adaptive compensation for non-linear and temperature effects

Two-Point Modulation for trunked/scanning schemes

Fully automated test/alignment/servicing

Self-test mode

Single hardware design approach
- *Software reconfigurable*

Full integration reduces PCB area

Greatly reduced development time

Multi-level powerdown modes

DPL™ is the registered trademark of Motorola, Inc. LTR™ is the registered trademark of E.F. Johnson Co.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830060.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Benefits

- DBS 800 is compatible with most Selcall schemes such as DTMF, 5/6-Tone, 2-Tone and MSK. It is also compatible with Sub-Audio CTCSS, DCS and LTR™.
- Allows advanced signaling: Digital Selcall, ANI, overair re-configuration, cloning, channel dependent signaling.
- A single design concept can be used for all models of mobile radio with different features or market destinations. Software is reconfigurable.
- One microprocessor is required to control all radio functions. DBS 800 devices contain additional hardware to minimize software overhead.
- Digitally controlled trimmers allow for "adaptive adjustment" of non-linear VCO conversion gain and temperature effects. This allows use of cheaper, lower-tolerance components.
- Non-predictive decoding of signaling devices gives total design flexibility.
- Smaller, lighter equipment design possible, e.g. handhelds.
- Non-predictive decoding offers features such as recognition and identification of own repeater CTCSS tone, multiple group call, etc.
- Voice management features voice security, voice mailbox, voice status, voice alarm, and voice buffering when a channel busy condition exists.
- For data communications, there is the ability to connect directly to mobile radio with no external interface, laptop PC's, printers, etc. RS232 interface or others are possible. Data storage and security are software dependent.
- Inventory is simplified by using the standard DBS 800 chip set.
- Radios can be calibrated and tested when completely assembled by using a single external audio/data/RF connection.
- Self test modes with audible/visual alert outputs.
- Simple field test unit can be used to test or reconfigure radios incorporating DBS 800.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830060.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

DBS 800 System Introduction

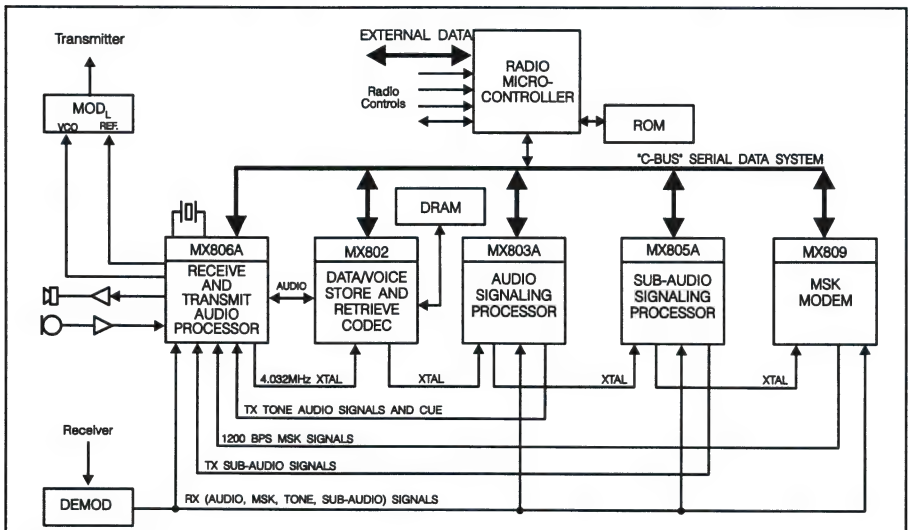


Figure 1 - DBS 800 Audio System

DBS800

The Digitally-Integrated Baseband Sub-system (DBS 800) is a family of low-power CMOS integrated circuits which provide a comprehensive range of audio processing and signaling functions for use within two-way radio systems.

Each IC can be used as part of the complete DBS 800 audio system, or as a "stand alone." The system and ICs are partitioned in such a way that radio designers can easily select the device(s) appropriate to their needs.

DBS800 ICs currently available are:

- **MX802 DVSR Codec**
  This is a Continuously Variable Slope Delta Modulation (CVSD) speech encoder and decoder with the ability to store and retrieve voice and data within attached external Dynamic Random Access Memory (DRAM) using an on-chip DRAM controller.

- **MX803A Audio Signaling Processor**
  This provides an inband tone signaling ability to LMR Systems.

- **MX805A Sub-Audio Signaling Processor**
  This provides a sub-audio and digital signaling (NRZ) ability to LMR Systems.

- **MX806A LMR Audio Processor**
  This is a half-duplex audio processor providing all DBS 800 system audio signal conditioning and filtering capabilities for the system transmit and receive paths.

- **MX809 MSK Modem**
  This is an intelligent, half-duplex 1200 baud MSK/FFSK Modem with a software programmable byte-synchronization system and checksum generation and checking.

Control of all DBS 800 ICs is by "C-BUS," a simple hardware and software system for the two-way transmission of commands and data between a microcontroller and the ICs.

C-BUS may be used with any microcontroller and allows the BUS data rate to be determined solely by the microcontroller. Control may be achieved by either the radio's microcontroller or a separate microcontroller dedicated to the purpose.

This section provides information on DBS 800 IC analog interconnections, including recommendations on application-specific gain and mixing components. It also provides C-BUS hardware and software information, including a complete list of address allocations and software commands.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830060.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

System Audio Interconnections

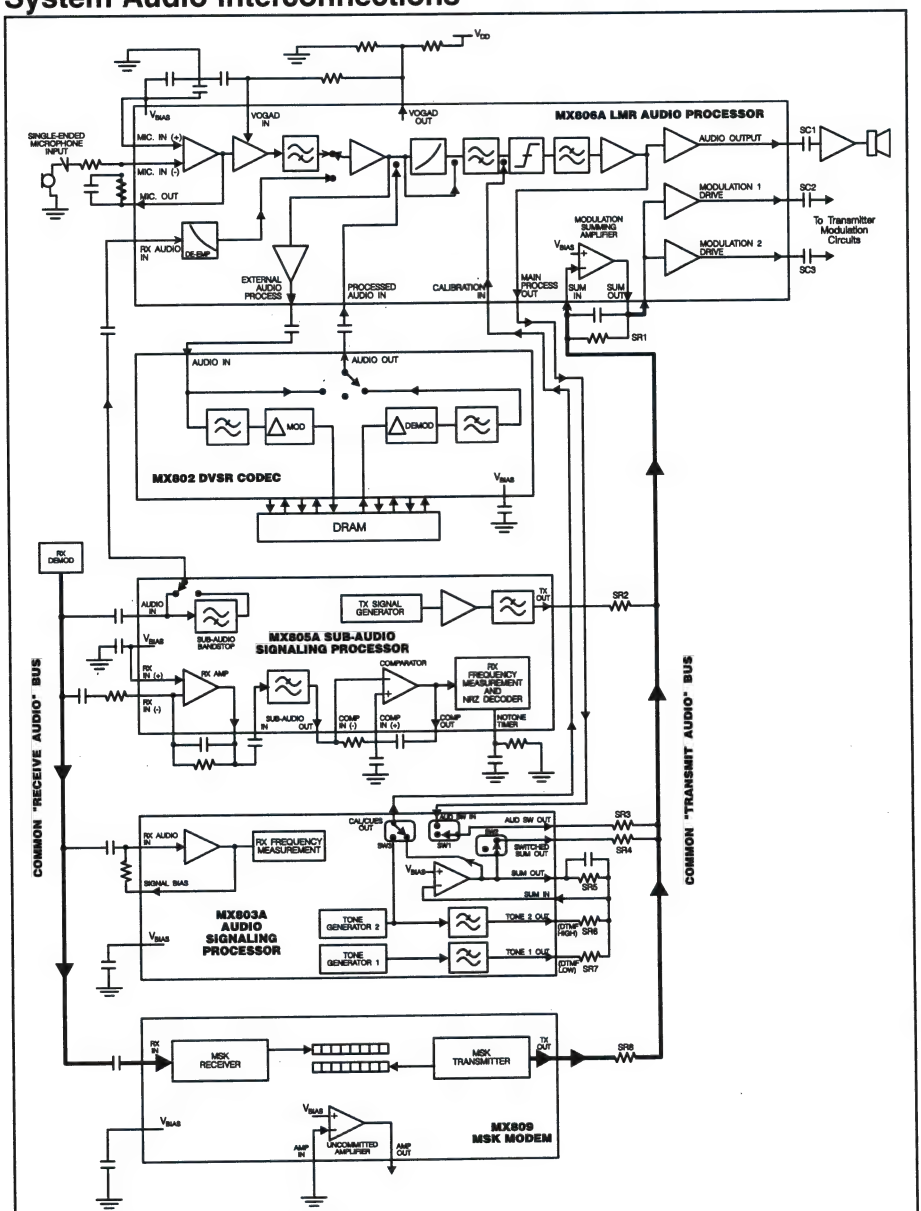


Figure 2 - System Audio Interconnections

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
All trademarks and service marks are held by their respective companies.
Doc. # 20830060.001

System Audio Interconnections

Figure 2 is an example of DBS 800 IC transmit and receive audio paths and interconnections. External components shown are those recommended in the individual Data Bulletins. Components identified by an "S" are illustrated as system components, which means that they are calculated to perform a specific function within the system. Table 1 shows recommended system component values and notes on their calculation.

System Component	Recommended Value	Notes - *(refer to Figure 2)*
SC_1 SC_2 SC_3	See Notes	These modulation drive coupling component values should be chosen with respect to the operational audio requirements and the radio's input specifications.
SR_1	100kΩ	The feedback resistor of the MX806A modulation summing amplifier. This amplifier satisfies the input gain and matching requirements of the remaining DBS 800 devices.
SR_2	1.0MΩ	Configured in conjunction with SR_1 to present a sub-audio signal content of -20.0dB to the modulator.
SR_3 SR_4	100kΩ 100kΩ	Configured in conjunction with SR_1 to present an audio signal level of 0dB to the modulator.
SR_5	100kΩ	The feedback resistor of the MX803A summing amplifier. This amplifier regulates the signal level output of Tone Generators 1 and 2, which in turn are to the Transmit Audio BUS by switch 2 and SR_4.
SR_6 SR_7	62.0kΩ 122kΩ	Configured in conjunction with SR5 to produce a 3.0dB tone-differential (twist) when the MX803A is used as a DTMF decoder. For selcall applications different output levels may be required, or the signal level from Tone 1 may be attenuated by the MX806A modulator drivers.
SR_8	100kΩ	Configured in conjunction with SR_1 to present an audio signal level of 0dB to the modulator.

Table 1 - Recommended System Component Values

MX803A Sub-Audio Signaling Processor

The audio switch (SW1) is used in this example application to allow interruption of the transmitter modulation path if it is required to provide a Calibration tone from the tone generator to the loudspeaker.

Xtal/Clock Frequencies

All DBS 800 ICs will operate with Xtal/Clock frequencies between 4.00 MHz and 4.10MHz. When considering a common Xtal/Clock frequency for all DBS 800 ICs in a system, it should be noted that:

a) A 4.032 MHz Xtal/Clock input will produce an accurate 1200 bps rate in the MX809 MSK Modem.
b) A 4.096 MHz Xtal/Clock input will generate an accurate 16kbps and 32kbps sampling clock rate in the MX802 DVSR Codec.
c) Driving all DBS 800 IC clock generators from a single Xtal/clock source prevents possible "beat-frequencies" and is therefore preferable.

DBS 800 IC audio frequency responses and internal sampling clock rates vary with respect to Xtal/Clock frequency (see Table 3).

Unused Pins

To improve screening and reduce noise levels around DBS 800 ICs, it is recommended that any unused pins are connected to VSS. This includes inputs to on-chip amplifiers and switches if not used within an application.

MX806A LMR Audio Processor

This is the audio terminal of any DBS 800 "core" audio installation. To demonstrate the versatility of the MX806A microphone input stage, Figure 2 shows the microphone input components in a single-ended configuration, with Figure 2 in the MX806A Data Bulletin showing a differential input configuration. Relevant component values are the same for both applications.

DBS 800 System Audio Level References

Table 2 gives a guide to the relevant signal levels used in the DBS 800 system.

Signal Level (dB)	Amplitude (mVrms)	TX Deviation (%)
-30.0	9.7	
-20.0	30.8	
-15.5	51.3	10
-9.6	102	20
-6.0	154	30
-3.5	205	40
-1.6	256	50
0	308	60
1.3	359	70
2.5	410	80
3.5	462	90
4.4	513	100

Table 2 - Audio Signal Levels

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830060.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

"C-BUS" Controlling System

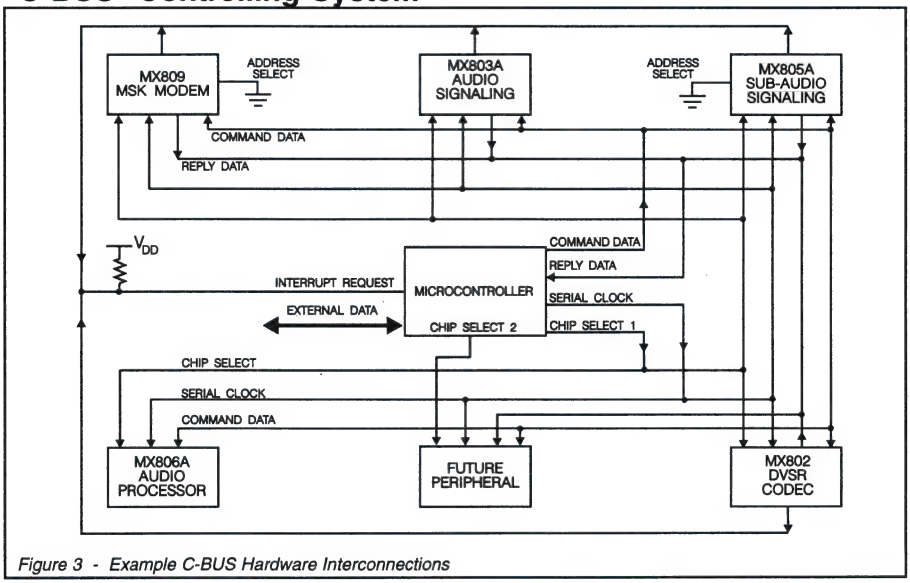


Figure 3 - Example C-BUS Hardware Interconnections

C-BUS Serial Interfacing

C-BUS is the controlling hardware and software interface for all members of the DBS 800 family. It enables the serial, bi-directional transfer of commands and data throughout the system, allowing total flexibility of operational control and data handling. System upgrades can be achieved by a simple software or firmware change.

C-BUS Hardware Interface

The BUS physically consists of 5 lines:

- **Serial Clock line** - driven by the microcontroller to all peripherals. All C-BUS commands and data transfers are synchronized, in bursts of 8 bits, to this clock.
- **Command Data** - to address, command, and transfer data from the microcontroller to a selected peripheral.
- **Reply Data line** - transfer of requested (commanded) data from the addressed peripheral as the result of a specific Address/Command (A/C).
- **Chip Select (CS) line** - carries the CS timing command from the microcontroller to all peripherals. All C-BUS sequences are initiated, completed, or aborted by this CS signal. (See Timing Diagrams in respective DBS 800 data bulletins.) All peripherals on the C-BUS will receive the CS signal, but only the peripheral that is addressed will react. Table 4 contains a list of all DBS 800 C-BUS Address allocations.
- **Interrupt Request (IRQ) line** - interactive peripherals have an Interrupt output (IRQ) for connection to the microcontroller interrupt input.

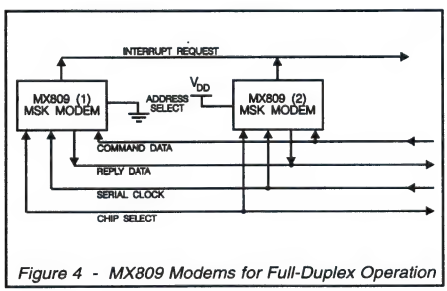


Figure 4 - MX809 Modems for Full-Duplex Operation

Full-Duplex Configuration

Figure 4 shows the configuration of the Address Select inputs when using 2 MX809 Modems on the C-BUS. MX805A Sub-Audio Signaling Processors should be embodied in the same manner when full-duplex operation is required.

C-BUS Serial Clock Rate

Generally, C-BUS Serial Clock rates that are harmonically related to the Xtal/Serial Clock = 32; this frequency cannot produce alias effects within a microcircuit, therefore using a C-BUS Serial Clock rate at this frequency is preferable. If it proves impractical to select a synchronous C-BUS clock, coupling between sensitive analog inputs (such as the MX806A Mic. Inputs) and the C-BUS should be avoided.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830060.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

"C-BUS" Controlling System

The Use of C-BUS Software and Protocol

Each individual DBS 800 Data Bulletin contains a table listing the C-BUS commands and instructions relevant to that peripheral. Table 4 gives an abridged list of all DBS 800 address allocations.

All transactions begin with the CS line going to a logic "0" level (Figure 5). The first byte that must be transmitted to the peripheral, on the Command Data line, is an Address/Command (A/C) byte. Generally, all bytes are transmitted MSB first.

Address/Command (A/C) Byte

Part of this byte is the "Address" that specifies which IC (or ICs) has been selected for that particular transaction. The second part of the A/C is the "Command" to fulfill a particular function (see Table 4).

The A/C may be followed by either
(a) a qualifying instruction, or
(b) data bytes from the microcontroller via the Command Data line or from the peripheral via the Reply Data line.

Example C-BUS Transactions

Address/Command byte 61_H is recognized as:

Address	/	Command
MX802 DVSR Codec	/	*Read Status Register*

- and in this case would be followed by 1 byte of Status data transmitted on the Reply Data line from the MX802 to the microcontroller.

Address/Command byte 10_H is recognized as:

Address	/	Command
MX806A Audio Processor	/	*Control Command*

- and in this case would be followed by 1 byte of Control data transmitted on the Command Data line from the microcontroller to the MX806A.

Address/Command byte 01_H is recognized as:

Address	/	Command
General Reset		

- and in this case will reset ALL DBS 800 ICs connected to the C-BUS. (Individual IC Data Bulletins give details of the General Reset actions.)

DBS 800 IC Sampling Rates

IC Functions		Xtal/Clock Frequencies (MHz) 4.00	4.032	4.096
		Sample Clock Rates (kbit/s)		
MX802DVSR Codec				
Voice Filters	at 16, 32 & 64 kbps	125	126	128
Voice Filters	at 25 & 50 kbps	100	100.8	102.4
Voice Sample Rates	16.0kbps	15.625	15.75	16.0
	25.0kbps	25.0	25.2	25.8
(Nominal)	32.0kbps	31.25	31.5	32.0
	50.0kbps	50.0	50.4	51.2
	64.0kbps	62.5	63.0	64.0
MX803A Audio Signaling Processor				
Tone Filters	Max	166	168	170
	Min.	13.15	13.28	13.47
Digital Filters	High	13.8	14.0	14.2
	Mid.	6.9	7.0	7.1
	Ext.	27.0	28.0	28.4
MX805A Sub-Audio Signaling Processor				
Voice Filters		125	126	
TX Filters	Max.	62.5	63.0	
	Min.	12.5	12.6	
RX Filters		35.7	36.0	
	or	25.0	25.2	
Digital Filters		1.04	1.05	
MX806A LMR Audio Processor				
Voice Filters		125	126	
MX809 MSK Modem				
TX Filters		250	252	
	or	166	168	
RX Filters		125	126	

If the Xtal/Clock frequency 4.096 MHz is used with the MX805A, MX806A, or MX809, it may result in sampling clock rates that place the voice-filter passband frequencies outside CEPT specifications.

Table 3 - Examples of DBS 800 IC sample rates relative to Xtal/Clock inputs

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830060.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

"C-BUS" Controlling Protocol

(a) C-BUS Address Listing: C-BUS Addresses (HEX) currently allocated to DBS 800 ICs.

C-BUS Performance Testing	00
General (all device) Reset	01
Audio Processor	**MX806A**
Control Command	10
Mode Command	11
Modulator Levels Set	12
Volume Set	13
Audio Signaling Processor	**MX803A**
Write to Control Register	30
Read Status Register	31
Read RX Tone Frequency	32
Write to Notone Timer	33
Write to TX Tone Generator 1	34
Write to TX Tone Generator 2	35
Write to G/Purpose Timer	36
MSK Modem 1	**MX809**
Write to Control Register	40
Read Status Register	41
Read RX Data Buffer	42
Write to TX Data Buffer	43
Write to Sync Program	44
MSK Modem 2	**MX809**
Write to Control Register	48
Read Status Register	49
Read RX Data Buffer	4A
Write to TX Data Buffer	4B
Write to Sync Program	4C
C-BUS Performance Testing	55

DVSR Codec	**MX802**
Write to Control Register	60
Read Status Register	61
Store "N" pages, Start page X (immediate)	62
Store "N" pages, Start page X (buffered)	63
Play "N" pages, Start page X (immediate)	64
Play "N" pages, Start page X (buffered)	65
Write Data, Start page P	66
Read Data, Start page P	67
Write Data, Continue	68
Read Data, Continue	69
Sub-Audio Signaling Processor 1	**MX805A**
Write to Control Register	70
Read Status Register	71
Read CTCSS RX Data	72
Write to CTCSS/NRZ TX	73
Read NRZ RX Data	74
Write to NRZ Data TX	75
Write to Gain Set	76
Sub-Audio Signaling Processor 2	**MX805A**
Write to Control Register	78
Read Status Register	79
Read CTCSS RX Data	7A
Write to CTCSS/NRZ TX	7B
Read NRZ RX Data	7C
Write to NRZ Data TX	7D
Write to Gain Set	7E
C-BUS Performance Testing	AA
C-BUS Performance Testing	FF

(b) Reserved Addresses: C-BUS Addresses (HEX) reserved for future DBS 800 IC/system use.

General Functions	02 to 07
Future Audio Processors	14 to 1F
Future Speech Products	20 to 2F
Future Audio Signaling Processors	37 to 3F
Future MSK Modems	45 to 47
Future MSK Modems	4D to 4F
Future DVSR Codecs	6A to 6F
Future Sub-Audio Signaling Processors	77
Future Sub-Audio Signaling Processors	7F
Future Products	80 to 8F
Future Products	90 to 9F
Future Products	D0 to DF
Future Products	E0 to EF

(c) Spare Addresses: C-BUS Addresses (HEX) that will not be allocated for DBS 800 IC/system use and are available for custom use.

08 to 0F	50 to 54	56 to 5F	A0 to A9
AB to AF	B0 to BF	C0 to CF	F0 to FE

Table 4 - C-BUS Address Allocations

General Reset

The General Reset command (01_H), when transmitted from the microcontroller, is non-selective and will reset all DBS 800 ICs connected to the C-BUS. Detailed information on the way this command affects each DBS 800 device can be found in individual Data Bulletins.

C-BUS Performance Testing

To asses the effect of C-BUS activity on audio noise levels, 4 addresses are allocated for C-BUS performance testing:

00_H	00000000	-all 0's
55_H	01010101	-bit reversals
AA_H	10101010	-bit reversals
FF_H	11111111	-all 1's

These bytes, which do not produce any changes in current, active DBS 800 settings and configurations, provide C-BUS activity. These A/C bytes, when following a $\overline{CS}$ edge, are ignored by the DBS 800 chip set and can be loaded as Command Data individually, or in common or mixed groups.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830060.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

Technical Specifications

Section 11: Development Kits

Device	Description	Page
DB900	Development Kit for the MX909A, MX919A, and MX929A	3
DB600	μController Board for use with DB602 and DB604	5
DB602	Development Kit for the MX602	7
DB604	Development Kit for the MX604	9
DB469	Development Kit for the MX469	11
DB800	Development Kit for the MX818, MX828, and MX829	13
DB1065	Development Kit for the MX465	15
DBS800	Development Kit for the DBS800	17

MX•COM, INC. MiXed Signal ICs

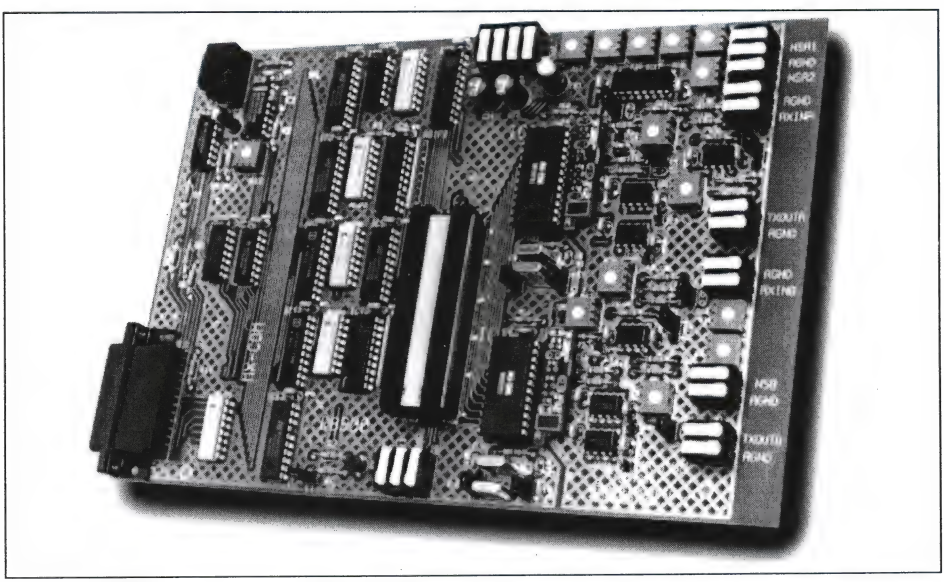
PRODUCT INFORMATION

DB900

Modem Development Kit for the MX909A, MX919A and MX929A

FEATURES

- **Exercise all modem functions with supplied PC software virtual interface**
- **Supports Narrow Bandwidth GMSK and 4-level FSK modulation**
- **Two baseband modem circuits provide simultaneous Rx and Tx functions**
- **Hardware interfaces support integration into product prototypes**
- **Includes MX909A, MX919A, and MX929A components**
- **User configurable to support different modems and data rates**
- **Adjustable gain, offset, and noise injection ports for error rate testing**
- **Test Points for probe access**



The DB900 Modem Development Kit is a complete test platform to demonstrate and test the MX909A, MX919A, and MX929A components. These parts include Gaussian filtered minimum shift keying (GMSK) or four level frequency shift keying (4 Level FSK) modems which execute a rich set of communication protocol tasks to maximize performance and minimize end product power consumption and cost. Automated modem functions include: bit and frame synch; forward error correction (FEC); cyclic redundancy checking (CRC); header, intermediate, and last block Tx & Rx; data interleaving for FEC enhancement; and support for protocols such as Mobitex™, RD-LAP™, and ARDIS℠.

The DB900 Modem Development Kit includes a pair of complete baseband modem circuits; one pair each of the MX909A, MX919A, and MX929A components; PC software; and a hardware interface to connect to the parallel port of your Microsoft Windows™ compatible personal computer. Modem circuits can be easily configured for user selected baud rates and operated using various automated test sequences. Signal injection circuits for each of the two channels include gain and offset adjustments to create a variety of test conditions. Modem circuits can be connected to end system designs via an exposed hardware interface.

©MX-COM 1996, 4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA Doc.# 20830016.001
800 638-5577 910 744-5050 Fax 910 744-5054 All trademarks and service marks are held by their respective companies.

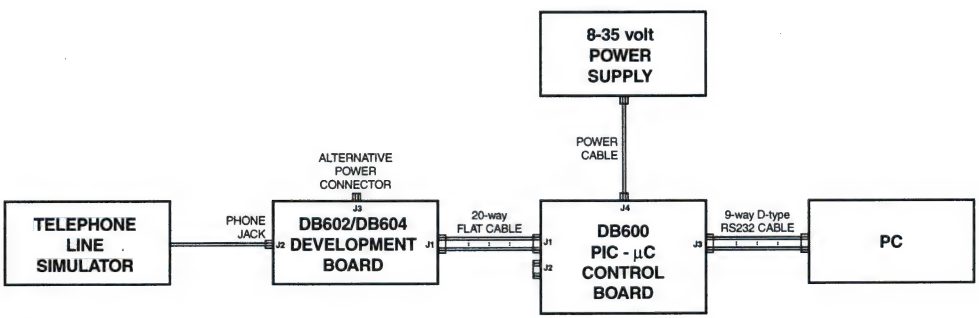
MX•COM, INC. MiXed Signal ICs

PRODUCT INFROMATION

DB600 µController Board for use with DB602 and DB604

FEATURES

- For use with DB602 and DB604
- Executes Applications Software for MX602, MX604 and MX614
- On-Board PIC Programming with Serial Interface and PC Software
- Serial (RS232) Interface to a PC
- Diagnostic Firmware/Software
- Socketed PIC 16-Series µC
- 8.0V - 35.0V Single Power Supply Operation
- On-Board Supply Regulator



The DB600 Development Board was designed for use with the DB602 and DB604 Development Kits. The DB602 is used to evaluate the MX602 and the DB604 is used to evaluate the MX604 and MX614.

The DB600 Development Kit consists of one board containing a socket for a UV-erasable PIC µC which the user may program and control via the RS232 serial interface. With the aid of suitable applications software, the user can demonstrate the use of the MX602, MX604 or MX614 in various telecommunication applications.

The DB600 may be powered from a single 8 - 35V dc power supply. There is an on-board regulator which sets the 3.3V or 5.0V requirement. The PIC µC may be driven from an external clock, or from its own crystal oscillator. Test points provide access to programming voltages. Additional space was designed in for the user to ZIF-socket the PIC µC, if desired. Interconnecting cables are provided for an RS232 link to a PC and for 20-way flat cable connections to other MX-COM Development Kits or other parts in a user's system.

This DB600 Development Kit is designed to be a general purpose product which may be used to support other MX-COM Development Kits in the future. Applications software is regularly updated and users should contact MX-COM for further details.

© 1997 MX•COM, Inc.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20830078.001
All trademarks and service marks are held by their respective companies.

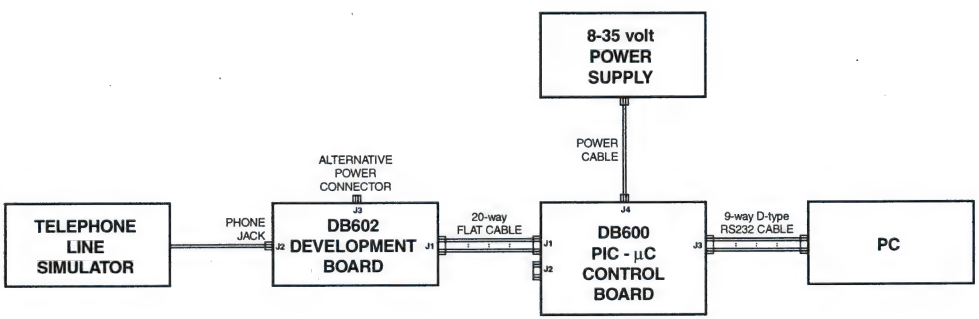
MX•COM, INC. MiXed Signal ICs

PRODUCT INFORMATION

DB602 Development Kit for the MX602

FEATURES

- For MX602 (Caller ID/Caller ID on Call Waiting) Product Development
- Reconfigurable Board with Interface to Optional µC Board
- Parallel Phone Detector
- Easy Access to Test Points
- User's Prototyping Area
- Space for Optional and Telco-Specific Components
- 8.0V - 35.0V Single Power Supply Operation
- On-Board Supply Regulator



The DB602 Development Kit consists of a single board containing an MX602 and the associated line interface components. The DB602 communicates with the MX-COM µC board (DB600), or with the user's own µC board. Each of which can demonstrate the use of the MX602 in various telecommunications applications, when user programmed. The DB602 board is powered from a single 8 - 35V dc power supply. An on-board regulator sets the 3.3V or 5.0V requirement. LEDs indicate data, control and interrupt line status (ZP, MODE, $\overline{IRQ}$ and DET) and the MX602 may be driven from an external clock, or from its own crystal oscillator. Easily accessible test points are provided for the monitoring of test signals. A socket is provided for the easy replacement of the MX602 or a user may fit a ZIF socket if desired. Additional user prototyping area is also provided on the DB602.

On-board relays may be used to implement a wetting pulse, to place an ac or dc load on the line, and to interface the line to a transformer/op-amp hybrid for voice communications. A mutable voice input and a µC controllable or pre-settable DTMF generator are provided for Caller ID/Caller ID on Call Waiting applications. Operation of both these and the relays are indicated by LEDs. The parallel phone detector may be used in adjunct box emulation. The MX602 supply current may be measured by removing a jumper. Where components are telco-specific (line impedance, line protection, ac-load, wetting pulse, etc.) space is provided for the user to add appropriate components.

© 1997 MX•COM, Inc.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20830079.001
All trademarks and service marks are held by their respective companies.

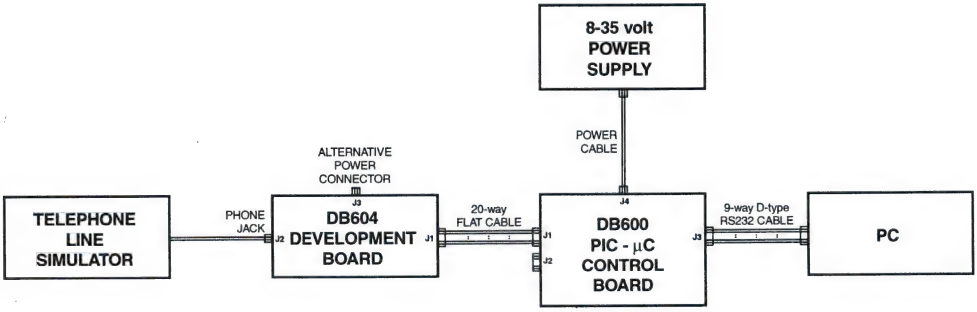
MX•COM, INC. MiXed Signal ICs

PRODUCT INFORMATION

DB604 Development Kit for the MX604 and MX614

FEATURES

- **For 1200bps FSK Modem (MX604 - v.23 Compatible Modem) and (MX614 - Bell 202 Compatible Modem) Product Development**
- **Reconfigurable Board with Interface to Optional µC Board**
- **Parallel Phone Detector**
- **Easy Access to Test Points**
- **User's Prototyping Area**
- **Space for Optional and Telco-Specific Components**
- **8.0V - 35.0V Single Power Supply Operation**
- **On-Board Supply Regulator**



The DB604 Development Kit consists of a single board containing an MX604 or an MX614 and the associated line interface components. The DB604 communicates with the MX-COM µC board (DB600), or with the user's own µC board. Each of which can demonstrate the use of the MX604/MX614 in various telecommunications applications, when user programmed. The DB604 board is powered from a single 8 - 35V dc power supply. An on-board regulator sets the 3.3V or 5.0V requirement. LEDs indicate data, control and interrupt line status (DET, $\overline{\text{RDY}}$, RXEQ, M0, and M1) and the MX604 may be driven from an external clock, or from its own crystal oscillator. Easily accessible test points are provided for the monitoring of test signals. A socket is provided for the easy replacement of the MX604/MX614 or a user may fit a ZIF socket if desired. Additional user prototyping area is also provided on the DB604.

On-board relays may be used to implement a wetting pulse, to place an ac or dc load on the line, and to interface the line to a transformer/op-amp hybrid for voice communications. A mutable voice input and a µC controllable or pre-settable DTMF generator are provided. Operation of both these and the relays are indicated by LEDs. The parallel phone detector may be used in adjunct box emulation. The MX604/MX614 supply current may be measured by removing a jumper. Where components are telco-specific (line impedance, line protection, ac-load, wetting pulse, etc.) space is provided for the user to add appropriate components.

© 1997 MX•COM, Inc.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20830080.001
All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

PRODUCT INFORMATION

DB469 Development Kit for the MX469

FEATURES

- **For MX469 Product Development**
- **Reconfigurable Board with Sync/Async operation.**
- **1200/2400 baud selectable**
- **Easy Access to Test Points**
- **Easy configuration/connection for standard bit error rate testing.**
- **Stand alone evaluation**
- **RS232 or TTL serial port connection**
- **Communicates with a PC over RS232 interface**
- **On-Board Supply Regulator**
- **Separate on-board noise summing and gain adjustment circuits.**

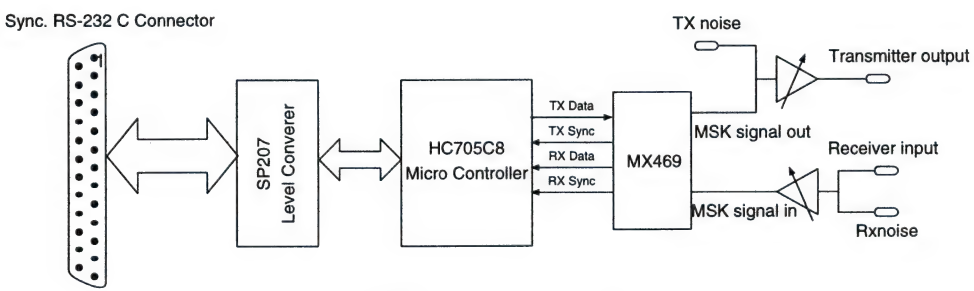


Figure1. DB469 block diagram

It is simple to set-up and use the DB469 development kit which provides a solid means of evaluating MXCOM's MSK modem IC MX469. A single DB469 can be used for complete evaluation of MX469 by connecting the device in loop around mode. The MX469 is a synchronous modem, by appropriately connecting some jumpers on the PC board, DB469 can be operated in both synchronous and asynchronous modes. In asynchrounous mode the microprocessor acts as asynchrnous to synchronous data converter by buffering the data internally and supplying it to MX469 in a synchronous fashion. A sample firmware program is provided for the micro comptroller when used in asynchronous mode. A personal computer running RS232 termianl emulator software can be used as a display terminal in a talk and listen mode. In synchronous mode the microprocessor is by-passed with on board jumpers. The evaluaiton board contains noise summing amplifiers at the MSK TX output and Rx input of MX469 to evaluate performance at different signal to noise ratios.

© 1997 MX•COM, Inc.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20830083.001
All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

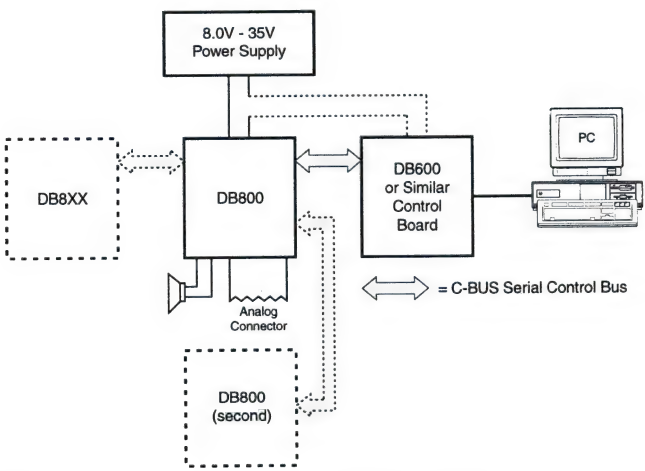
PRODUCT INFROMATION

DB800

Development Kit for the MX818, MX828, and MX829

FEATURES

- **For MX818 (CTCSS), MX828 (CTCSS, DCS, SelCall), and MX829 (1200/2400bps MSK Modem, Tx/Rx Audio Processor, DTMF Encoder) Product Evaluation**
- **Interface to Optional μC Board**
- **On-Board Microphone**
- **On-Board Regulator**
- **Easy Access Test Points**
- **8.0V - 35.0V Single Power Supply Operation**
- **Speaker Output**
- **Socketed Discrete Components around Target Devices**
- **User's Prototype Area**



The DB800 Development Kit consists of a single board containing an MX828 and an MX829. An MX818 is also provided which can be fitted in place of the MX828.

The DB800 board is powered by a single 8 - 35V dc power supply. An on-board regulator sets the 3.3V or 5.0V requirement. LEDs indicate the status of the MX829 carrier detect output and the MX828 comparator output. Both lines are available at the same connectors as the C-BUS. There is an on-board microphone and a speaker output.

The MX828/818 and MX829 may be driven from a common external clock, or from a common crystal oscillator. The supply current of either target device may be measured by removing the appropriate jumper. Easily accessible test points are provided for the monitoring of test signals. Additional prototyping space has been provided for the user.

Serial control bus (C-BUS) signals are made accessible at three connector regions. Two include both C-BUS and MX828/MX829 I/O signals to support experiments for both Tx and Rx ends of a system. The third region includes C-BUS signals only to support daisy chaining of other C-BUS compatible equipment which may be found in complete system designs.

The DB800 can be used with the MX-COM μC board (DB600), or the user's own μC board, with appropriate software. Component footprints are provided in case the user requires level shifting between the C-BUS input logic HI and the V_{DD} level of the DB800.

© 1997 MX•COM, Inc.
www.mxcom.com Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20830081.001
All trademarks and service marks are held by their respective companies.

MX•COM, INC. MiXed Signal ICs

PRODUCT INFORMATION

DB1065

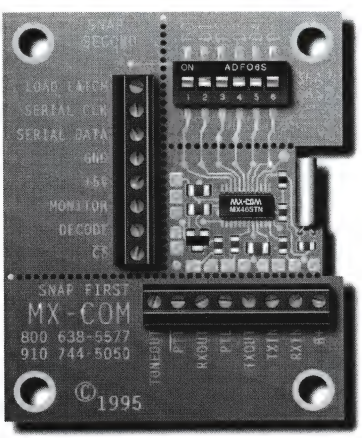
MX465 CTCSS Encoder/ Decoder Development Kit

Features

- **Quick Solderless Connections**
- **On Board Regulator**
- **Dip Switch Selectable Tones**
- **Small Snap-out Circuit**
- **47 CTCSS Tones + Notone**
- **Parallel Programming using Dip Switch Serial mode also available**

Applications

- **Mobile Radio Channel Sharing**
- **Repeater Control**
- **Wireless Intercom Traffic Control**
- **Hookswitch Supervision**
- **Simultaneous Voice Plus Control Signaling**
- **Remote Control**



The DB1065 Development Kit provides an evaluation platform complimentary to the MX465. Convenient access to the MX465's entire feature set, with user's manual and data bulletin, allows rapid MX465 evaluation, development and design. Utilizing a dip switch for tone selection and quick connect screw terminals, various configurations can be evaluated quickly. In addition, a smaller sub-circuit may be snapped apart from the main PCB board for an embeded evaluation. On board circuits provide several methods to set tone encoding, indicate tone detection, and mute/unmute the audio path. External 8-25 VDC or 2.7-5.5 VDC regulated power supplies are supported. The MX465 provides Continuous Tone Controlled Sub-audible Squelch (CTCSS) encoding and decoding for a discrete tone, taken from a field of 39, in the range of 67 to 250 Hz, according to TIA/EIA-603 Standard plus 159.8Hz, 183.5Hz, 189.9Hz, 196.6Hz, 199.5Hz, 206.5Hz, 229.1Hz, and 254.1Hz.

CTCSS tone signaling 'hides' control commands below the normal voice spectrum to allow combined voice and control features. Because the hidden signals are embedded in a subaudio band, CTCSS can easily enhance existing voice systems without requiring major design modifications.

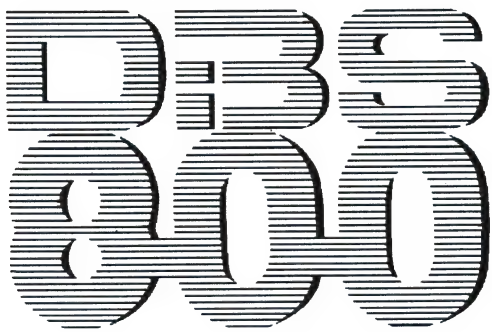
In systems where multiple receivers are connected to a common transmitter, control signals can be used to select individual or grouped receivers as found in intercom and radio systems. CTCSS can also activate various functions in a remote receiver while conversation takes place. Example applications include:

- LMR's (Land Mobile Radios) address individual and grouped target receivers, all sharing the same radio frequency channel, while sustaining voice communications.
- LMR radio systems identify traffic which must be re-transmitted on repeaters for longer range communications.
- Intercom allows audience selection using push-button control.
- Caller identification uses caller's subaudio signal tone as identification code.
- Simultaneously transmit voice while activating remote control functions (e.g. stop, go, turn left, turn right) with CTCSS.
- Hidden CTCSS signals coordinate and activate programmed events in audio/video playback systems (training, display and toy applications).

©MX-COM 1996, 4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA Doc. # 20830022.002

800 638-5577 910 744-5050 Fax 910 744-5054 All trademarks and service marks are held by their respective companies.

MX•COM, INC.



Digitally-integrated Baseband Subsystem

DBS 800 Development Kit

C-BUS
COMPATIBLE

© 1997 MX•COM, Inc.
www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA
Doc. # 20830082.001
All trademarks and service marks are held by their respective companies.

DBS800 Devkit Introduction

OVERVIEW

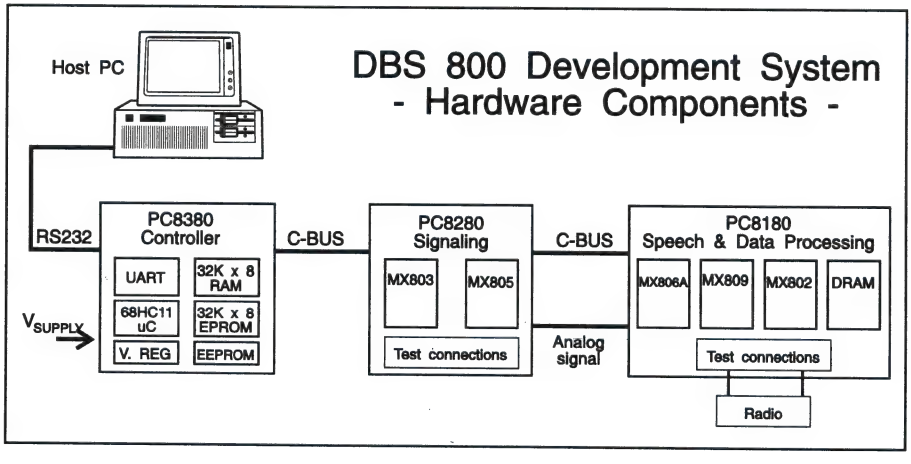
The DBS800 Development System (Devkit) is a general purpose hardware and software platform for:

- The evaluation and functional testing of DBS800 devices (the MX802, MX803A, MX805A, MX806A & MX809).
- The demonstration and evaluation of DBS800 group functions.
- A base for use in developing application-specific software routines.

This document provides a general introduction to the Development System. Additional software and supporting documentation is available that demonstrates DBS800 application-specific functions, such as Voice Management, Data Communications, Sub-Audio Signaling and Selective Calling.

SYSTEM COMPONENTS

The complete DBS800 Development System consists of three printed circuit boards (PC8380, PC8280 & PC8180) with their interconnecting cables, software on diskette and EPROM, and supporting documentation. Access to the system is through a 'Host' PC.



© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054 Doc. # 20830082.001
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA All trademarks and service marks are held by their respective companies.

HARDWARE

The PC8180 Speech and Data Board is used for the evaluation of the MX802 DVSR Codec, MX806A Audio Processor and MX809 MSK Modem devices. It is controlled by a C-BUS link from the PC8380 controller board, and includes peripheral components, test links and connectors to allow the devices to be tested individually or in several representative combinations. For a detailed description of this board, see the document "PC8180 Speech and Data DevKit Documentation."

The PC8280 Signaling Board provides a similar hardware platform for evaluation of the MX803 Audio Signaling Processor and MX805 Sub-Audio Signaling Processor and is fully described in "PC8280 Signaling DevKit Documentation."

The PC8380 Controller Board contains a 68HC11 microcontroller with RAM, EPROM, EEPROM, C-BUS and RS232 ports, and is used to control the DBS800 devices on the attached PC8180 and/or PC8280 boards. For DBS800 device evaluation, the PC8380 may run under the direct control of the 'Host' PC or it may run a special test program downloaded from the 'Host' PC. "PC8380 Controller DevKit Documentation" gives a complete description of this board.

In some circumstances you may wish to use two sets of boards, for example to evaluate the end to end performance of a link using the (half duplex) MX809 MSK Modem devices. You could use a separate 'Host' PC to control each set of boards, but the Development System also lets you connect two sets of PC8180/8280/8380 boards to a single PC.

The **'Host' PC** can be any IBM compatible 80*88 or 80*86 based computer running MS-DOS (or PC-DOS) V 2.0 or greater with at least 512k bytes of RAM, a disk drive and an RS232 port (COM1 or COM2) capable of running at 9600 baud. A color graphics display, hard disk drive, and a second RS232 port are useful but not essential. Although the software will run on a PC/XT, a faster machine will give a smoother response to the user's input.

SOFTWARE

The **software components** of the Development System are DLINK86 (the 'Host' PC control software), DLINK11 (which controls the.68HC11 microcontroller on the PC8380 board), and various special DBS800 device evaluation programs. DLINK11 is contained in an EPROM on the PC8380 board. Other software is supplied on a diskette.

The Evaluation diskette supplied with the DBS800 Development System contains all of the programs needed to run the system:

DLINK86.EXE:	the 'Host' PC software.
Various '.HEX' files:	specific device test programs.

You will also receive a diskette for LTR evaluation (p/n 40450005.001) and one for DCS evaluation (p/n 40450006.001).

The diskettes also contain contain source files, of interest to a programmer but not needed to actually run the system. In addition, there may be a READ.ME text file on the disk, giving details of any recent updates to the programs or their use. The DBS800 Development System software may be run from diskette or from a hard disk.

MS-DOS is a trademark of Microsoft Corporation. PC-DOS is a trademark of IBM Corporation.
LTR is a trademark of EF Johnson Co.

© 1997 MX•COM, Inc. www.mxcom.com Tele: 800 638-5577 910 744-5050 Fax: 910 744-5054
4800 Bethania Station Road, Winston-Salem, NC 27105-1201 USA Doc. # 20830082.001
All trademarks and service marks are held by their respective companies.

Appendix

Description	Page
Glossary of Technical Terms	3
Device Handling Procedures	7
Package Description	9
Tape and Reel Specifications	11
Notes	17

Glossary of Technical Terms

ADPCM	Adaptive Differential Pulse Code Modulation
AGC	Automatic Gain Control
AMPS/NAMPS	Advanced Mobile Phone Service is a cellular system used in the United States. NAMPS (Narrow AMPS) uses FDMA technique to derive three voice channels from one AMPS channel.
ANI	Automatic Number Identification: Identification of the transmitting party by a pre-assigned number.
ANSI	American National Standards Institute: A voluntary organization in the United States that coordinates standards.
ARDIS™	An FM radio data system that operates at 9.6kbps and 19.2kbps. Trademarked by Motorola.
Asynchronous Transmission	A mode of data transmission in which each bit is not in sync. Regarding frequency or timing. Signals are sent as groups of a specified length with start and stop bit indicators at the beginning and end of each group.
Bandwidth	The range of frequencies within which a device can transmit or receive.
Baseband	The band of frequencies which is modulated on a carrier or subcarrier in a wire or radio transmission system to form the transmitted signal.
Baud	A unit that measures signaling speed in signal events per second. This may not be the same as bits per second.
BCD	Binary Coded Decimal: A binary (1,0) numbering system in which the digits 0 through 9 are represented by four bits.
BER	Bit Error Rate: A ratio of the number of transmitted bits that are incorrectly received to the number that are correctly received.
Bit Rate	The speed at which bits are transmitted over a data channel, given in bits per second (bps).
Carrier	A carrier is a wave capable of being modulated by an information-carrying signal. The use of multiple carriers permits multiple voice frequency signals in the same transmission, as in frequency division multiplexing.
C-BUS	MX-COM's serial control bus used to communicate digital information between a µP or µC and a peripheral IC such as the MX803A, MX818, and MX829.
CCIR	International Radio Consultative Committee, a subsidiary organization of the International Telegraphic Union dealing in radio standards.
CCITT	The Consultative Committee on International Telegraph and Telephone is an International Telecommunications Standard Agency. It has been renamed ITU-T.
CDMA	Code Division Multiple Access
CDPD	Cellular Digital Packet Data: An industry standard for data transmission. CDPD utilizes that analog cellular networks already in place in the United States and Canada to provide 2-way data communications for users of devices such as laptops and PDAs.
Channel, Voice Grade	A channel with a frequency range of about 300Hz to 3400Hz which is suitable for transmission of data or speech in analog form.
CID	Caller Identification or Calling Line Identifier (Type 1)
CIDCW	Caller Identification on Call Waiting or Calling Line Identifier on Call Waiting (Type 2)
C-MSG	'C-Message Weighting': Represents frequency response of typical United States telephone wireline.
CMOS	Complementary Metal-Oxide Semiconductor (an integrated semiconductor manufacturing process). MXCOM uses both Metal-gate CMOS and Silicon-gate CMOS processes.
CODEC	A single device comprising both Encoder and an Decoder.
Compandor	Acronym for Compressor-Expander, a circuit that compresses the dynamic range of an input signal and expands it almost back to its original form on the output.
Concatenation	Combining multiple data packets or frames in a contiguous series.
CPFSK	Continuous Phase Frequency Shift Keying

Glossary of Technical Terms

CPM	Continuous Phase Modulation
Crosstalk	Undesired crossover of voice transmissions from one circuit to another.
CS	Carrier Sense: a logic level supplied by the radio when and RF carrier is detected.
CTCSS	Continuous Tone-Controlled Squelch System: A type of tone decoding used in 2-way radio systems in which a sub-audible tone, taken from a field of 39 in the 67Hz to 250Hz range, is multiplexed continuously with speech to engage repeaters and allocate traffic among talk groups on shared channels. Trademarked by Motorola as Private Line or PL.
CVSD	Continuously Variable Slope Delta Modulation: A method by which a voice signal is digitized for transmission, and then changed back to an analog voice signal for reception
DCE	Data Communications Equipment or Data Circuit-Terminating Equipment: This equipment functions to establish and maintain a connection, and provides signal conversion between a terminal and data or telephone line.
DCS/CDCSS	Digital Coded Squelch: Similar to CTCSS in function but utilizes 13? digital tones to control the same operations Trademarked by Motorola as Digital Private Line or DPL.
DPCM	Differential Pulse Code Modulation
DPM	Differential Phase Modulation
DQPSK	Differential Quadrature Phase Shift Keying: $\frac{\pi}{4}\text{DQPSK} \Rightarrow \text{Shift} = \frac{\pi}{4}$
DSP	Digital signal Processing
DTMF	Dual Tone Multi-Frequency: A telephone signaling system employing four tones from a low group and three or four tones from a high group comprising twelve to sixteen different unique tone pairs. Radio applications of DTMF should avoid "twist" (differences in level between tone pairs) and time-limit digits to prevent signaling errors caused by fades.
DVSR	Data/Voice Storage and Retrieval. Trademarked by MXCOM as Radio MailVox.
ECPA	Electronic Communications Privacy Act of 1986: This amendment to Section 2510 of title 18, United States Code, establishes the illegality if intercepting protected (i.e. scrambled) communications.
EIA	Electronics Industry Association: A United States Manufacturer's group which, as part of its function, sets and publishes electronics standards.
Eye Pattern / Eye Diagram	An oscilloscope display of the detector voltage waveform in a modem. The openness of an eye gives a representation of the bit error rate (the more open, the less distortion).
FDMA	Frequency Division Multiple Access
FEC	Forward Error Correction
FFSK	Fast Frequency Shift Keying: See MSK
FSK	Frequency Shift Keying: a form of frequency modulation used to transmit two states of a signal as two separate frequencies. FSK is characterized by frequency spacing of 1
Full-Duplex	Simultaneous two-way communication
Gaussian Filter	A filter having the symmetrical bell shape of a Gaussian curve (normal distribution)
GFSK	Gaussian Filtered Frequency Shift Keying: (mod index $\neq 0.5$)
GMSK	Gaussian Minimum Shift Keying: A type of FSK that uses pre-modulation Gaussian filtering to achieve high data rates in an FM communications channel bandwidth.
GPS	Global Positioning System
Half-Duplex	Communications in which both transmit and receive occur , but not at the same time.

Glossary of Technical Terms

HSC	Hexadecimal Sequential Coding: A tone signaling protocol comprising 16 tone states. Ten tone states represent decimals 0-9, a NOTONE, a Repeat tone, a Group tone, an address/DATA frame delineator, plus Reset and control, totaling 16 tone-coded logic states. HSC operation is predicated on a decoding technique able to detect tones in random order. These must be contained within a frame preceded and concluded by NOTONE. HSC Tonesets: HSC-A: USA or Metropage™. A Motorola radio Paging system employing sequential tones comprising ten decimal and two special function tones ("R" for repeat and "X" as an alternate address) and NOTONE in a predictive code format. HSC-C: CCIR toneset. A toneset developed by the International Radio Consultative Committee. HSC-E: EEA toneset. An EEA (UK) variation of the CCIR HSC toneset, in which the lowest frequency tone is 930Hz and the highest is 2247Hz. Duration is 40ms HSC-Z: ZVEI German HSC toneset HSC-ZS: SZVEI or Suppressed ZVEI HSC toneset
IEEE	The Institute of Electrical and Electronic Engineers: One of the functions of this association of engineers is to publish standards defining technical terms.
ITU-T	International Telegraphic Union: Telecommunications (includes the CCITT and CCIR) is an international telecommunications standards agency.
Jitter	Small, abrupt, spurious variations in a waveform due to time, amplitude frequency or phase
LMR	Land Mobile Radio System
LSI	Large Scale Integration
LTR™	EF Johnson trademarked trunking system.
MOBITEX	A data transmission protocol developed by Swedish Telecom.
MODEM	Modulator/Demodulator: This is a type of DCE that connects data terminal equipment to a communications line/channel. It converts data to and from the signal form needed for the communication channel.
Modulation	The process of modulation a carrier or signal for transmission, also the result of this process.
Monolithic	Constructed from a single crystal or piece of material
MSK	Minimum Shift Keying: Continuous phase FSK modulation (also called FFSK) used to transmit two states of a signal as two separate frequencies using coherent detection and a frequency spacing of 0.5.
Multiplexing	Combining multiple signals for transmission as a group over a single transmission facility.
NMT	Nordic Mobile Telephone: A Cellular communication systems used primarily in Europe
PABX	Private Automatic Branch Exchange
PAMR	Public Access Mobile Radio
PCM	Pulse Code Modulation: A process in which an analog signal is sampled and converted to a binary code for transmission
PCMCIA (PC CARD)	Personal Computer Memory Card International Association: This association defines and promotes an interchangeable standard for PC memory and expansion cards. The PCMCIA standard applies to 68-pin I/O or interchange type cards.
PCS	Personal Communications Services
PDA	Personal Digital Assistant: A handheld computer that provides functions lit a notepad or messagepad. PDAs often include data transmission capabilities
PL	Private Line: A Motorola trademarked name for CTCSS
PMR	Public Mobile Radio
PSK	Phase Shift Keying: A form of phase modulation requiring coherent detection. The most straightforward type of PSK shifts the carrier by 0° or 180°.

Glossary of Technical Terms

Psophometric	A weighting curve used to represent the energy density of speech.
PTM/PTL	'Push To Monitor' or 'Push To Listen': This is a control on two-way portable and mobile radios that allows channel monitoring.
PTT	'Push To Talk': This is a control on two-way portable and mobile radios that enables transmission.
PSTN	Public Switched Telephone Network:
Pvt SQUELCH™	MX•COM's trademarked combination of CTCSS and voice inversion to provide voice privacy.
QAM	Quadrature Amplitude Modulation: A hybrid amplitude/phase modulation technique that allows the transmission of four bits of information during a signaling interval, and requires less bandwidth than normal amplitude or phase modulation techniques.
QPSK	Quadrature Phase Shift Keying
Quick Call II™	A Motorola trademarked 2-Tone sequential signaling format comprising 80 tones arranged in eight tone groups
R2000	This is a trunked communication system used in France.
RD-LAP™	An FM radio data protocol that operates at 9.6kbps and 19.2kbps. Trademarked by Motorola.
Repeater	a device used as an intermediate point in a communications system to receive and retransmit signals, often for the purpose of extending range.
SAT	Supervisory Audio Tone used in cellular systems.
SIGATE	Silicon Gate: A CMOS process used in manufacturing ICs that is smaller and more modern than metal gate.
Simplex	A circuit which can communicate information in one direction only.
SINAD	A ratio of the total output power to the power of noise plus distortion only: $\frac{\text{signal} + \text{noise} + \text{distortion}}{\text{noise} + \text{distortion}}$
SIT	Special Information Tones
SMD/SMT	Surface Mount Device / Surface Mount Technology
SMR	Specialized Mobile Radio
SS	Spread Spectrum: The spreading of a signal over a wider bandwidth than the minimum required for transmission of the information
Synchronous Transmission	A type of data transmission in which the sending and receiving ends operate continuously at the same frequency and in phase
TACS/ETACS	Total Access Communications Systems is a cellular system used in the United Kingdom. ETACS is used in Europe and Japan
TDMA	Time Division Multiple Access
TIA	Telecommunications Industry Association: A United States Manufacturer's group which, as part of its function, sets and publishes telecommunications standards.
Type 99™	A General Electric trademarked 2-Tone sequential format comprising 30 tones.
Trunking	A system sharing communication channels.
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration
VOGAD	Voltage Operated Gain Adjusting Device: Similar in concept to an AGC (Automatic Gain Controlled) amplifier, used to ensure full modulation of all speech levels.
VOX	Voice Operated Switching
VSB	Variable Split Band: A type of high-level analog scrambling which splits and inverts the voice band. VSB is utilized in MX-COM's IC and board level products.

Device Handling Procedures

Integrated Circuit devices and board assemblies containing integrated circuit devices are susceptible to the sudden application of thousands of volts of static electricity known as an ESD (Electro Static Discharge) event. Many modern IC's can withstand ESD discharges exceeding 4000 volts, but devices with ESD ratings of 2000 volts - and less than 2000 volts - are readily available. The threshold for human detection of static charge is about 3500 volts - an ESD discharge below this threshold limit cannot be felt.

MX-COM recommends that all semiconductor devices and assemblies containing semiconductor devices be handled, installed, and tested as static sensitive devices. Accordingly, standard ESD handling procedures should be used. These are:

- Handle sensitive devices and assemblies only at a "static-safe" work station. Generally this means:
  - use conductive work-surfaces connected to ground with a 1 MΩ resistor,
  - use grounded wrist straps (with a current limiting 1 MΩ resistor),
  - ground electrical equipment on the worksurface,
  - ban static generators such as common plastics, tapes, sprays, etc. from the worksurface, and
  - do not use hand tools with plastic handles. When plastic hand tools are necessary, treat the handles with a topical antistat.
- Use antistatic garments: Smocks, clothing and especially shoes made of highly insulating materials(such as nylon) should not be worn at the workstation. Natural materials, such as cotton, or conductive smocks should be used.
- Store and transport sensitive devices only in ESD protective enclosures. Conductive cardboard boxes and conductive or antistatic shipping tubes are examples of such enclosures.
- Maintain a relative humidity as high as practical. High humidity tends to reduce triboelectric generation of charges over large surfaces and also allows charges to bleed off to ground more easily. High humidity, however, does not wholly eliminate electrostatic problems. Static charge developed at high humidity can still cause ESD discharges capable of damaging sensitive components.
- Use antistatic surface materials where possible on sliding surfaces in automatic handling equipment.
- Use ion generating devices, such as ionized airblowers or ionizing bars, which can reduce charge buildup, especially in areas where grounding is not practical.

Package Description

Consumer Suffix		MX-COM Suffix			Summary of Available Package styles					
Old	New	1st Letter	2nd Letter	3rd Letter	# pins	Description	Pin Pitch mil(mm)	Stand-off Height (max) mil(mm)	Body Width mil(mm)	Material
P	P1 P2 P3 N/A	P			8, 14 16 18	Plastic Dual In Line(PDIP)	100(2.54)		300(7.62)	Plastic
P	N/A	P			22	Plastic Dual In Line(PDIP)	100(2.54)		400(10.16)	Plastic
P	P4 N/A P5	P			24 28 40	Plastic Dual In Line(PDIP)	100(2.54)		600(15.24)	Plastic
J	J1 J2	J			14 16	Ceramic Dual In Line package (CDIP)	100(2.54)		300(7.62)	Ceramic
J	J3	J			22	Ceramic Dual In Line package (CDIP)	100(2.54)		400(10.16)	Ceramic
J	J4 J5	J			24 28	Ceramic Dual In Line package (CDIP)	100(2.54)		600(15.24)	Ceramic
DW	D4 D3 D2 D1	D	W		16 20 24 28	wide-body Small Outline Package (SOIC)	50(1.27)	105(2.67)	300(7.59)	Plastic
	D5	D	S		24	Small Shrink Outline Package (SSOP)	25.6(0.65)	79(2.0)	209(5.3)	Plastic
LS	L2	L	H		24	Plastic Leaded Chip Carrier (PLCC)	50(1.27)	146(10.4)	400(10.16)	Plastic
	L6	L	H		44	Plastic Leaded Chip Carrier (PLCC	50(1.27)			Plastic
LH	L3	L	H	8	28	Plastic Leaded Chip Carrier (PLCC)	50(1.27)	180(4.57)	450(11.3)	Plastic
LG	L1	L	G		24	Plastic Leaded Chip Carrier with GULLWING leads	50(1.27)	98(2.5)	400(10.16)	Plastic
L	L5	N/A			24	Plastic Leaded Chip Carrier with STRAIGHT leads				
	N/A	K			24	Ceramic LeadLess Chip Carrier (CLLCC), (CLCC)	50(1.27)	88(2.23)	400(10.16)	Ceramic
	N/A	K			28	Ceramic LeadLess Chip Carrier (CLLCC), (CLCC)	50(1.27)	70(2.23)	465(12.06)	Ceramic
	M1	N/A			28	Ceramic LeadLess Chip Carrier (CLLCC), (CLCC) - Hook				
	N/A	K			44	Ceramic LeadLess Chip Carrier (CLLCC), (CLCC)	50(1.27)	70(1.77)	650(16.51)	Ceramic
	N/A	T	N		24	Thin Narrow body shrink Small Outline package (TSSOP)	25.6(0.65)	47(1.19)	175(4.44)	Plastic
	L4	T	G		48	Thin Quad Flat Pack with gullwing leads (TQFP)	20(.51)	63(1.6)	275(6.98)	Plastic
		S				Bare Die, no package				

NOTE: The letters A, B, and C following a product number refer to the product revision.

Tape and Reel Specifications

1. PURPOSE/SCOPE

1.1. This specification relates to the tape and reel packaging of integrated circuits for use in "surface mount" assembly. It includes only those dimensions which are essential for the purchasher to use the product.

2. APPLICABLE DOCUMENTS

2.1. EIA-481: Revision A Taping of Surface Mount Components for Automatic Placement.

3. DEFINITIONS

Note: For 3.1 -3.13, refer to Figure 1 and for 3.14 - 3.18, refer to Figure 4.

3.1. W: Carrier Tape Width

3.2. t: Carrier Tape Thickness

3.3. P_0: Pitch of Sprocket Holes

3.4. D: Diameter of Sprocket Holes

3.5. E: Distance from center of sprocket holes to edge of carrier tape

3.6. F: Distance from center of sprocket hole to center of pocket

3.7. P_2: Distance from center of pocket to center of divider

3.8. A_0: Inside length of pocket

3.9. B_0: Inside width of pocket

3.10. Ko: Depth of pocket cavity

3.11. P: Pitch of component pockets (center to center)

3.12. B_1: Outside width dimension of pocket

3.13. D_1: Diameter of pocket center holes

3.14. G: Inside width of reel

3.15. T: Outside width of reel

3.16. C: Sprocket hole diameter of reel

3.17. N: Hub diameter of reel

3.18. A: Diameter of reel

3.19. R: Minimum hub diameter (see Fig.5) allowed

3.20. LG: 24 lead gull wing PLCC

3.21. LH: 24 lead J-lead PLCC

3.22. DW-16: 16 lead SOIC

3.23. DW-24: 24 lead SOIC

3.24. TN: Thin Shrunk Small Outline Package(TSSOP)

3.25. D3-20: 20 lead SOIC

3.26. DS-24: Shrunk Small Outline Package(SSOP)

4. TAPE AND REEL CHARACTERISTICS

4.1. Dimensions (all dimensions in Millimeters)

Dim	LG	LH	DW-16	DW-24	TN-24	D3-20	DS-24
W	24 ± 0.3	24 ± 0.3	16 ± 0.3	24 ± 0.3	16 ± 0.3	24 ± 0.3	16 ± 0.3
t(max)	0.4	0.4	0.4	0.4	0.4	0.4	0.4
P_o	4.0 ± 0.1	4.0 ± 0.1	4.0 ± 0.1	4.0 ± 0.1	4.0 ± 0.1	4.0 ± 0.1	4.0 ± 0.1
D	1.5 +0.1/-0.0	1.5 +0.1/-0.0	1.5 +0.1/-0.0	1.5 +0.1/-0.0	1.5+0.1/-0.0	1.5 +0.1/-0.0	1.5 +0.1/-0.0
E	1.75 ± 0.1	1.75 ± 0.1	1.75 ± 0.1	1.75 ± 0.1	1.75 ± 0.1	1.75 ± 0.1	1.75 ± 0.1
F	11.5 ± 0.1	11.5 ± 0.1	7.5 ± 0.1	11.5 ± 0.1	7.5 ± 0.1	11.5 ± 0.1	7.5 ± 0.1
P_2	2.0 ± 0.1	2.0± 0.1	2.0 ± 0.1	2.0 ± 0.1	2.0 ± 0.1	2.0 ± 0.1	2.0 ± 0.1
A_o	15.8 ± 0.1	11.5 ± 0.1	10.9 ± 0.1	10.9 ± 0.1	6.95 ± 0.1	10.9 ± 0.1	8.2±0.1
B_o	15.8 ± 0.1	11.5 ± 0.1	10.7 ± 0.1	16 ± 0.1	8.3 ± 0.1	13.3 ±0.1	8.6±0.1
Ko	2.9 ± 0.1	4.1 ± 0.1	3.0 ± 0.1	3.0 ± 0.1	1.6 ± 0.1	3.2 ± 0.1	3.0 ± 0.1
P	20 ± 0.1	16 ± 0.1	12 ± 0.1	12 ± 0.1	12 ± 0.1	12 ± 0.1	12 ± 0.1
$B_{1(max)}$	16.5±0.1	20.1	12.1	20.1	9 ± 0.1	20.1	9 ± 0.1
K_1	N/A	N/A	N/A	N/A	1.2±0.1	2.7±0.1	2.3±0.1
D_1	1.5 min	1.5 min	1.6+1.0/-0.1	1.55 +1.0/-0.05	1.6+1.0/-0.1	1.5 min	1.5 min

Table 1: Carrier Tape Dimensions(reference Figure 1)

Dim	LG	LH	DW-16	DW-24	TN-24	D3-20	DS-24
A(max)	360	360	360	360	180	360	180
C	13 ± 0.2	13 ± 0.2	13 ± 0.2	13 ± 0.2	13 ± 0.2	13 ± 0.2	13 ± 0.2
N R(min per EIA)	50 (50)	80 (50)	80 (40)	80 (50)	50 (40)	80 (50)	50 (40)
G	24.4+2.0/-0.0	24.4+2.0/-0.0	16.4+2.0/-0.0	24.4+2.0/-0.0	16.4+2.0/-0.0	24.4+2.0/-0.0	16.4+2.0/-0.0
T	30.4	30.4	22.4	30.4	22.4	30.4	22.4

Table 2: Reel Dimensions (reference Figure 4)

4.2. Components on a reel

	360MM DIAMETER	180MM DIAMETER
LG	700	
LH	700	
DW-16	1200	
DW-24	1200	
D3-20	1200	
DS-24		1000
TN-24		1000

4.3. Polarity and Orientation of Components in Carrier Tape

4.3.1. All components are placed such that pin-1 is adjacent to the sprocket holes, as shown in Figure 6.

4.3.2. The mounting side of the component is oriented to the bottom side of the carrier tape as shown in Figure 2.

4.4. Placing of Components in Carrier Tape

4.4.1. The Cover Tape does not cover the sprocket holes

4.4.2. The tapes in adjacent layers do not stick together in the finished reel.

4.4.3. The adhesive of the cover tape does not affect the mechanical and electrical characteristics and marking of the components.

4.4.4. Components do not stick to either the carrier tape or the cover tape.

4.4.5. The tapes will withstand storage without danger of emitting any vapors which might impair soldering or chemically deteriorate the components or component leads.

4.4.6. When the tape is bent to the minimum radius of R mm, as shown in Figure 5 and Table 2, the tape is not damaged and the components remain in their position and orientation in the tape.

4.4.7. The carrier tape is conductive.

4.4.8. The cover tape is antistatic.

4.4.9. The peel strength of the cover tape is 60-90 grams, measured at an angle of 175^{o} to 180^{o} and a peel speed of 184 mm/minute, with respect to the carrier tape along its longitudinal axis.

4.5. Packaging

4.5.1. At the start of each carrier tape, a minimum of 75 empty compartments are passed before placing components into the carrier tape compartments.

4.5.2. At the end of the tape (carrier plus sealed cover), there is a trailer tape which is a minimum of 40 empty components.

4.5.3. The tape releases from the reel hub as the last portion of the carrier tape unwinds from the reel.

4.5.4. The tape is prevented from unreeling by winding an additional strip of cover tape around the outside of the reel between 2 and 3 times. Secure the tape on the reel with a small tab of self-adhesive tape.

4.5.5. All reels display the following information:

MX-COM or Customer Specific device type
Quantity on reel
Date Code
Static Sensitive warning label
Barcode Label per customer request

4.6. Storage Conditions and Shelf Life

4.6.1. Ideal storage conditions are $15^{o}C$ to $20^{o}C$ with a relative humidity of 60-70%.

4.6.2. Maximum estimated shelf life when stored at ideal conditions is 18 months.

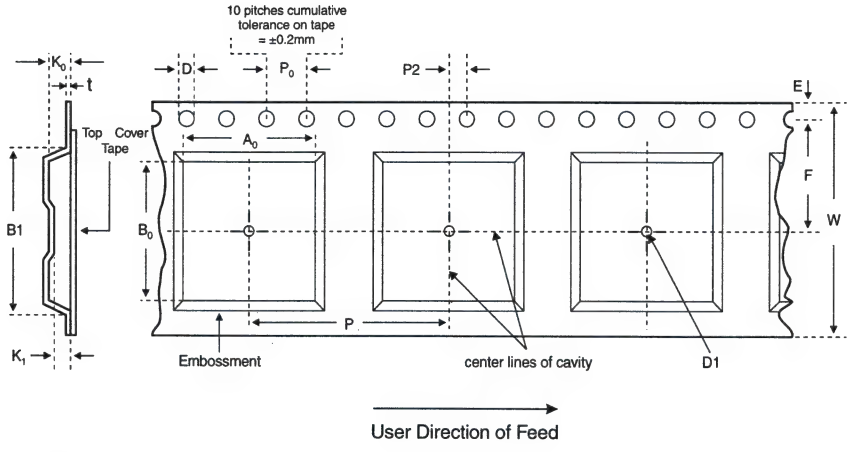


Figure 1. Embossed Carrier Dimensions

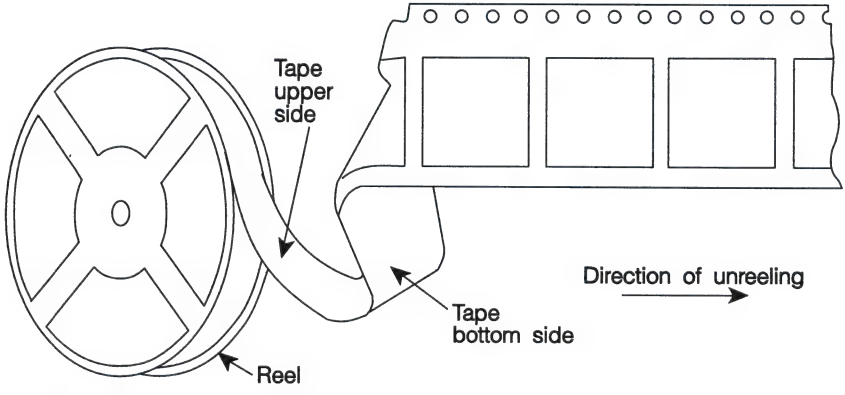


Figure 2. Tape Top and Bottom Orientation

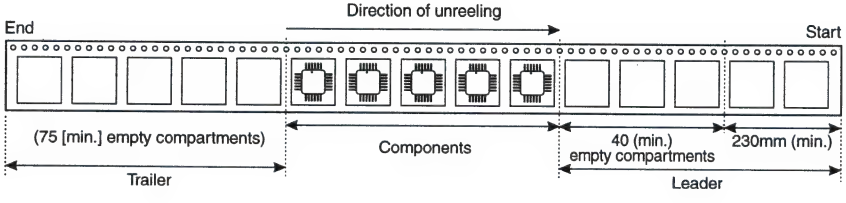


Figure 3. Layout of Tape

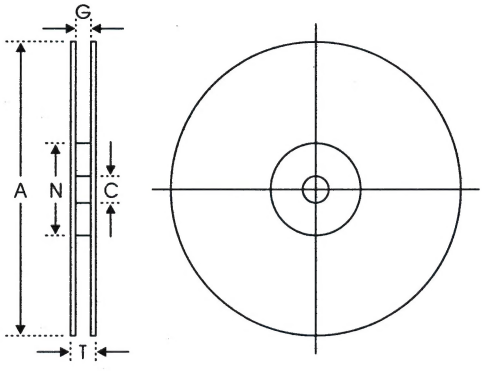


Figure 4. Reel Dimensions

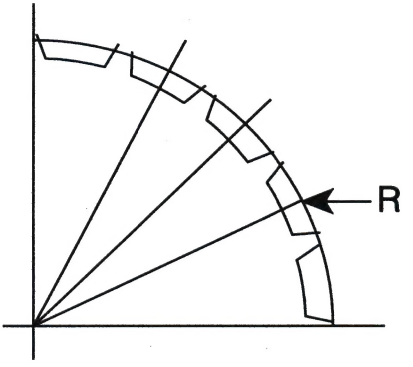
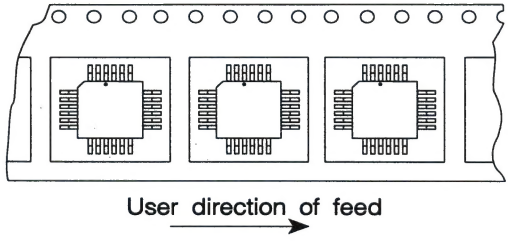
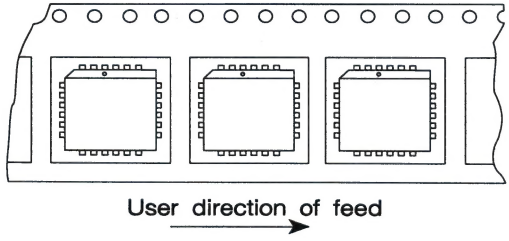


Figure 5. Minimum Radius = 50mm

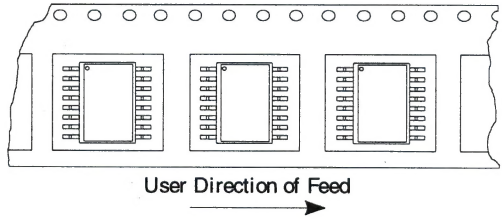
LG Package



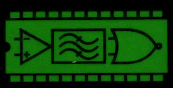
LH Package



DW Package



Fgure 6. Component Orientation



MX•COM, INC.

MiXed Signal ICs & Modules

Wireless Modems
Telephony
Sub-Audio Tone Signaling and Detection
Sequential Tone Signaling
Voice Processors
CVSD Codecs
Voice Security
Cellular
General Purpose

4800 Bethania Station Road, Winston-Salem, NC 27105-1201
Tele: 800 638 5577 910 744 5050 Fax: 910 744 5054
www.mxcom.com